

**INPUT DEVICE HAVING TWO JOYSTICKS AND
TOUCHPAD WITH DEFAULT TEMPLATE**

Field of the Invention

The present invention relates generally to coordinate-type pointing devices for use with digital systems and, more specifically, to an input device having a touchpad with an inscribed default template
5 associated therewith, a retainer for removably securing template overlays to the pad surface, and a pair of joysticks positioned one to each side of the touchpad.

Background of the Invention

Video graphics computer systems are well known,
10 popular consumer products. A typical system includes a data processing unit that connects to an ordinary television set for displaying images of a game or other application. The data processing unit receives controlling software from a read only memory (ROM) that
15 is usually packaged in the form of a cartridge. The cartridge is removably plugged into the data processing unit. At least one pointing device, such as a mouse, joystick, touchpad, touchscreen, switch pad, or light gun, is also connected to the data processing unit to
20 allow the player to input positional information that is used by the controlling software to execute the application.

The data processing unit typically has a single central processing unit (CPU) and associated volatile
25 and non-volatile memory, including all random access memory (RAM) and bootstrap read-only memory (boot ROM), a television (RF video) signal generator, and an input/output (I/O) processor to interface to the various pointing devices. These devices are in circuit
30 communication. One distinguishing characteristic of these systems is the use of a motherboard or system

This Sheet Has Been Replaced



planar to electrically connect these components together.

Joysticks are directional type pointing devices used to input directional data to computer systems. 5 Joysticks typically comprise a base and an elongated "stick," which is typically gripped by the hand of the user. The "stick" typically pivots from a point at the base and has a default position perpendicular to the base. Pivotal motions of the stick away from the 10 default perpendicular position are interpreted as a directional input parallel to the base in the direction needed to displace the stick from the default perpendicular position. Typically a button is located at the top portion of the stick. Closure events of the 15 switch are used as control inputs for applications executing on the computer system.

Touchpads are coordinate type pointing devices used to input coordinate type data to computer systems. The touchpad is typically a pressure-sensitive bounded 20 plane capable of detecting localized pressure at its surface. When a user touches the surface with a finger, stylus, or the like, the touchpad reports to the attached computer system the coordinates of the location touched. In response, the computer performs the 25 function, if any, associated with the location pressed.

Typically one or more regions of the touchpad are assigned to certain functions within the system. The user is made aware of what function is associated with each region by a template. A template is a sheet with 30 a graphic design and is typically placed over and in contact with the touchpad surface. The graphic design typically maps out regions of the touchpad surface and the regions are typically labeled to provide a reminder



to the user as to the functions associated with the various mapped regions.

Touchpad systems typically either (1) have a permanent template inscribed in or on the touchpad surface and are incapable of accepting template overlays or (2) have no permanent inscribed template but have the means for accepting template overlays. Therefore, each application using the touchpad as an input device must either use the permanent inscribed template exclusively or provide a template overlay. Thus, typical systems force software application designers to either limit the possible inputs from the touchpad (by using only the permanent template) or design and define one or more custom templates for use with that particular software application.

Moreover, joysticks are typically combined only with switches and other closure type input devices. Thus, joysticks are typically not used with other input devices in a coordinated fashion.

Summary of the Invention

According to the present invention, an input device is provided having a touchpad and a pair of joysticks positioned one to each side of the touchpad. The joysticks are positioned to allow two people, e.g., an adult and a child, to provide positional inputs to the computer system simultaneously and in such a manner that one person can aid the second.

The touchpad has an inscribed default template graphical design and a retainer for removably securing other template overlays to be used with the touchpad instead of the default template graphical design. The default inscribed template has a set of commands usable by many software applications. The template overlays



have command sets for one or more specific software applications.

It is therefore an advantage of the present invention to provide an input device configured to allow
5 two people to provide positional information simultaneously and to provide command access in a complete package.

It is therefore a further advantage of the present invention to provide software applications with a common
10 set of functions accessible from a default template graphical image while at the same time giving software applications access to custom template overlays.

These and other advantages of the present invention will become more apparent from a detailed
15 description of the invention.

Brief Description of the Drawings

In the accompanying drawings, which are incorporated in and constitute a part of this specification, embodiments of the invention are
20 illustrated, which, together with a general description of the invention given above, and the detailed description given below serve to example the principles of this invention.

Figures 1A and 1B are block diagrams showing the
25 general layout of the system of the present invention;

Figure 1C is a schematic diagram showing the details of the video digital to analog converter used in the system of the present invention;

Figure 2A is a top plan view of the input device
30 of the present invention showing the touchpad with default template, the two joysticks, and a template overlay;



Figure 2B is a top plan view of the input device of the present invention with a template overlay inserted into the template overlay retainer;

Figure 2C is an enlarged fragmentary plan view of
5 a portion of the input device of the present invention shown in Figure 2B;

Figure 2D is a sectional view taken substantially along the plane designated by the line 2D-2D of Figure 2C;

10 Figure 2E is a sectional view taken substantially along the plane designated by the line 2E-2E of Figure 2C;

Figure 2F is a sectional view taken substantially along the plane designated by the line 2F-2F of Figure
15 2A;

Figure 2G is a fragmentary top plan view of the view of the input device of the present invention shown in Figure 2A with parts broken away for clarity;

Figures 2H-2K are bottom plan views of different
20 embodiments of an edge of a template overlay showing the identification patterns;

Figure 2L is a front elevational view of the input device of the present invention;

Figure 2M is a partial sectional view taken
25 substantially along the plane designated by the line 2M-2M of Figure 2A showing the details of the joysticks used in the input device of the present invention; and

Figure 3 is a block diagram showing the electrical circuitry of the input device of the present invention.

30 **Detailed Description of the Preferred Embodiment**

Referring to Figures 1A and 1B, a computer system
10 of the present invention is shown. As shown in Figure 1A, the system 10 comprises a data processing unit 12 with a program cartridge 14 removably connected

thereto. Also connected to the data processing unit 12 is a standard television set (TV) 16, and an input device 18, which has a touchpad 19 and two joysticks 20a, 20b. The input device 18 sends to the data
5 processing unit 12 coordinate type data corresponding to the location of a touch of a finger, stylus 21, or the like on the touchpad 19. In addition, the input device 18 sends to the data processing unit 12 directional type data corresponding to movements of the joysticks 20a,
10 20b. Although not shown in Figure 1A, the standard TV 16 can be replaced with a pair of speakers and a display device that accepts a composite video signal. The input device 18 connects to the data processing unit 12 via a serial data link 22. The TV 16 connects to the data
15 processing unit 12 via an RF video line 24.

The cartridge 14 has an edge card connector, indicated generally at 26, which connects to a cartridge connector 28 thereby electrically connecting devices in the cartridge 14 to devices in the data processing unit
20 12.

The processing unit 12 comprises a central processing unit (CPU) 30, having a SYSTEM bus 31 associated therewith, an audio/video (A/V) controller/coprocessor 32, a system memory 33, which is
25 connected to a SYSTEM' bus 34 generated by the A/V controller/ coprocessor 32 from the SYSTEM bus 31, first and second decoder chips (not shown), an I/O coprocessor 36, two cartridge connectors (one indicated at 28, the other not shown), additional circuitry 38 required to
30 generate the audio and video signals, and an expansion connector 39. These devices are connected in circuit communication as shown in the Figures. The additional circuitry 38 is shown in Figure 1B and discussed in more detail in the text accompanying Figure 1B.

The CPU 30 generates multiple buses: a DATA bus, an ADDRESS bus, and a CONTROL bus, as are well known in the art. These three buses are collectively referred to as the SYSTEM bus 31. In the preferred embodiment, the CPU 30 is an 80376, manufactured by Intel Corp., 3065 Bowers Ave., Santa Clara, California, 95051. The 80376 is a variation of the well known 80386SX, which is well known in the art and also available from Intel Corp. The 80376 differs from the 80386SX in that the 80376 starts up in 32-bit mode, rather than 16-bit mode. Specifically, the CR0 register is forced to a 0011H (0011 in hexadecimal notation) state with bit 0 forced to a logical ONE, effectively making the 376 operate in a 32-bit memory mode. Paging is enabled to allow virtual 386 operation.

The A/V controller/coprocessor 32 generates three spare general purpose I/O decoder lines (GPIO1, GPIO2, and GPIO3) from the SYSTEM bus 31, each providing a 32-bit I/O address range. The general purpose decoders can be used to provide three active low chip enables to devices external to the A/V controller/coprocessor 32. In the data processing unit 12, the general purpose decoders are used to decode address ranges to the I/O coprocessor 36 (GPIO1) and the two cartridge connectors (GPIO2 and GPIO3). The remaining circuitry of the A/V controller/coprocessor 32 is discussed below.

The system memory 33 comprises screen RAM, system RAM, and bootstrap ROM (all not shown). The on-board screen RAM and system RAM is 1 megabyte of 32-bit DRAM. Suitable DRAM are a pair of TCS14170BJ 256 kilobyte by 16-bit memory chips, manufactured by Toshiba, configured to provide a 32-bit memory. A portion of the address space of the CPU 30 is decoded to a number of eight-bit registers within the A/V controller/ coprocessor 32.

All internal locations are on even address boundaries; word-wide I/O reads and writes can be performed where appropriate. In this particular embodiment, the byte-wide writes cannot be performed on word-wide registers
5 and I/O cycles cannot be used to access odd addresses.

The bootstrap ROM is always 16 bits wide. The bootstrap ROM comprises two 27C512 erasable programmable read-only memories, manufactured by numerous manufacturers, thereby giving 128K of bootstrap ROM.
10 Following a reset, the one megabyte window from F20000H to FFFFFFFH containing ROM and internal memory is repeated throughout the 16 megabyte address range.

The system memory 33 is shared between a number of devices. The A/V controller/coprocessor 32 is the
15 arbitrator for the system memory 33; therefore, the SYSTEM bus 31 is modified to a SYSTEM' bus 34 (comprising a DATA' bus, an ADDRESS' bus, and a CONTROL' bus, all not shown) by the A/V controller/coprocessor 32. Thus, the system memory 33 is accessed via the
20 SYSTEM' bus 34.

The I/O coprocessor 36 interfaces the CPU 30 to numerous input devices, such as the input device 18 and optional devices such as a keyboard (not shown), controllers (not shown), a mouse (not shown), and a
25 printer (not shown). In the preferred embodiment, the I/O coprocessor 36 is a preprogrammed MC68HC705C8 (hereinafter "68HC705"), manufactured by Motorola Corp, running at 2 MHz. The 68HC705 I/O coprocessor 36 is interfaced to the CPU 30 by configuring the 68HC705 as
30 a peripheral device: (1) PA0-PA7 are connected to D0-D7 of the DATA bus; (2) PB7, PB1, and PB2 are connected to GPIO1 (a 32-byte address range decoded by the A/V controller/ coprocessor 32, as described below), A1, and A2, respectively, of the CONTROL bus and ADDRESS bus;



and (3) PB3, PB4, and PB5 are connected to ADS, READY, and W/R, respectively, of the CONTROL bus. The I/O coprocessor 36 is decoded by the A/V controller/coprocessor to have four 16-bit addresses in I/O space (referred to herein as AS0, AS2, AS4, and AS6).

The program inside the 68HC705 interfaces to the CPU 30 as follows. The 68HC705 is designed to attach directly to the processor bus and act as an I/O port to the CPU 30. A pair of internal latches holds data passing between each of the processors until the other is ready to receive it. Status bits to each processor indicate the condition of the data latches. Each can tell if the previous data has been read and if any new data is waiting to be read by checking the status bits.

The I/O coprocessor 36 implements, inter alia, the following functions: (1) a 50 ms timer, (2) a serial controller link for receiving communication packets from the input devices, (3) a cartridge/expansion sense, for determining the presence or absence of a cartridge 14 in each cartridge connector and the presence or absence of an expansion device or CD drive in the expansion connector, (4) a system reset, and (5) an I²C nonvolatile RAM (NVRAM) interface. The I/O coprocessor 36 also implements an optional DSA compact disk control serial line to allow communications with an optional CD device.

The 50 ms timer is implemented by configuring the watchdog timer of the 68HC705 I/O coprocessor 36 to expire at regular 50 millisecond intervals. Each time the watchdog timer expires, the I/O coprocessor 36 interrupts the CPU 30 using analog interrupt 0 (AI0) of the A/V controller/coprocessor 32 (the A/V controller/coprocessor interrupts the CPU via the IRQ line in response to the I/O coprocessor pulling AI0



low). The CPU enables and disables the 50 ms timer by writing either the byte 0F0H or the byte 00H, respectively, to the I/O port AS0. The timer defaults to being enabled.

5 During the interrupt acknowledge cycle of the CPU, the A/V controller/ coprocessor asserts the address of the interrupt handling routine. The interrupt handling routine causes the CPU 30 to read one or more bytes from the 16-bit I/O port AS0, which corresponds to the I/O
10 coprocessor. During each read of I/O port AS0, the A/V controller/ coprocessor 32 to selects the I/O coprocessor 36, thereby allowing a data transfer between the CPU 30 and the I/O coprocessor 36.

15 The I/O coprocessor 36 will always have one byte to be transferred to the CPU in response to the 50 ms interrupt. The lower nibble of this byte contains the number of expirations of the 50 ms time since the last interrupt acknowledge cycle and the upper nibble of this byte contains the number of I/O device messages to be
20 transferred to the CPU. If the 50 ms timer is disabled, then the lower nibble of this byte will be zero. If more than 15 messages have been received, then 15 is sent in the upper nibble and any remaining messages are sent during the next transfer. Depending on the
25 contents of this first byte, the CPU might read subsequent bytes from the I/O coprocessor 36, which will, for the most part, be packets of data from input devices. Typically, the input devices will only send messages when their respective states change, thereby
30 keeping message transmission frequency very low.

The input device 18 and all other input devices are connected to the I/O coprocessor 36 via the serial data link 22. The individual input devices (e.g., the input device 18) transform the movements of the control



devices into a format suitable for transmission along the serial link 22. The input device 18 sends data packets via the serial data link 22 to the system unit 12. As will be explained below, the structure of the data packets differ depending on the type of input device. Coordinate type devices (mouse, analog joystick, touchpad, etc) have a different data packet structure than a switch closure type of device (keyboard, digital joystick, switch pad, etc).

10 The serial controller link 22 consists of three (3) lines: a data receive line, a VCC (+5 VDC) line, and a ground line. The 68HC705 implements the data receive line of the controller serial link using the PD0/RDI pin of the 68HC705. This pin is designed to be
15 used as an interface to serial devices using the well known asynchronous format. Serial transmissions have the following format: 4800 bits per second, no parity, 8 data bits, and one stop bit. A clocked synchronous format could be used in the alternative. The serial
20 controller link 22 is connected to external devices by a six-conductor mini-din plug connector (not shown), which are well known in the art. Input devices are daisy chained, thus a single device physically connects to the data processing unit 12. For example, if a so-
25 called mouse pointing device is added to the system 10, the mouse is connected to the input device 18, which is connected to the processing unit 12.

The cartridge sense and expansion sense are for determining the presence or absence of a cartridge 14 in
30 each cartridge connector or the expansion connector and is implemented by having the I/O coprocessor 36 poll a pin of the cartridge connector 28. The pin is pulled to a logical ONE by a suitable pullup resistor (not shown) on the system planar and a properly connected cartridge



14 pulls the pin to a logical ZERO. Thus, a ONE at each cartridge sense indicates the absence of a cartridge 14 and a ZERO indicates the presence of a cartridge 14. Likewise, a ONE the expansion sense indicates the absence of an expansion device, such as an optional CD drive, and a ZERO indicates the presence of an expansion device.

The reset is implemented by giving the I/O coprocessor 36 control over the reset signal of the A/V controller/coprocessor 32, which in turn controls the reset signal of the CPU 30. The CPU 30 can command the I/O coprocessor 36 to reset the system 10 by causing the I/O coprocessor 36 to reset the A/V controller/coprocessor, which in turn resets the CPU 30. The CPU causes the I/O controller to generate a system reset by writing the byte 0FFH to I/O port AS0. In addition, the I/O coprocessor 36 monitors the optional reset switch (not shown) for the system and resets the system when it detects a switch closure.

Finally, the I/O coprocessor implements an I²C nonvolatile RAM (NVRAM) interface to read, write, and verify the contents of 512 bytes of nonvolatile system RAM. The NVRAM (not shown) comprises a PCF8594 manufactured by Philips Semiconductor and is in circuit communication with the I/O coprocessor via the I²C interface. More than one PCF8594 can be cascaded to provide more NVRAM capability. To access the NVRAM, a three-byte sequence is used. All three bytes are accessed through I/O port AS0. The first byte written to the I/O coprocessor by the CPU indicates whether the transfer is a read or a write and gives the I/O coprocessor a segment address. The lower nibble of this byte indicates the type of transfer: 01H indicates a write from NVRAM and 02H indicates a read from NVRAM.



The upper nibble of this byte is a 4-bit segment number corresponding to a 256-byte segment of NVRAM. With 512 bytes of NVRAM, only the bottom two segments (0 and 1) are used. For both reads and writes, the next byte is the same--the next byte is written by the CPU and is the address of the byte being accessed within the segment. The last byte is either written to or read from the I/O coprocessor by the CPU and is the data byte read from or to be written to the NVRAM.

10 In the alternative, the I/O coprocessor can be implemented in other ways. For example, a tristated readable shift register might suitably receive the information from the serial data link 22. In that case, the CPU 30 periodically reads the shift register to
15 access the data packets from input devices.

The first decode chip (not shown) is in electrical circuit communication with the CPU 30, the A/V controller/ coprocessor 32, and the two cartridge connectors 28 (the other not shown). The first decode
20 chip accepts as inputs the upper two address lines of the SYSTEM bus 31, decodes the 16 megabyte address space of the 80376 CPU 30 into four 4 megabyte regions, represented by three chip select lines: two for the cartridge connectors 28 (the other not shown) and one
25 for the A/V controller/coprocessor 32. The upper four megabytes and the lower four megabytes are decoded to the A/V controller/coprocessor chip select and the two remaining four-megabyte regions are decoded to two cartridge connector chip selects.

30 The second decoder chip (not shown) is used to implement the chip select for the expansion connector 39. The second decode chip is in circuit communication with the A/V controller/coprocessor 32 and the expansion connector 39 along the SYSTEM' bus 34. The second



decode chip permits the A/V controller/coprocessor 32 to decode a 128K block of system ROM starting at F20000H. The range from F40000H to FFFFFFFH is decoded by the second decode chip for use by the expansion connector 39. This block of ROM decoded by the second decode chip is used to add ROM to the system 10 via the expansion connector 39.

The data processing unit 12 also has a pair of cartridge connectors (one indicated at 28, the other not shown) for placing a cartridge 14 in circuit communication with the CPU 30 and other system components. The cartridge 14 connects to the connector 28 of the data processing unit 12 via a gold plated 62-pin (two rows of 31 conductors) edge card connector 26. The processor unit 12 has two cartridge connectors 28 for accepting the edge card connections of the edge card connector 26. The cartridges 14 have gold plated card edge connections to match the conductors of the connectors 28, allowing the cartridges 14 to be pluggably connected to the processor unit 12. The following signals are communicated to external devices via the cartridge connectors 28 (the other not shown): SYSTEM bus 31 signals, a cartridge sense line, power, ground, analog interrupt 1 or 2 (each cartridge has a unique interrupt), GPIO 2 or 3 (each cartridge has a unique chip select), a lock line (which is a typical signal of the 80376 and 80386SX SYSTEM bus 31), and a cartridge select, which is generated by the first decode chip. In the alternative, the signals needed to connect to an optional CD drive can also be connected to external devices via the cartridge connector 28.

In addition, the processor unit 12 has a single 112-pin (two rows of 56 pins each) edge card expansion connector 39. The expansion connector 39 allows devices



to add more memory to the system memory 33 and to add various other features. Devices connected to the expansion connector 39 have gold plated card edges to match the expansion connector, allowing the devices to be pluggably connected to the processor unit 12. The following signals are communicated to external devices via the expansion connector 39: SYSTEM' bus signals, an expansion connector 39 sense line, power, ground, CAS and RAS lines, and an expansion connector 39 select, which is generated by the second decode chip. In the alternative, the signals needed to connect to an optional CD drive can also be connected to external devices via the expansion connector 39.

The program cartridge 14 comprises a program ROM 40 and a decoder 42. In the alternative, the decoder 42 can be designed into the processing unit 12. The program ROM 40 contains code suitable for execution on the CPU 30 in a read only memory format. In the alternative, other memory types, such as battery-backed RAM can be used as the storage device in the cartridge 14. The program ROM 40 is in circuit communication with the CPU 30, as shown in Figure 1A.

The address decoder 42 within the cartridge 14 decodes the full width of the ADDRESS bus to a memory range appropriate for the program ROM 40 and generates a chip select signal 44 required by the ROM 40, as is well known in the art. The address decoder 42 is implemented in a 16V8 programmable array logic (PAL), which is well known in the art and is manufactured by numerous manufacturers, e.g., AMD Corp. If the decoder 42 is designed into the processing unit 12, then the select 44 is electrically communicated to the ROM 40 by the connector 26.



Referring now to Figure 1B, the additional circuitry 38 of Figure 1A is shown connected to the A/V controller/coprocessor 32. The additional circuitry 38 comprises four devices: a video digital-to-analog converter (video DAC) 50, an NTSC/PAL ("PAL" referring to the well known European television signal standard) encoder 52, an audio digital-to-analog converter/analog-to-digital converter/compressor/decompressor (ADC/DAC/CODEC) 54, and an RF modulator 56. Each is connected as shown in the Figures.

The Audio/Video controller/coprocessor (A/V controller/coprocessor) 32 electronics are largely contained within one massive custom logic chip, known as an ASIC (Application Specific Integrated Circuit). An A/V controller/coprocessor 32 meeting the description herein can be purchased from MSU Ltd., 270 Upper 4th Street, Witan Gate West, Central Milton Keynes, MK9 1DP England. The A/V controller/coprocessor 32 contains a processor interface 60, a processor cache 62, a memory interface/refresh 64, a video controller 66, an interrupt controller 68, a video blitter 70, an optional CD block decoder, a digital signal processor (DSP) 74, and a DSP memory 76. The processor interface 60, the memory interface/refresh 64, and the video controller 66 are referred to collectively as the video/memory controller 67. The system memory 33, central processing unit 30, and other devices lie outside the A/V controller/coprocessor 32.

The A/V controller/coprocessor 32 generates the SYSTEM' bus 34 from the SYSTEM bus 31, thereby isolating the CPU 30 from the system memory 33. Thus, the SYSTEM' bus 34 electrically connects the various devices to the system memory 33. Sharing the SYSTEM' bus 34 are six possible bus masters (in order from highest priority to



lowest priority, respectively): the memory refresh 64, the video controller 66, an optional CD block decoder (not shown), the DSP 74, the blitter 70, and the CPU 30 (through the processor interface 60). Only one of the bus masters can control the SYSTEM' bus 34 at any one time. The arbitrator within the video/memory controller 67 controls the changing priorities of the devices, as described herein, and is in electrical circuit communication with all the devices within the A/V controller/coprocessor 32. For example, the CPU 30 has the lowest priority of all bus masters until an interrupt occurs. Thus, the arbitrator is in circuit communication with both the CPU interface 60 and the interrupt controller 68.

15 The cache 62 is not a cache in the sense that it prefetches instructions for the CPU 30. Rather, the cache 62 is a 512 x 16-bit static RAM located at F14000H to F143FFH that can be used by the CPU 30 for variables, stack, or program code to speed up program execution.

20 The video/memory controller 67 (the processor interface 60, the memory interface/refresh 64, and video controller 66) controls the SYSTEM' bus 34, and provides the memory timing signals (e.g., CAS, RAS, write enable, etc.) for memory devices attached to the SYSTEM' bus 34, as is well known in the art. It suspends bus master operations during video lines for brief periods to fetch any video display data, and to refresh dynamic RAM (DRAM). It also controls the interface with the CPU 30.

30 The video controller 66 has a flexible video timing generator that can be programmed to suit different TV standards and monitors up to a 640 by 480 VGA standard. The exact video format is controlled by setting various registers in the A/V controller/coprocessor: horizontal period, horizontal sync,



horizontal blanking end, horizontal blanking begin,
horizontal display begin, horizontal display end,
horizontal fetch begin, horizontal fetch end, horizontal
vertical sync, vertical period, vertical sync, vertical
5 blanking end, vertical blanking begin, vertical display
begin, vertical display end, video interrupt, and light
pen registers. The video controller 66 has three color
resolutions available: four bits per pixel, eight bits
per pixel, and 16 bits per pixel. The memory map of the
10 screen is not tied to the video display width, but is
defined independently.

The video/memory controller 67 decodes the 16
megabyte address range of the 80376 CPU 30 into the
following memory map: 1 MB of system RAM (000000H -
15 0FFFFFFH), 4 MB for the first cartridge ROM (400000 -
7FFFFFFH), 4 MB for the second cartridge ROM (800000 -
BFFFFFFH), 64 KB of internal memory for the audio/video
controller/coprocessor (F10000H - F1FFFFH), and a 128 KB
block of system ROM (FE0000H - FFFFFFFH). The 64
20 kilobytes of internal memory comprises palette RAM,
blitter registers, and DSP registers and memory. The
palette address range was stated above. The blitter
registers extend from the range F10400H to F107FFH. The
DSP memory extends from F10800H to F18000H.

25 if the optional CD drive is added to the system,
the following regions are added to the memory map:
another 1 MB of system RAM (100000H - 1FFFFFFH) and 128
KB for the CD drive (FC0000H - FFFFFFFH).

The interrupt controller 68 interfaces six
30 internal interrupts to the CPU 30: video interrupt
(highest priority), analog interrupt 0 (AI0), analog
interrupt 1 (AI1), analog interrupt 2 (AI2), CD block
decoder interrupt, and DSP interrupt (lowest priority).
The interrupt controller automatically clears an



interrupt when the CPU 30 performs the interrupt acknowledge cycle. A mask bit is available for each of the interrupts.

5 The blitter 70 is a graphics processor for fast screen updates and animation, acting as a hardware graphics subroutine for the CPU 30 or DSP 74. It executes commands written by the CPU 30 and the DSP 74 into memory. It can perform arbitrarily long sequences of graphics operations by reading new command sets from
10 system memory 33. It becomes bus master through blitter program operation, and can therefore have exclusive control of the SYSTEM' bus 34 for considerable periods. However, its priority over the CPU 30 is not absolute; it can be requested to give up the SYSTEM' bus 34 to the
15 CPU 30 when an interrupt occurs. The CPU 30 is the lowest priority bus master at the system level; however, it has complete control of the other hardware, therefore, the use of the SYSTEM' bus 34 is entirely under CPU 30 program control.

20 The blitter 70 has a versatile comparator to allow intelligent blitting operations, and a logic function unit (LFU) to generate the output data. The logic function unit can combine the contents of the data registers in a number of useful ways to produce the
25 output data and the comparator can perform certain comparisons on the data to inhibit write operations, and optionally stop blitter operation.

The logic function unit generates the output data, which is written to the destination in system memory 33.
30 It can perform any logical combination of the source and destination register pixels. "Source data pixels" can be selected from either of the source data register or the data pattern data register. The LFU selects any of the four Boolean minterms ($A \& B$, $\bar{A} \& B$, $A \& \bar{B}$, and $\bar{A} \&$



B) of the two sets of input data from the data registers, and generates the logical OR of the two selected minterms. This allows any logical combination of input data; thus 16 functional possibilities exist.

5 The comparator can perform a variety of comparisons on the data in the source, destination, and pattern data registers. If its comparison conditions are met, then it generates an inhibit signal. The inhibit signal is used to inhibit a write operation, and
10 optionally, to stop the blitting operation. The comparator can also be used to provide a pixel plane effect, to give transparent colors, for collision detection and system memory 33 search operations, and as an aid to character painting.

15 The DSP 74 is a simple, very high-speed processor for sound synthesis, operating at up to 33 million instructions per second (MIPs). It has access to the SYSTEM' bus 34 via a DSP DMA controller (not shown), which allows it to read and write bytes or words into
20 system memory 33. These transfers occur in short bursts, and are under DSP program control. The DSP 74 actually executes programs and stores data in its own private high-speed memory 76.

 The DSP 74 audio coprocessor is a general purpose
25 arithmetic coprocessor with sufficient power to implement a high performance music synthesizer. Synchronous serial outputs are provided for a generation of stereo audio signals with 16 bit precision, giving a sound quality normally associated with compact disc
30 technology. The DSP 74 is micro-programmable from the host CPU 30 and the instruction set is sufficiently flexible to enable the user to program the device to fulfill many different functions that are quite different from that of "music synthesizer." Such



applications might include algorithmic speech generation, audio analysis using fast Fourier transform techniques, and three-dimensional graphics rotations. The DSP 74 uses Harvard architecture (separate program
5 and data buses) for maximum data throughput. The DSP 74 has an arithmetic logic unit (ALU), which features a hardware 16-bit by 16-bit hardware multiply/accumulate as well as addition, subtraction, and logical functions. There is also a separate serial divide unit, which
10 generates one quotient bit per tick.

The ALU within the DSP 74 is a 16-bit arithmetic logic unit, with the same functions as a Texas Instruments 74181, which is well known in the art. Common arithmetic operations are encoded as
15 instructions; uncommon instructions can be performed by directly setting up the ALU mode bits with the general purpose arithmetic instruction (GAI).

The DSP 74 has a DSP memory 76 associated with it. The DSP memory 76 comprises program RAM, data RAM, a
20 register/constant table, and a sine ROM (all not shown). The DSP memory 76 in general is accessible in both the DSP's internal address space as well as the address space of the system memory 33. The DSP program RAM is 512 18-bit words. These locations can only be written
25 by the CPU 30, and are program read-only as far as the DSP 74 is concerned. Program RAM does not appear in the DSP internal address space. The program RAM is not accessible to the host when the DSP 74 is running, but is accessible when the DSP is idle.

30 The DSP 74 also has a serial audio digital-to-analog convertor (DAC) interface. The serial DAC interface allows the DSP 74 to both drive a synchronous serial (I²S or similar) DAC, and to input data from a synchronous serial data source such as a CD drive.



The video controller 66 of the A/V controller/coprocessor 32 connects to the external video DAC 50, which converts the eighteen bits of pixel information 78 (six bits each of red, green, and blue) from the video controller 66 into an RGB signal 80, as is well known in the art. Each color channel (R 80a, G 80b, and B 80c) of the video DAC 50 is implemented with an R2R resistor tree and a 2N2222 transistor, as shown in Figure 1C. The devices in Figure 1C are in circuit communication, as shown. The resistors 86a-86j in Figure 1C are all 0.25 watt resistors with the values shown, within 5% tolerance. The transistor 88 is a 2N2222.

Referring once again to Figure 1B, the RGB signal 80 is converted to an NTSC composite video signal 90 by the NTSC/PAL encoder 52. The NTSC/PAL encoder 52 accepts the chroma clock 92, the HSYNC and VSYNC signals 94, which are generated by the video controller 66 of the A/V controller/coprocessor 32, and the red 80a, green 80b, and blue 80c video outputs, which are generated by the video DAC 50, and generates a composite video signal 90 in the well known NTSC or baseband video format. In the alternative, the well known PAL (European television signal standard) format can be generated. The composite video signal 90 is connected to external devices with a single female RCA type phono jack (not shown), as is well known in the art. In the preferred embodiment, the NTSC/PAL encoder 52 is a CXA1145, manufactured by Sony Corp. In the alternative, an MC1377, manufactured by Motorola Corp. can be used.

The audio ADC/DAC/CODEC 54 is linked to the DSP 74 with a serial link 96 conforming to the well known Philips I²S protocol. The ADC/DAC/CODEC 54 converts analog data to digital data, and vice versa, and compresses and decompresses digital data. The



ADC/DAC/CODEC 54 interfaces external stereo analog data 97a-97b from optional microphones to the A/V controller/coprocessor 32. The audio inputs 97a-97b are connected to external devices with a standard stereo 1/4" connector. The audio ADC/DAC/CODEC 54 also interfaces digital data from the A/V controller/coprocessor to external devices by generating left and right audio line out signals 98a-98b. These signals 98a-98b are connected to external devices, such as optional speakers (not shown) with two female RCA phone jacks, as are well known in the art. As mentioned below, the audio line signals 98a-98b are also added to the RF video signal 22.

In the preferred embodiment, the ADC/DAC/CODEC 54 is a CS4216, manufactured by Crystal Semiconductor. The part contains microphone inputs, with programmable gain, as well as outputs with programmable attenuators. Gain and attenuation are both programmably controlled by the DSP 74.

In the alternative, the ADC/DAC/CODEC 54 can be replaced with a TDA1311 DAC manufactured by Philips. If this chip is used, the ADC and CODEC functions will not be available.

The RF modulator 56 merges the composite video signal 90 from the NTSC/PAL encoder 52 with the left and right audio line out signals 98a and 98b from the audio ADC/DAC/CODEC 54 onto a carrier frequency to generate an RF video signal 22 that is suitable for being directly inputted into the TV 16. To generate the different PAL (European television signal standard) and NTSC formats a different RF modulator and crystal must be used. The RF video signal 22 is connected to external devices with a single female Type F coaxial connector, as is well known in the art.



Referring now to Figures 2A-2M and 3, an embodiment of the input device 18 of the present invention is shown. As shown in that figure, the input device 18 comprises a touchpad 19 and two joysticks 20a, 20b enclosed in a single enclosure 100. The enclosure 100 is made of ABS-T (acrylonitrile-butadiene-styrene; available from Wong's Electronics Co. LTD., Wongs Industrial Centre, 180 Wai Yip Street, Kwun Tong, Kowloon, Hong Kong, as material ABS, grade T). The input device 18 accepts template overlays 102, each of which overlay comprises a body 104, a tab 106, and an identification pattern 108 at one edge on the bottom. The template overlay 102 is made of a thin material such as coated paper, coated cardboard, or polyester film. One suitable polyester film is manufactured by Du Pont and widely available under Du Pont's "Mylar" trademark. The body 104 has a graphical image inscribed therein or thereon; that is, the graphic design is written, printed, painted, carved, engraved, silkscreened, or otherwise permanently affixed on or in the overlay body 104. The tab 106 extends from the body 104 and is used to grip the template overlay 102. The identification pattern 108 will be described in the text accompanying Figures 2G-2K.

The touchpad 19 has a pad surface 110, which is exposed to allow contact by a finger, stylus 21, or the like. The pad surface has a default template graphical design inscribed in or on the pad surface 110; that is, the default template graphic image is permanently written, printed, painted, carved, engraved, silkscreened, or otherwise affixed on or in the pad surface 110.

As shown in Figure 2A, the following functions can be supported by the default template graphic design



inscribed in or on the pad surface 110: "enter," "exit," "pause," "previous," "next," and arrow keys (up, down, left, and right). In the alternative, "select" can be used instead of "enter" and "cancel" can be used instead of "exit." Again in the alternative, ten rectangular areas can be mapped out--one for each Arabic numeral. Again in the alternative, the letters of the English language can each be mapped to a region of the touchpad. Again in the alternative, a QWERTY keyboard could be mapped onto the pad surface 110. Indeed, virtually any pattern, or combination of patterns and symbols, can be chosen. The default template graphic image should be chosen to be useful to a large number of applications targeted for the system 10.

15 The input device 18 comprises two forms of retainers to secure a template overlay 102 proximate to the pad surface 110: (1) an overhanging lip 112, which comprises three straight lip portions 112a-c that define a generally U-shaped slot 114 and that retain the template overlay 102 on three sides and (2) a pair of ridges 116a, 116b that retain the template overlay 102 on the fourth side. The lip 112, slot 114, and ridges 116a, 116b are shown in more detail in and described in the text accompanying Figures 2C, 2D, and 2E.

25 Also shown in Figure 2A are a handle 118 for carrying the input device 18 and a tubular aperture 120 for storing the stylus 21.

Referring now to Figure 2B a top plan view of the input device 18 with a template overlay 102 in place proximate to the pad surface 110 is shown. As shown in that figure, three sides of the body 104 of the overlay 102 are slipped under the three lip portions 112a-112c. Also shown in that figure are the ridges 116a, 116b retaining the fourth side of the body 104 of the overlay



102, one positioned on either side of the tab 106 of the overlay 104. The overlay 102 is inserted by slipping the left hand and right hand sides of the body 104 of the overlay 102 under the lip portions 112a and 112c and
5 sliding the overlay 102 down until the bottom edge of the body 104 of the overlay 102 is under the other lip portion 112b. Finally the overlay 102 is released and the tab 106 is nested between the ridges 116a, 116b, which retain the overlay 102 at the top side.

10 Figures 2C, 2D, and 2E show the details of the ridges 116a, 116b and the overlay 102. Figure 2D shows the tab 106 extending beyond the ridge 116b. Figure 2E shows the body 104 of the overlay 102 abutting the ridge 116b.

15 The overlay 102 is removed by gripping the tab 106 with thumb and forefinger and raising the body 104 of the overlay 102 above the ridges 116a, 116b, thereby allowing the overlay 102 to slide out from under the U-shaped lip 112 and over the ridges 116a, 116b.

20 Figure 2F shows the slot 114 that retains the overlay 102 on three sides. Also shown in that figure are the touchpad sensor 122, an overlay sensor 124, a cavity 126 for storing a plurality of template overlays 102, and a substantially rigid base 127 made of the same
25 material as the enclosure 100 that provides a resistive force sufficient to allow a touch of the sensor 122 to be detected.

The touchpad sensor 122 is located proximate to said pad surface 110 and is configured in such a manner
30 that pressure on or near the pad surface 110 by the finger, stylus 21, or the like allows the sensor 122 to detect the location of the touch.

The touchpad sensor 102 can be any one of many types, such as impedance-based sensors, acoustic



sensors, and switch closure type sensors. Examples include membrane switch matrixes, e.g., the device disclosed in U.S. Patent No. 4,736,190 to Florella, and finer resolution switch closure type sensors, e.g., the device disclosed in U.S. Patent No. 4,529,959 to Ito et al. One suitable sensor 102 can be purchased from Wong's Electronics Co. LTD., Wongs Industrial Centre, 180 Wai Yip Street, Kwun Tong, Kowloon, Hong Kong, as part number PR39983.

10 The sensor 122 generates at least one electrical signal responsive to the stylus 21, finger, or the like touching the pad surface 110 or touching the template overlay 102 proximate to the pad surface 110. For example, switch closure type sensors typically require
15 a number of drivers to sequentially drive the many lines on one axis and a number of receivers to detect which of the lines on the other axis is conducting the signal driven by the drivers. Knowing which driver generated the signal detected by which receiver allows one to
20 determine the location of the touch causing the switch closure.

 The overlay sensor 124 is a sensor that generates an electrical signal corresponding to the identification pattern 108 on the overlay 102. Thus the overlay sensor
25 124 of the touchpad 19 and the identification pattern 108 of the template overlay 102 must correspond both in location and in device technology. A suitable overlay sensor 124 is a bank of six optoelectrical transmitter/receivers each having an angled transmitter and an
30 angled receiver, which are well known in the art and are available from Wong's Electronics Co. LTD, as part number PR39990.

 As shown in Figure 2G the overlay sensor 124 is optically coupled to the identification pattern 108 via



six holes 128a-128f in the enclosure 100. Under each hole 128 is a single optoelectronic transmitter/receiver pair (not shown). In another embodiment (not shown), the six receiver/transmitter pairs of the overlay sensor 124 and the six holes 128a-128f can be divided into two groups of three and positioned one on either side of the touchpad sensor 122. That is, three holes 128a-128c (and their associated receiver/transmitter pair) can be positioned under one lip portion 112a and the other three holes 128d-128f (and their associated receiver/transmitter pairs) can be positioned under another lip portion 112c.

Figures 2H-2K show examples of identification patterns 108. The identification patterns 108 are located on one edge of the template overlay 102. There are six individual marks--one for each individual transmitter/receiver pair of the overlay sensor 124. When the overlay 102 is in place, the identification pattern 108 aligns with the sensor 124. If the alternative embodiment, described above, in which two groups of three holes is used for the sensors, then the identification patterns 108 must likewise be divided into two groups of three and positioned one on either side of the touchpad sensor 122.

Using optoelectrical transmitter/receiver pairs as the sensor 124 allows very simple identification patterns 108 to be designed into the template overlay 102. If the material from which the overlay is made is white, then regions of black ink or paint applied to the back of the overlay can be used as one form of identification pattern and white areas without black ink can be used as the other.

Examples of several different possible combinations of identification patterns are shown in



Figures 2H-2K. Figures 2H through 2K show identification patterns 108 corresponding to binary patterns of 010001_2 , 0111102_2 , 000000_2 , and 111111_2 , respectively. Thus, the identification patterns appear to be a group of light and dark regions spaced along the edge of the template overlay 102. The 000000_2 pattern is shown for illustrative purposes only. In actual use, the all white 000000_2 pattern will probably not be used, because that pattern corresponds to the absence of any template overlay 102, in which case the default template graphic image would be used.

Figure 2L, which is a front elevational view of the input device 18 of the present invention, shows the positioning of the joysticks 20a, 20b one on each side of the touchpad 19. As shown in that figure, the joysticks 20a, 20b each have momentary pushbutton switches 130a, 130b affixed in their respective ends. Figure 2L also shows the rectangular aperture 132 that opens to the cavity 126, which is used to store a plurality of template overlays.

Figure 2M, which is a partial sectional view taken substantially along the plane designated by the line 2M-2M of Figure 2A, shows the details of the joysticks used in the input device of the present invention. The details of Figure 2M are repeated for both joysticks 20a and 20b. Moreover, the details of Figure 2M are 90-degrees rotationally symmetrical; thus, while two of many structures are shown in that figure, actually four of the same structures are used in this particular embodiment. The joystick 20a is affixed to a rod 134, which extends through an aperture 136 into the volume defined by the enclosure 100. The rod 134 terminates in a pivot point 138, which pivots on a switch base 140. The switch base 140 is secured to the enclosure 100 by



four screws 142a-142d to several standoffs 144a-144d, which are physically annexed to the enclosure 100. The aperture 136 is sealed by an annular seal 146, the annulus of which fits snugly around the rod 134 and the outer edge of which is physically annexed to the enclosure 100 at the aperture by common methods.

The joystick 20a has a 14-degree freedom of motion about the pivot point; i.e., the rod 134 can move seven degrees from being perfectly perpendicular to the plane defined by the switch base 140 in virtually all directions. The rod 134 has four switch actuator arms 150a-150d physically annexed thereto. The actuator arms 148 are located proximate to four rubber dome momentary pushbutton switches 150a-150d, which are physically annexed to the switch base 140. The arms 148 and switches 150 are configured so that when the joystick 20a is displaced from the perpendicular, one or more of the arms 148 cause a closure event of their associated switches 150. Thus, motion of the joystick 20a is detected by closure events of the switches 150. In the alternative, the joysticks 20a, 20b can be implemented by other structures, such as potentiometer-based systems, which are well known in the art.

Referring now to Figure 3, a block diagram of the circuitry within the input device 18 is shown. The input device 18 comprises the touchpad sensor 122, the overlay sensor 124, joystick sensors 200a, 200b, coordinate determining circuitry 202, overlay detection circuitry 204, a 100 millisecond timer 208, and interface circuitry 210, all connected in electrical circuit communication as shown in Figure 3.

The coordinate sensor 122 and overlay sensor 124 are as described above in the text accompanying Figure 2. The coordinate determining circuitry 202 is in



circuit communication with the coordinate sensor 122, the interface circuitry 210, and the 100 millisecond timer 208. The coordinate determining circuitry 202 is configured to accept the electrical signals 203 from the coordinate sensor 122 and determine the X-axis and Y-axis values corresponding to the location of the touch by the finger, stylus 21, or the like. For example, if the coordinate sensor 122 is a switch-type sensor, then the coordinate determining circuitry 202 will comprise drivers and receivers to determine which switch is closed, as are well known in the art, and logic to translate the location of that switch to a meaningful value relative to the pad surface 110.

The overlay detection circuitry 204 is in circuit communication with the overlay sensor 124 and the interface circuitry 210. The overlay detection circuitry 204 accepts the electrical signal 205 from the overlay sensor 124 and generates a message corresponding to the identification pattern 108, or lack thereof, which is detected as the 000000₂, as described above.

The direction determining circuitry 206 is in circuit communication with the joystick sensors 200a, 200b and the interface circuitry 210. The joystick sensors 200a, 200b comprise four rubber dome switches 150a-150d and the two joystick switches 130a, 130b, as described above. The direction determining circuitry generates a message based on closure events of these switches.

The 100 millisecond timer 208 is in electrical circuit communication with the coordinate determining circuitry 202. The timer 208 repeatedly determines the expiration of a 100 millisecond period of time and generates a signal 209 that indicates the expiration of the period. The coordinate determining circuitry 202



uses the signal 209 to detect a change in the touch location of the finger, stylus 21, or the like between expirations of the 100 millisecond periods detected by the timer 116.

5 The interface circuitry 210 is in circuit communication with the coordinate determining circuitry 202, the overlay detect circuitry 204, the data processing unit 12 (via the serial data line 22), and other input devices, if any, via the serial data line
10 extension 23. The interface circuitry 210 accepts the coordinate values determined by the coordinate determining circuitry 202, the overlay message generated by the overlay detection circuitry 204, and the messages generated by the direction determining circuitry 206 and
15 transmits any such information to the data processing unit 12 via the serial data link 22.

All input devices are daisy chained to the processing unit 12. Thus, the interface circuitry must pass any packets from other input devices on to the CPU
20 30. As will be explained more fully below, each input device connected to the processing unit 12 has a unique device number. The device closest to the processing unit 12 has a device number of 0, and the farther away from the processing unit 12 a device is, the higher its
25 device number is. However, the input devices are not aware of their own or other devices' device numbers. Thus, each device must add one to the device number of any data packet passed from other input devices of the same type. Any input device in the chain with a device
30 number greater than fifteen is ignored.

For example, assume that three input devices of the same type α , β , and γ are connected to the processing unit 12 as follows: α is connected to the processing unit 12, β is connected to α , and γ is



connected to β . Therefore, α has a device number of 0, β has a device number of 1, and γ has a device number of 2. The other devices are not aware of their own or other device numbers. Each device sends its own data
5 packets with a device number of 0.

When α passes a data packet to the processing unit 12, the default device number of 0 is correct, because α is closest to the processing unit 12. However, β and γ also send data packets with a device number of 0. To
10 remedy the situation, each device adds one to the device number of packets passed on. Thus, when β passes a data packet from γ to α , β adds one to the device number, thereby giving the packet from γ a device number of 1. Likewise, when α passes the γ data packet to the
15 processing unit 12, α adds one to the device number, thereby giving the packet from γ a correct device number of 2. Thus, each device in the chain adds one to the device number of each data packet from devices of the same type passed on to the next device.

20 Therefore, in addition to passing on data packets received from other input devices (if any), the interface circuitry 210 adds one to the device number in any data packets from devices of the same type received via the serial data line extension 23. The interface
25 circuitry 210 passes the data packets with modified and unmodified device numbers to the data processing unit 12.

Using the system 10 with the input device 18 of the present invention is very straightforward. The
30 input devices send data packets to the data processing unit 12 via the serial link 22. As mentioned above, the input devices interface to the CPU 30 via the I/O coprocessor 36. Each input device is daisy chained to the next input device. The I/O coprocessor 36 receives



the data packets and stores them in a first-in-first-out (FIFO) manner.

Every 50 msec "tick" the I/O coprocessor 36 interrupts the CPU 30. In response, the CPU accesses the single byte at I/O port AS0 of the coprocessor 36 to determine the number of ticks since the last access by the CPU and the number of device messages to be transferred, as explained above. The ten types of device messages are shown in the table below.

Device Type	Byte 0 (Count)	Byte 1 (Device ID)		Byte 2	Byte 3	Byte 4
		(Bits 4-7)	(Bits 0-3)			
Keyboard (PS/2)	2	0	0	Scan Code	N/A	N/A
Mouse (PS/2)	4	1	0	Mouse Byte 1 (Buttons)	Mouse Byte 2 (X Data)	Mouse Byte 3 (Y Data)
Switch Closure	Variable 1-255	Device Number in Chain	1	Button States 0: Open 1: Closed	Button States (Optional)	Button States (Optional)
Joystick (Digital)	2	Device Number in Chain	2	Switch Closure /Open Code	N/A	N/A
Coordinate (Relative)	4	Device Number in Chain	3	Button States	Delta X	Delta Y
Coordinate (Absolute)	4	Device Number in Chain	4	Button States	X Coord.	Y Coord.
Touchpad Overlay Message	2	Device Number in Chain	5	Overlay Code (0-63)	N/A	N/A
Action Message	Variable 1-255	Device Number in Chain	6	Action Button Data	(Optional)	(Optional)



5	System Pass-through	Variable 1-255	Device Number in Chain	14	Byte 0	Byte 1 (Optional)	Byte 2 (Optional)
	Initiali- zation Message	Variable 1-255	Device Number in Chain	15	Device Type (ID)	Mfg Code Byte 0	Mfg Code Byte 1 (Optional)

Table: Input Device Message Structures

As seen in the table, the message structures are of different length and have structures closely related to the input devices to which they correspond. The device messages in the table are the same for the data sent to the I/O coprocessor from the individual I/O devices as the data sent to the CPU by the I/O coprocessor. In addition to the structures shown above, each message from an I/O device to the I/O coprocessor has a checksum to ensure uncorrupted data is sent from the input device 18 to the processor unit 12. The checksum is a standard modulo 256 checksum in which the checksum value is the value needed to make the sum of all the bytes zero (ignoring any carry during the summation). The I/O coprocessor strips off the checksums before sending the data to the CPU. Therefore, the stream of bytes read by the CPU is virtually identical to the stream of bytes received by the I/O coprocessor, with the following exceptions: (1) the first byte read by the CPU is the special byte containing the number of ticks and the number of I/O device messages and (2) the checksums are missing.

The PS/2 mouse and keyboard devices are supported as device type 0. The keyboard has a chain number of 0 and the mouse has a chain number of 1. These devices are supported by the I/O coprocessor using the existing PS/2 protocol via the serial data link 22.



This device type 1 is intended for devices with multiple buttons. Up to 255 bytes (8 buttons per byte) or 2040 buttons can be input to the system using this message type. Open buttons are sent as a logical ZERO while closed buttons are sent as a logical ONE. This is a variable length message.

Digital joysticks, such as joysticks 20a, 20b are supported as device type 2. There are two joysticks associated with each touchpad 19. Each joystick has a unique chain number. Each left joystick is odd (1, 3, 5, 7, 9, etc.) and each right joystick is even (0, 2, 4, 6, etc.). Each joystick is reported independently. The message is a fixed length message. Recall that digital joysticks sensors comprise a number of switches 150a-150d. The message is a byte representing up to eight switches, which include the movement sensor switches 150a-150d and data input switches, such as switch 130a. The individual bits of the message byte for this type represent: up switch (MSB), down switch, left switch, right switch, switch #1, switch #2, switch #3, and switch #4 (LSB). The joysticks 20a, 20b included with the touchpad 19 only have one button 130, which corresponds to switch #1 above. The other three buttons are always reported as zero.

Coordinate devices such as mice and trackballs are reported as device type 3. The first byte following the ID is to report any button information for the device. Up to 8 buttons can be reported. The next byte is a delta X value followed by a delta Y value. The delta X and Y values are based on the last reported position of the device. The application programs must convert these values to absolute coordinates, if necessary. The maximum movement is 255. If the actual movement exceeds



255, then two or more messages will be sent. This is a fixed length message.

The touchpad 19 is supported as device type 4. Other devices in this device type include analog joysticks. The first byte following the ID is used to report button information. The next byte is used to report the absolute X position. The absolute Y position is next in sequence. The absolute X and Y values are each 1 byte and are limited to a range of 0-255. This is a fixed length message.

Touchpad overlays 102 are reported as device type 5. Touchpad overlays are sensed using the 6-bit sensor 124 in the touchpad. When an overlay change is sensed by the touchpad, a message is generated. All overlay codes are application-dependent and the application program must recognize the codes of each overlay. This message is a fixed length message.

The action message is used to define a common set of predefined device-independent functions that can be generated by multiple device types in different ways but are used and interpreted by the system and application programs in the same way. Action messages are reported as device type 6 using a variable length message. In this particular embodiment, three device-independent functions are defined and associated with the lower three bits of this byte: START (start an activity or process), PAUSE (pause an activity or process), and SELECT (select one of multiple events or actions), respectively. The bits are set to report these functions. All other bits are reserved for future use and are reported as zero to the CPU.

The system pass-through message type is used to handle any device types not applicable to any previously defined device types. Message type 14 is used. This is



a variable length message. Definition of the data is device-dependent and is application specific. Each application must translate this type of message into the required functionality.

5 The first message from each device is device type 15. This is used to tell the system that a device will send input messages. This message also defines the future device type that will be used to report input. This is a variable length message.

10 On system power up and 50 ms intervals, the I/O coprocessor scans the cartridge and expansion sense lines to determine the configuration and alert the system and sends a configuration byte to the CPU. This is the first byte the CPU receives from the I/O
15 coprocessor on power up. The I/O coprocessor will only generate a module configuration interrupt when a change is sensed; a change in cartridge status causes a system reset, thereby causing the I/O coprocessor to send another configuration byte to the CPU. The appropriate
20 bits set in the byte sent are set to indicate the presence of the associated item: bit 0 corresponds to cartridge 1, bit 1 corresponds to cartridge 2, and bit 2 corresponds to the optional CD drive. The other bits are set to ZERO.

25 In addition, the CPU can transmit data to the I/O devices via the serial link 22 by writing the information to the I/O coprocessor 36. Data bytes are written to I/O port AS0 with each byte prefaced by the byte 03H. The I/O coprocessor writes these bytes to the
30 I/O devices. This capability is used to send data to, for example, a printer (not shown).

Interfacing to the input device having two joysticks and a touchpad with an inscribed default template graphic image of the present invention is also



straightforward. An interrupt handler executing on the CPU 30 from the system BIOS receives data from the input devices via the I/O coprocessor 36. The interrupt handler merely places any transmissions from the I/O coprocessor 36 into memory 33. Application programs executing on the CPU 30 poll the operating system BIOS periodically via a software interrupt to determine if any inputs were received. If so, they are communicated to the application programs by the operating system in response to the software interrupt.

The application programs monitor the current template. If the default template graphic image is detected (the overlay sensor 124 will detect all transmission-type identification patterns 108, i.e., 000000₂), then the application program operates responsive to the default template. If, on the other hand, a template overlay 102 is detected, then the application program operates responsive to that particular template overlay 102.

While the present invention has been illustrated by the description of embodiments thereof, and while the embodiments have been described in considerable detail, it is not intended to restrict or in any way limit the scope of the appended claims to such detail. Additional advantages and modifications will readily appear to those skilled in the art. For example, a QWERTY or other type of keyboard could be inscribed in or on the touchpad surface 100. As another example, the coordinate determining circuitry 202, overlay detection circuitry 204, joystick circuitry 206, 100 millisecond timer 208, and interface circuitry 210 can all be implemented in a single microcontroller. Therefore, the invention in its broader aspects is not limited to the specific details, representative apparatus and method,

and illustrative examples shown and described. Accordingly, departures may be made from such details without departing from the spirit or scope of the applicant's general inventive concept.





We claim:

- 1 1. An input device comprising:
 - 2 (a) a pad surface exposed to allow contact by a
 - 3 finger, stylus, or the like;
 - 4 (b) a retainer for removably securing a template
 - 5 overlay proximate to said pad surface; and
 - 6 (c) a touchpad proximate to said pad surface for
 - 7 generating an electrical signal responsive to a stylus,
 - 8 finger, or the like touching said pad surface or
 - 9 touching a template overlay proximate to said pad
 - 10 surface and said touchpad configured such that said
 - 11 electrical signal corresponds to the coordinates of the
 - 12 location touched;
 - 13 wherein said pad surface has an inscribed default
 - 14 template graphic image associated therewith.

- 1 2. A touchpad comprising:
 - 2 (a) a pad surface exposed to allow contact by a
 - 3 finger, stylus, or the like;
 - 4 (b) a retainer for removably securing a template
 - 5 overlay proximate to said pad surface;
 - 6 (c) a coordinate sensor proximate to said pad
 - 7 surface for generating at least one electrical signal
 - 8 responsive to a stylus, finger, or the like touching
 - 9 said pad surface or touching a template overlay
 - 10 proximate to said pad surface and said coordinate sensor
 - 11 configured such that said at least one electrical signal
 - 12 corresponds to the coordinates of the location touched;
 - 13 (d) a rigid base proximate to said pad surface;
 - 14 (e) coordinate determining circuitry in circuit
 - 15 communication with said coordinate sensor for
 - 16 determining from said at least one electrical signal the
 - 17 coordinates of the stylus, finger, or the like touching





18 said pad surface or touching a template overlay
19 proximate to said pad surface; and
20 (f) interface circuitry in circuit communication
21 with said coordinate determining circuitry for
22 communicating the determined coordinates to devices
23 external to said touchpad;
24 wherein said pad surface has an inscribed default
25 template graphic image associated therewith.

1 3. A computer system comprising:
2 (a) a central processing unit (CPU);
3 (b) a memory circuit in circuit communication with
4 said CPU;
5 (c) a video circuit in circuit communication with
6 said CPU and said memory for generating an electrical
7 signal corresponding to a visual image to be displayed
8 on a video display device;
9 (d) a peripheral interface circuit in circuit
10 communication with said CPU for interfacing signals from
11 external devices to said CPU;
12 (e) a pad surface exposed to allow contact by a
13 finger, stylus, or the like;
14 (f) a retainer for removably securing a template
15 overlay proximate to said pad surface;
16 (g) a coordinate sensor proximate to said pad
17 surface for generating at least one electrical signal
18 responsive to a stylus, finger, or the like touching
19 said pad surface or touching a template overlay
20 proximate to said pad surface and said coordinate sensor
21 configured such that said at least one electrical signal
22 corresponds to the coordinates of the location touched;
23 (h) a rigid base proximate to said pad surface;
24 (i) coordinate determining circuitry in circuit
25 communication with said coordinate sensor for





26 determining the coordinates of the stylus, finger, or
27 the like touching said pad surface or touching a
28 template overlay proximate to said pad surface; and

29 (j) interface circuitry in circuit communication
30 with said coordinate determining circuitry and said
31 peripheral interface circuit for communicating the
32 determined coordinates thereto;

33 wherein said pad surface has an inscribed default
34 template graphic image associated therewith.

1 4. The computer system of claim 3 further comprising
2 a software module for execution on said CPU configured
3 to communicate determined coordinates to application
4 programs executing on said CPU.

1 5. The computer system of claim 3 further comprising:

2 (a) a template overlay sensor for detecting the
3 presence of identification structures associated with a
4 template overlay and for detecting the absence of any
5 identification structures;

6 (b) overlay detection circuitry in circuit
7 communication with said template overlay sensor and said
8 interface circuitry for generating an electrical signal
9 corresponding to identification structures responsive to
10 identification structures being detected by said
11 template overlay sensor.

1 6. An input device comprising:

2 (a) a touchpad; and

3 (b) at least two joysticks operatively associated
4 with said touchpad.

1 7. The input device of claim 6 wherein said joysticks
2 are positioned one to each side of said touchpad.





1 8. An input device comprising:

2 (a) an enclosure;

3 (b) a touchpad physically annexed to said
4 enclosure and exposed to allow contact by a finger,
5 stylus, or the like; and

6 (c) two joysticks physically annexed to said
7 enclosure and positioned one to each side of said
8 touchpad.

1 9. An input device for use with a computer system
2 having a central processing unit (CPU) enclosed in a
3 central enclosure comprising:

4 (a) at least two joysticks having joystick
5 circuitry associated therewith, which is configured to
6 generate joystick signals responsive to movements of
7 said joysticks;

8 (b) a touchpad having a pad surface and configured
9 to generate touch location signals responsive to touches
10 of said pad surface;

11 (c) interface circuitry in circuit communication
12 with said joystick circuitry and said touchpad and
13 configured to communicate to the CPU data packets
14 corresponding to movements of said joysticks and further
15 configured to communicate to the CPU data packets
16 corresponding to the locations of touches of said pad
17 surface by a finger, stylus, or the like.

1 10. The input device of claim 9 further comprising an
2 input device enclosure and wherein said joysticks and
3 said touchpad are physically annexed to said input
4 device enclosure.

1 11. The input device of claim 9 further comprising an
2 input device enclosure and wherein said joysticks and





3 said touchpad are physically annexed to said input
4 device enclosure and configured such that said touchpad
5 is centrally located on one face of said input device
6 enclosure and said joysticks are positioned on opposite
7 sides of said touchpad.

1 12. The input device of claim 9 further comprising an
2 input device enclosure and wherein said joysticks and
3 said touchpad are physically annexed to said input
4 device enclosure, said touchpad has a generally
5 rectangular shape having a longer pair of sides and a
6 shorter pair of sides, said touchpad is centrally
7 located on one face of said input device enclosure, and
8 said joysticks are positioned adjacent to the shorter
9 sides of said touchpad.

1 13. A computer system comprising:

2 (a) a CPU enclosed in a central enclosure;

3 (b) first and second joysticks in circuit
4 communication with said CPU; and

5 (c) a touchpad in circuit communication with said
6 CPU.

1 14. The computer system of claim 13 further comprising
2 an input device enclosure and wherein said touchpad and
3 said first and second joysticks are physically annexed
4 to said input device enclosure.

1 15. The input device of claim 13 further comprising an
2 input device enclosure and wherein said first and second
3 joysticks and said touchpad are physically annexed to
4 said input device enclosure and configured such that
5 said touchpad is centrally located on one face of said





6 input device enclosure and said joysticks are positioned
7 on opposite sides of said touchpad.

1 16. The input device of claim 13 further comprising an
2 input device enclosure and wherein said first and second
3 joysticks and said touchpad are physically annexed to
4 said input device enclosure, said touchpad has a
5 generally rectangular shape having a longer pair of
6 sides and a shorter pair of sides, said touchpad is
7 centrally located on one face of said input device
8 enclosure, and said joysticks are positioned adjacent to
9 the shorter sides of said touchpad.

This Sheet Has Been Replaced

