

METHOD OF FORMING A BARRIER LAYER IN A CONTACT STRUCTURE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains to a method of forming a titanium-comprising or a tantalum-comprising barrier/wetting layer structure. This structure is useful when a series of semiconductor substrates is to be fabricated in a process chamber, as it enables a consistently high degree of $\langle 111 \rangle$ crystal orientation in an aluminum interconnect layer or a copper interconnect layer deposited over such a barrier/wetting layer structure, throughout the processing of the series of substrates.

2. Brief Description of the Background Art

Titanium nitride layers have been used in semiconductor device structures as barrier layers for preventing the interdiffusion of adjacent layers of materials such as aluminum and silicon, for example. However, the crystal orientation of aluminum deposited over the surface of the titanium nitride barrier layer is typically polycrystalline, and polycrystalline aluminum has poor electromigration resistance.

In the formation of integrated circuit interconnect structures, such as a Ti/TiN/TiN_x/Al stack, electromigration of aluminum atoms within the aluminum layer becomes a problem if the aluminum layer is not formed with a high degree of $\langle 111 \rangle$ crystal orientation. Electromigration of the aluminum atoms can result in open circuits within the integrated circuit structure, and therefore, such electromigration must be inhibited or eliminated. Electromigration of aluminum atoms can occur within filled vias as well, impairing the conductivity of the contacts.

1 U.S. Patent No. 4,944,961 to Lu et al., issued July 31, 1990, describes a process
2 for partially ionized beam deposition of metals or metal alloys on substrates, such as
3 semiconductor wafers. Metal vaporized from a crucible is partially ionized at the
4 crucible exit, and the ionized vapor is drawn to the substrate by an imposed bias.
5 Control of substrate temperature is said to allow non-conformal coverage of stepped
6 surfaces such as trenches or vias. When higher temperatures are used, stepped surfaces
7 are planarized. The examples given are for aluminum deposition, where the non-
8 conformal deposition is carried out with substrate temperatures ranging between about
9 150°C and about 200°C, and the planarized deposition is carried out with substrate
10 temperatures ranging between about 250°C and about 350°C.

11 S. M. Rossnagel and J. Hopwood describe a technique of combining conventional
12 magnetron sputtering with a high density, inductively coupled RF plasma in the region
13 between the sputtering cathode and the substrate in their 1993 article titled "Metal ion
14 deposition from ionized magnetron sputtering discharge", published in the *J. Vac. Sci.*
15 *Technol. B*. Vol. 12, No. 1, Jan/Feb 1994. One of the examples given is for titanium
16 nitride film deposition using reactive sputtering, where a titanium cathode is used in
17 combination with a plasma formed from a combination of argon and nitrogen gases.

18 U.S. Patent No. 5,262,361 to Cho et al., issued November 16, 1993, describes a
19 method for forming single crystal aluminum films on the surface of a substrate such as
20 silicon (111). The object is to increase the amount of the aluminum (111) crystal
21 orientation, to improve the electromigration resistance of the aluminum. Electrically
22 neutral aluminum is deposited by a vacuum evaporation technique upon a silicon wafer
23 surface at a temperature ranging between about 300°C and about 400°C.

1 U.S. Patent No. 5,543,357 to Yamada et al., issued August 6, 1996, describes a
2 process for manufacturing a semiconductor device wherein a titanium film is used as an
3 under film for an aluminum alloy film to prevent the device characteristics of the
4 aluminum alloy film from deteriorating. The thickness of the titanium film is set to 10 %
5 or less of the thickness of the aluminum alloy film and at most 25 nm. In the case of the
6 aluminum alloy film containing no silicon, the titanium film is set to 5% of less of the
7 thickness of the aluminum alloy film. The aluminum film is formed at a substrate
8 temperature of 200 °C or less by a sputtering process, and when the aluminum film or an
9 aluminum alloy film is to fill a via hole, the substrate is heated to fluidize the aluminum.
10 The pressure during the aluminum film formation and during the fluidization is lower
11 than 10^{-7} Torr. A titanium nitride barrier layer may be applied on an interlayered
12 insulating film (or over a titanium layer which has been applied to the insulating film),
13 followed by formation of a titanium film over the titanium nitride film, and finally by
14 formation of the aluminum film over the titanium film. After formation of the titanium
15 nitride barrier layer, the barrier layer is heated to a temperature of about 600°C to 700°C
16 in a nitrogen atmosphere using a halogen lamp so that any titanium which is not nitrided
17 will become nitrided. The titanium nitride barrier layer is said to be a poor barrier layer
18 if un-nitrided titanium is present within the layer.

19 U.S. Patent No. 5,571,752 to Chen et al., issued November 5, 1996, discloses a
20 method for patterning a submicron semiconductor layer of an integrated circuit. In one
21 embodiment, titanium or titanium nitride having a thickness of between approximately
22 300 and 2000 Å is formed by sputter deposition to reach the bottom of a contact opening.
23 The barrier layer may be annealed to form a silicide in the bottom of the opening. A
24 conformal conductive layer of a refractory metal or refractory metal silicide is formed
25 over the titanium or titanium nitride using chemical vapor deposition (CVD). Finally, a
26 second conductive layer, typically aluminum is applied over the surface of the conformal

1 conductive layer. The aluminum is sputtered on, preferably at a temperature ranging
2 between approximately 100°C and 400°C. This method is said to make possible the
3 filling of contact openings having smaller device geometry design requirements by
4 avoiding the formation of fairly large grain sizes in the aluminum film.

5 U.S. Patent Application, Serial No. 08/753,251 of Ngan et al., filed November
6 21, 1996, describes a method for producing a titanium nitride-comprising barrier layer on
7 the surface of a contact via. For certain contact geometries, when the reactor pressure is
8 reduced during formation of the titanium nitride-comprising barrier layer, the thickness
9 of the barrier layer on the sidewalls of the via increases. This enables an aluminum fill to
10 travel along the sidewalls of the via more easily, resulting in a better fill of the via. In
11 particular, the titanium nitride comprising barrier layer needs to be of a minimum
12 thickness and to have a minimum titanium content so that the barrier layer can react
13 slightly with the Aluminum, to draw the aluminum along the sidewalls of the via.

14 U.S. Patent Application, Serial No. 08/511,825 of Xu et al., filed August 7, 1995,
15 assigned to the Assignee of the present invention, and hereby incorporated by reference
16 in its entirety, describes a method of forming a titanium nitride-comprising barrier layer
17 which acts as a carrier layer. The carrier layer enables the filling of apertures such as
18 vias, holes or trenches of high aspect ratio and the planarization of a conductive film
19 deposited over the carrier layer at reduced temperatures compared to prior art methods.

20 A "traditionally sputtered" titanium nitride-comprising film or layer is deposited
21 on a substrate by contacting a titanium target with a plasma created from an inert gas
22 such as argon in combination with nitrogen gas. A portion of the titanium sputtered from
23 the target reacts with nitrogen gas which has been activated by the plasma to produce
24 titanium nitride, and the gas phase mixture contacts the substrate to form a layer on the
25 substrate. Although such a traditionally sputtered titanium nitride-comprising layer can
26 act as a wetting layer for hot aluminum fill of contact vias, good fill of the via generally

1 is not achieved at substrate surface temperature of less than about 500°C. To provide for
2 aluminum fill at a lower temperature, Xu et al. (as described in U.S. Patent Application,
3 Serial No. 08/511,825), developed a technique for creating a titanium nitride-comprising
4 barrier layer which can act as a smooth carrier layer, enabling aluminum to flow over the
5 barrier layer surface at lower temperatures (at temperatures as low as about 350°C, for
6 example). A typical barrier layer described by Xu et al., is a combination of three layers
7 including a first layer of titanium (Ti) deposited over the surface of the via; a second
8 layer of titanium nitride (TiN) is deposited over the surface of the first titanium layer;
9 finally a layer of TiN_x is deposited over the TiN second layer. The three layers are
10 deposited using Ion Metal Plasma (IMP) techniques which are described subsequently
11 herein. Typically, the first layer of titanium is approximately 100 Å to 200 Å thick; the
12 second layer of TiN is about 800 Å thick; and the third layer of TiN_x is about 60 Å thick.
13 Although a good fill of contact vias having 0.25 μ diameter through holes having an
14 aspect ratio of about 5 was achieved, the crystal orientation of the aluminum was low in
15 <111> crystal orientation content, resulting in poor electromigration (EM) performance
16 for the aluminum interconnect. It was desired to increase the aluminum <111> crystal
17 orientation content for purposes of improving the EM performance.

18 U.S. Patent Application, Serial No. 08/825,216 of Ngan et al., filed March 27,
19 1997, discloses various process techniques which can be used to control the crystal
20 orientation of a titanium nitride barrier layer as it is deposited.

21 U.S. Patent Application, Serial No. 08/824,911 of Ngan et al., filed March 27,
22 1997, discloses improved Ti/TiN/TiN_x barrier/wetting layer structures which enable the
23 aluminum filling of high aspect vias while providing an aluminum fill exhibiting a high
24 degree of aluminum <111> crystal orientation. In particular, an improved Ti/TiN/TiN_x
25 barrier layer deposited using IMP techniques can be obtained by increasing the thickness
26 of the first layer of Ti to range from greater than about 100 Å to about 500 Å (the feature

1 geometry controls the upper thickness limit); by decreasing the thickness of the TiN
2 second layer to range from greater than about 100 Å to less than about 800 Å (preferably
3 less than about 600 Å); and, by controlling the application of the TiN_x third layer to
4 provide a Ti content ranging from about 50 atomic percent titanium (stoichiometric) to
5 about 100 atomic percent titanium. Preferably the TiN_x third layer is formed at the end
6 of the deposition of the TiN second layer and exhibits a Ti content gradient which begins
7 at a stoichiometric, 50 atomic percent, Ti content and ends at a Ti content of about 100
8 atomic percent. The thickness of the TiN_x third layer preferably ranges from about 15 Å
9 to about 500 Å. The improved Ti/TiN/TiN_x barrier layer enables the deposit of an
10 aluminum interconnect an aluminum via fill where the aluminum exhibits a high <111>
11 crystallographic content. U.S. Patent Application, Serial No. 08/824,911 is hereby
12 incorporated herein by reference, in its entirety.

13 Subsequent to the filing of U.S. Patent Application No. 08/824,911, we
14 discovered that in a production simulation, with a cassette containing a large quantity of
15 semiconductor wafers processed in series in a given process chamber, there were
16 unknown factors present at the beginning of processing which affected the <111> crystal
17 orientation of the aluminum layer. Although the method provided in U.S. Patent
18 Application No. 08/824,911 enables the deposit of a high <111> crystallographic
19 aluminum content, to ensure a consistently high aluminum <111> content throughout the
20 processing of a large number of semiconductor substrates, it is necessary to either
21 eliminate the unknown factors affecting the crystalline structure or to find a way to
22 compensate for them.

SUMMARY OF THE INVENTION

The crystal orientation content of a metallic interconnect layer, such as the $\langle 111 \rangle$ crystal orientation content of an aluminum or copper interconnect layer, can be maintained at a consistently high value during the processing of an entire series of semiconductor substrates in a given process chamber. To provide the stable and consistent crystal orientation content for the metallic interconnect layer, it is necessary that the barrier layer structure underlying the metallic interconnect layer have a consistent crystal orientation. This means the barrier layer structure crystal orientation content must remain consistent throughout the processing of the entire series of substrates in a given process chamber. We have determined that to ensure the consistent crystal orientation content of the barrier layer structure, it is necessary to form the first layer of the barrier layer structure to have a minimal thickness of at least about 150 Å, to compensate for irregularities in the crystal orientation which may be present during the initial deposition of this layer.

As an alternative to increasing the thickness of the first layer of the barrier layer structure, this first layer can be deposited at lower process chamber pressures, so that harmful irregularities in the crystal orientation are eliminated.

By forming the first layer of the barrier layer using one of the alternative means described above, we were able to obtain the desired $\langle 111 \rangle$ crystal orientation content of an aluminum interconnect layer throughout the processing of an entire cassette of at least 25 wafers in a given process chamber.

The above described method has been demonstrated for a Ti/TiN/TiN_x barrier layer and is expected to produce equivalent results for a TiN/TiN_x barrier layer as well. Further, we would expect the method to apply to a tantalum-comprising barrier layer used in combination with an overlying copper interconnect layer. In this latter case, the barrier layer structure, whether it be a Ta layer, a TaN layer, a TaN_x layer, or a

1 combination thereof, should be deposited in the manner described, to ensure a high
2 $\langle 111 \rangle$ crystal orientation content in each of these barrier layers. This will provide for a
3 high $\langle 111 \rangle$ crystal orientation content in the copper layer deposited over the barrier
4 layer.

5 BRIEF DESCRIPTION OF THE DRAWINGS

6 Figure 1 shows a schematic of an ENDURA® semiconductor processing system
7 of the kind available from Applied Materials, Inc. of Santa Clara, California.

8 Figure 2 illustrates a schematic of a conductive contact formed within a high
9 aspect ratio via, and shows, in particular, a Ti/TiN/TiN_x barrier layer of the kind
10 described with reference to U.S. Patent Application, Serial No. 08/824,911.

11 Figure 3 shows the normalized X-ray diffraction (XRD) curve for an aluminum
12 film and for the IMP-deposited TiN barrier layer over which the aluminum film was
13 deposited, as a function of the number of wafers processed in succession in the barrier
14 layer deposition chamber. These curves relate to a barrier layer which was processed
15 outside the method of the present invention.

16 Figure 4 shows the normalized XRD curve for an IMP-deposited TiN barrier
17 layer and for the IMP-deposited Ti layer over which the TiN layer was deposited, as a
18 function of the number of wafers processed in succession in the barrier layer deposition
19 chamber. These curves relate to a barrier layer which was formed using the method of
20 the present invention.

1 Figure 5 shows the normalized XRD curve for an aluminum film and for the
2 IMP-deposited TiN layer on which the aluminum film was deposited, as a function of the
3 number of wafers processed in succession in the barrier layer deposition chamber. These
4 curves relate to a barrier layer which was formed using the method of the present
5 invention.

6 Figure 6 shows the XRD intensity curve for an IMP-deposited Ti layer as a
7 function of the deposition chamber pressure, when the power input to the Ti target is in
8 the range of 3 kW to 5 kW. This curve is for a Ti layer which is 1,000 Å thick.

9 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

10 This disclosure pertains to a method of ensuring that the desired crystal
11 orientation content of a metallic interconnect layer remains consistently high during the
12 processing of an entire series of semiconductor substrates in a given process chamber.
13 To provide the consistent crystal orientation content of the metallic interconnect layer, it
14 is necessary to form the first layer of an underlying barrier layer structure to a minimal
15 thickness of at least 150 Å, to compensate for irregularities in the crystal orientation
16 which may be present during the initial deposition of this layer. In the alternative, this
17 first layer can be less than the minimal thickness specified above if it is deposited at a
18 sufficiently low process chamber pressure.

19 **I. DEFINITIONS**

20 As a preface to the detailed description, it should be noted that, as used in this
21 specification and the appended claims, the singular forms "a", "an", and "the" include
22 plural referents, unless the context clearly dictates otherwise. Thus, for example, the
23 term "a semiconductor" includes a variety of different materials which are known to have

1 the behavioral characteristics of a semiconductor, reference to a "plasma" includes a gas
2 or gas reactants activated by an RF glow discharge, reference to "the contact material"
3 includes aluminum, aluminum alloys, and other conductive materials which have a
4 melting point enabling them to be sputtered over the temperature range described herein.

5 Specific terminology of particular importance to the description of the present
6 invention is defined below.

7 The term "aluminum" includes alloys of aluminum of the kind typically used in
8 the semiconductor industry. Such alloys include aluminum-copper alloys, and
9 aluminum-copper-silicon alloys, for example. The preferred embodiments described
10 herein were for aluminum comprising about 0.5% copper.

11 The term "aspect ratio" refers to the ratio of the height dimension to the width
12 dimension of particular openings into which an electrical contact is to be placed. For
13 example, a via opening which typically extends in a tubular form through multiple layers
14 has a height and a diameter, and the aspect ratio would be the height of the tubular
15 divided by the diameter. The aspect ratio of a trench would be the height of the trench
16 divided by the minimal travel width of the trench at its base.

17 The term "feature" refers to contacts, vias, trenches, and other structures which
18 make up the topography of the substrate surface.

19 The term "ion-deposition sputtered" and the term "ion metal plasma (IMP) refer
20 to sputter deposition, preferably magnetron sputter deposition (where a magnet array is
21 placed behind the target). A high density, inductively coupled RF source is positioned
22 between the sputtering cathode and the substrate support electrode, whereby at least a
23 portion of the sputtered emission is in the form of ions at the time it reaches the substrate
24 surface.

25 The term "normalized" refers to a method by which one or more sets of figures
26 are scaled appropriately in order to describe or explain any relationships between the

1 figures. A common approach, as is used here, is to normalize to "1". This is achieved by
2 selecting the highest value in a data set and then dividing all numbers in the data set by
3 this value. By applying this approach to two or more data sets, a graph can be produced
4 which shows the relative change in values between the data sets.

5 The term "reactive ion deposition" or "reactive ion metal plasma (IMP)" refers to
6 ion-deposition sputtering wherein a reactive gas is supplied during the sputtering to react
7 with the ionized material being sputtered, producing an ion-deposition sputtered
8 compound containing the reactive gas element.

9 The term "traditional sputtering" refers to a method of forming a film layer on a
10 substrate wherein a target is sputtered and the material sputtered from the target passes
11 between the target and the substrate to form a film layer on the substrate, and no means is
12 provided to ionize a substantial portion of the target material sputtered from the target
13 before it reaches the substrate. One apparatus configured to provide traditional
14 sputtering is disclosed in U.S. Patent No. 5,320,728, the disclosure of which is
15 incorporated herein by reference. In such a traditional sputtering configuration, the
16 percentage of target material which is ionized is less than 10%, more typically less than
17 1%, of that sputtered from the target.

18 The term "traditionally sputtered aluminum" refers to aluminum applied using
19 traditional sputtering techniques, where the substrate temperature during application of
20 the aluminum ranges between about 200°C to about 550°C, unless specified otherwise.

21 The term "XRD" (X-ray Diffraction) refers to a technique commonly used to
22 measure crystalline orientation, wherein radiation over particular wavelengths is passed
23 through the material to be characterized, and the diffraction of the radiation, caused by
24 the material through which it passes, is measured. A map is created which shows the
25 diffraction pattern, and the crystal orientation is calculated based on this map.
26

II. AN APPARATUS FOR PRACTICING THE INVENTION

A process system in which the method of the present invention may be carried out is the ENDURA® Integrated Processing System available from Applied Materials, Inc. of Santa Clara, California. This process system 100 is shown in the Figure 1. Of particular interest are individual processing chambers which would be used in the practice of the present invention. Process chamber 102 is used for the IMP deposition of a barrier layer such as a Ti/TiN/TiN_x layer. Process chamber 104 is similar to process chamber 102. Process chamber 106 is used for traditional sputtering of an aluminum layer, and transfer chamber 108 is a process chamber which enables movement of a substrate from one of the surrounding process chambers to another. For example, after deposition of a Ti/TiN/TiN_x barrier layer in process chamber 102, a substrate is moved through transfer chamber 108 to process chamber 106 for sputtering of an overlying aluminum film.

Process chamber 102 is typically is a magnetron chamber which employs a standard sputter magnet (to confine the sputtering plasma, enabling an increased sputtering rate); an inductively coupled RF source positioned between the sputtering cathode and the substrate support electrode, whereby at least a portion of the sputtered emission is in the form of ions at the time it reaches the substrate surface; and a sputtering target cathode to which DC power is applied.

EXAMPLE ONE

To form the Ti/TiN/TiN_x barrier layer structure of the present invention, a titanium target cathode of about 14 inches (35.5 cm) in diameter was used, and a DC power was applied to this cathode over a range from about 4 kW to about 8 kW. The substrate, comprising an 8 inch (20.3 cm) diameter silicon wafer, was placed a distance of about 5.5 inches (14 cm) from the target cathode. A high density, inductively coupled

1 RF plasma was generated in the region between the target cathode and the substrate. The
2 inductively coupled plasma was generated by applying RF power to a coil having at least
3 one turn and preferably from about 1 to 3 turns. The power was applied over a range
4 from about 100 kHz to about 60 MHz (and preferably about 2 MHz) at a wattage ranging
5 from about 0.5 kW to about 6 kW (and preferably ranging from about 1.5 kW to about
6 4 kW). Typically the coil is fabricated from metal tubing which permits water cooling,
7 and has a diameter of about 0.125 inch (0.32 cm). However, the coil can be fabricated
8 from a sheet or ribbon, or other form which provides the desired function.

9 A substrate bias voltage ranging from 0 to about -300 V DC may be applied to
10 the substrate or to the platen on which the substrate sets. When a bias voltage is applied
11 a D.C. substrate self bias is created which attracts ions from the plasma to the substrate.
12

13 III. THE STRUCTURE 14 OF THE Ti/TiN/TiN_x BARRIER LAYER 15

16 The typical barrier layer structure comprises a stack of three layers. In the more
17 preferred embodiment, the first layer (applied directly over an underlying substrate such
18 as silicon or silicon oxide) is ion-deposited titanium (Ti). The second layer, applied over
19 the first layer, is ion-deposited titanium nitride (TiN). The third layer, applied over the
20 second layer, is an ion-deposited layer, TiN_x, where the composition of the layer varies
21 from about 50 atomic % titanium to about 100 atomic % titanium. Preferably the
22 titanium concentration is a gradient beginning with essentially stoichiometric TiN and
23 progressing toward pure Ti.

24 An electrical contact or conductive layer is applied over the barrier layer
25 structure. Although the contact or conductive layer described herein is aluminum
26 containing about 0.5% by weight copper, other conductive materials benefit from use of
27 the smooth barrier layer structure described herein. The <111> crystallographic content

1 of a subsequently applied conductive material can be adjusted using the concepts
2 described herein. The aluminum deposited in the examples which follow was
3 traditionally sputtered aluminum, applied over a temperature range of from about 350°C
4 to about 450°C. Preferably the aluminum is applied at reduced pressures ranging from
5 greater than about 0.5 mT up to about 50 mT, preferably between about 1 mT and
6 30 mT, and more preferably between about 1 mT and 4 mT, depending on the feature to
7 be fabricated.

8 Figure 2 shows a schematic of a trench or via 213 containing a barrier layer
9 structure 200 of the kind which would utilize the method of the present invention. The
10 structure 200 was formed on a semiconductor substrate comprising a silicon base 210
11 having an overlying silicon dioxide layer 211. The via or trench 213 was created by dry
12 etching through the silicon dioxide layer 211 to silicon base 210. Structure 200
13 comprised three layers: Ti/TiN/TiN_x. The first layer of titanium was IMP deposition
14 sputtered upon the surface of both silicon dioxide layer 211 and silicon base 210; a
15 second layer of reactive ion-deposition sputtered titanium nitride layer 214 was deposited
16 overlying first titanium layer 212; and a third ion-deposition sputtered titanium nitride-
17 comprising layer 216 was deposited overlying titanium nitride layer 214. (Upon ion-
18 sputtering of titanium layer 212, a thin layer of titanium silicide 224 is typically formed
19 at the bottom of via 213 upon high temperature annealing). Structure 200 was then filled
20 with a conductive layer 219. The aspect ratio of via or trench 213 was as illustrated by
21 the ratio of dimension 222 to dimension 220, and was approximately 20 : 1, with the
22 dimension of 220 being approximately 0.25 μ .

23 Aluminum was traditionally sputtered upon a structure 200 at a substrate
24 temperature of about 400 °C.

IV. THE METHOD OF APPLICATION OF BARRIER LAYERS AND ALUMINUM

The apparatus in which the preferred embodiments described herein were fabricated was the ENDURA® Integrated Processing System previously described and illustrated in Figure 1.

EXAMPLE TWO:

The description which follows pertains to the fabrication of the Ti/TiN/TiN_x barrier layer described above.

To obtain an ion-deposition sputtering rate of about 700 Å per minute of Ti upon the surface of an 8 inch (20.3 cm) diameter substrate, typically about 2 MHz ($\approx$ 2.5 kW) of RF power was applied to the induction coil while about 4 kW of DC power was applied to the titanium target cathode. No power was applied to the substrate platen electrode. The Ti deposition was carried out at about 30 mT. This pressure corresponded to an argon feed rate of about 65 sccm. The temperature on the substrate surface was about 200°C.

To obtain a reactive ion-deposition sputtering rate for TiN of about 250 Å per minute over the Ti first layer surface, typically about 2 MHz ($\approx$ 2.5 kW) of RF power was applied to the induction coil while about 5 kW of DC power was applied to the titanium target cathode. Again, no power was applied to the substrate platen electrode. The TiN deposition was carried out at about 30 mT. This pressure corresponded to an argon feed rate of about 10 sccm and a nitrogen feed rate of about 70 sccm in the Applied Materials ENDURA® Integrated Process System. The temperature on the substrate surface was about 200°C.

1 To obtain a reactive ion-deposition sputtering rate for TiN_x of about 600 Å per
2 minute upon the TiN second layer surface, the process conditions were set at those
3 specified for the TiN second layer; however, at the beginning of the sputtering of the
4 TiN_x layer, the flow of nitrogen gas to the process chamber was discontinued. Since the
5 titanium target becomes nitrided during the TiN deposition, TiN continues to be
6 produced for a limited time period after the nitrogen gas flow is discontinued. Typically,
7 under the operational conditions specified with reference to the TiN deposition, but with
8 the flow of nitrogen gas to the chamber discontinued, the nitrided portion of the target is
9 sputtered away within 5 to 10 seconds. The thicker the TiN second layer, the longer the
10 time period before the nitrided portion of the target is sputtered away. In this particular
11 instance, the TiN_x layer deposition was carried out for a period ranging from about 30 to
12 about 40 seconds after the flow of nitrogen to the process chamber was discontinued.

13 Subsequently an aluminum layer about 6,000 Å thick was sputtered upon the via
14 surface using traditional sputtering techniques, a substrate temperature of about 400°C,
15 and a pressure of about 2 mT. Complete via fill (with essentially no voids evidenced in
16 the photomicrographs) was achieved for the contact vias using the Ti/TiN/ TiN_x
17 barrier/wetting layer fabricated as described above.

18 EXAMPLE THREE:

19 To obtain an aluminum fill of the via where the crystallographic $\langle 111 \rangle$ content is
20 sufficiently high to prevent electromigration, the crystallographic structure of the
21 underlying Ti/TiN/ TiN_x barrier layer 200 is critical, as the underlying TiN_x $\langle 111 \rangle$ crystal
22 orientation content is mirrored in the overlying aluminum $\langle 111 \rangle$ crystal orientation
23 content.

1 With reference to Figure 3, An IMP-deposited Ti/TiN/TiN_x barrier structure was
2 prepared on a wafer surface, with the upper surface of the barrier layer being TiN_x. An
3 aluminum layer was deposited over the barrier layer structure using traditional sputtering
4 techniques. XRD readings were taken to determine the <111> crystal orientation for the
5 TiN_x layer and the aluminum layer.

6 The three layer Ti/TiN/TiN_x structure from which the data for Figure 3 was
7 obtained was prepared as follows. A first layer of Ti was IMP deposited to a thickness
8 of about 100 Å. The DC power to the Ti sputtering target was about 4 kW; the RF power
9 to the inductively coupled IMP coil was about 2.5 kW; the argon flow rate to the
10 deposition chamber was about 65 sccm; the pressure in the deposition chamber was
11 about 30 mT; and the substrate temperature was about 200°C. No power was applied to
12 the substrate support platen. A second layer of TiN was deposited over the Ti layer by
13 reactive IMP deposition, where the conditions were generally the same as during the IMP
14 deposition of the Ti layer, except that nitrogen was added to the deposition chamber at a
15 flow rate of about 70 sccm, with the argon flow rate being 10 sccm. The thickness of the
16 second layer of reactive ion-deposition sputtered TiN was about 250 Å. Subsequently, a
17 third layer of TiN_x was applied over the TiN layer using IMP deposition. The TiN_x layer
18 was applied using the conditions used during the IMP deposition of the TiN layer, except
19 that nitrogen flow was shut off after the formation of the TiN layer, and the IMP
20 deposition was continued for an additional 40 seconds. (Residual nitrogen in the
21 chamber and on the target surface was incorporated into the TiN_x layer.) The resulting
22 TiN_x layer was approximately 400 Å thick. The composition of the TiN_x layer ranged
23 from 50 atomic % Ti initially to toward about 100 atomic % Ti toward the upper surface
24 of the TiN_x layer. The Aluminum was sputtered over the surface of the TiN_x layer using
25 traditional sputtering, at a temperature of about 400°C and at a pressure of about 2 mT.

We discovered that, during the processing of a cassette of 25 semiconductor wafers, the normalized $\langle 111 \rangle$ crystal orientation content, as represented by curve 304, of the TiN_x layer decreased with each subsequent wafer processed. The normalized XRD intensity reading which is indicative of the $\langle 111 \rangle$ content of the TiN_x layer is shown on scale 302, and the number of wafers processed is shown on scale 306. This decrease in normalized $\langle 111 \rangle$ crystal orientation content was mirrored in the overlying aluminum layer, which showed a decreasing normalized $\langle 111 \rangle$ crystal orientation content, represented by curve 308.

The first 7 wafers were "dummy wafers" processed to condition the process vessel, so no data is provided for these wafers. In fact, had the first seven wafers been used for data collection, curves 304 and 308 would be expected to show a decreasing $\langle 111 \rangle$ crystal orientation content over processing of the first 17 wafers. Obviously, such a decreasing $\langle 111 \rangle$ content cannot be tolerated, as it means that the electromigration of the aluminum is adversely impacted. Further, it means that the product is not consistent and that different performance may be expected for each wafer processed. Even if the $\langle 111 \rangle$ crystal orientation content 310 of the aluminum after stabilization were acceptable, no commercially acceptable process would provide for discarding of 17 of 25 wafers processed. We had to find a method for maintaining the aluminum layer $\langle 111 \rangle$ crystal orientation throughout wafer production.

Figure 4 shows the normalized XRD curves for the Ti first layer and for the TiN layer of a Ti/TiN/ TiN_x barrier layer. The Ti first layer $\langle 002 \rangle$ crystal orientation content, as represented by curve 402, and the TiN second layer $\langle 111 \rangle$ crystal orientation content, as represented by curve 404 increase as the number of wafers processed increases. The normalized crystal orientation XRD intensity reading is shown on scale 406, and the number of wafers processed is shown on scale 408. The improvement in crystal orientation of the Ti first layer is mirrored in the TiN layer. This improvement is an

1 indication that there is a factor in the process chamber which causes irregularities in the
2 crystal orientation of the forming barrier layers which is eliminated as additional
3 processing is carried out in the deposition chamber. No aluminum layer was deposited
4 over the surface of the barrier layer structure, as we wanted to have the clearest XRD
5 possible for the structure.

6 With further reference to Figure 4, the barrier layer structure was deposited
7 under the same conditions as described for the barrier layer with reference to Figure 3,
8 except that the thickness of the first Ti layer was 200 Å thick. Due to the increased
9 thickness (from 100 Å to 200 Å) of the first Ti layer, the normalized XRD intensity
10 reading for the <002> crystal orientation of the first Ti layer is relatively high for the 8th
11 wafer (again, the first 7 wafers were dummy wafers) at about 0.86, as shown on curve
12 402 at 410 and remains high for all 25 wafers processed. This high degree of <002>
13 crystal orientation is mirrored in the overlying TiN layer which exhibits a relatively high
14 <111> crystal orientation for the 8th wafer through the 25th wafer, as well. The TiN
15 layer normalized XRD intensity reading for the <111> crystal orientation is about 0.89
16 for the 8th wafer, as illustrated at point 412 on curve 404. As will be shown
17 subsequently with reference to Figure 5, when the normalized XRD intensity reading for
18 the TiN layer is about 0.89, the aluminum layer (overlying the Ti/TiN/TiN_x barrier layer
19 structure) <111> crystal orientation can be expected to have a normalized XRD intensity
20 reading of about 1.0, indicating a very high <111> crystal orientation content for the
21 aluminum layer.

22 The high and increasing <111> crystal orientation of the TiN layer illustrated
23 graphically by curve 404 in Figure 4 stands in stark contrast with the rapidly decreasing
24 <111> crystal orientation of the TiN layer illustrated by curve 304 in Figure 3. We
25 attribute this unexpected difference in crystal orientation stability to the increase in the
26 thickness of the first Ti layer from 100 Å to 200 Å. In view of this surprising result, we

now believe that there is a minimum thickness which the first Ti layer must have to overcome irregularities in the crystal orientation of that layer caused by the presence of a factor in the deposition chamber (which factor is gradually eliminated as additional wafer processing is carried out in the chamber). We know that a 100 Å first Ti layer thickness is inadequate to overcome the effect of this unidentified species, but that a 200 Å thickness is adequate. Our present data indicates that a minimum first Ti layer thickness of about 150 Å is required to ensure an acceptable and constant <002> crystal orientation content for the first Ti layer.

EXAMPLE FOUR:

We have also discovered that it is possible to obtain a high and constant aluminum <111> crystal orientation content when the first Ti layer thickness is 100 Å if an alternative method is used which provides for the elimination of the factor which causes the crystal orientation irregularities.

By reducing the pressure in the process chamber during the deposition of the first Ti layer, we have apparently been able to effectively eliminate the factor which causes the crystal orientation irregularities.

Figure 5, shows the normalized XRD intensity curve 502 for the <111> crystal orientation content of the TiN layer of a Ti/TiN/TiN_x barrier layer, and the normalized XRD intensity curve 504 for the <111> crystal orientation content of an overlying aluminum layer. The <111> crystal orientation content of the TiN layer was high and remained relatively constant (within testing error) as indicated by a normalized XRD intensity of about 0.94 for each wafer tested, beginning with wafer number 14 and extending through wafer 25, as shown in Curve 502. This behavior was mirrored in the overlying aluminum layer, which also exhibited a high and constant <111> crystal orientation content. This was indicated by a normalized XRD intensity of about 1.0 for

1 each wafer tested, beginning with the 7th wafer (which was the first non-dummy wafer
2 in this instance) and continuing through the 25th wafer, as indicated by curve 504.

3 The thickness of the first Ti layer of the structure for which data is presented in
4 Figure 5 was only 100 Å and the process conditions under which the structure was
5 generated were generally the same as those for the structure for which data is presented
6 in Figure 3, with the exception of process chamber pressure. The process chamber
7 pressure during the deposition of the barrier layer of Figure 5 was only 10 mT compared
8 with a process chamber pressure of 30 mT during the deposition of the barrier layer of
9 Figure 3. (There was a 10 second shorter deposition time after nitrogen cut off for the
10 TiN_x layer of the Figure 5 barrier layer, but this is considered to be insignificant and
11 should not result in an improvement in the overlying aluminum <111> crystal orientation
12 content in any case.) We believe the improvement in the <111> crystal orientation
13 content of the TiN layer illustrated in Figure 5 (and in the overlying aluminum <111>
14 crystal orientation content) is attributable to the elimination of the factor which would
15 otherwise cause irregularities in the first Ti layer crystal orientation as that layer is
16 formed.

17 EXAMPLE FIVE:

18 With reference to barrier layers having a first Ti layer of substantial thickness,
19 200 Å or greater for example, where process pressures of 10 mT or higher are known to
20 be acceptable during deposition of this layer, we have discovered a preferred operational
21 pressure which is dependent upon the DC power to the Ti target. We have discovered
22 that the XRD intensity (indicating the desired <002> crystal orientation) for the Ti layer
23 is unexpectedly lower at 20 mT than it is at 10 or at 30 mT when the DC power to the Ti
24 target is moderately low. The reverse is true when the DC power to the Ti target is
25 higher.

Figure 6 shows the XRD intensity 604 as a function of process chamber pressure 606 for a 1,000 Å thick Ti layer. The Ti layer was deposited at an RF induction coil power of 1 - 2 kW, a DC power to the Ti target of 3 - 5 kW, with no substrate bias power applied, and at a substrate temperature of about 200°C. Curve 602 shows that the <002> crystal orientation content of the Ti layer decreases unexpectedly between the process chamber pressures of 30 mT and 10 mT, when the DC power to the Ti target is 5 kW or less.

The above described preferred embodiments are not intended to limit the scope of the present invention, as one skilled in the art can, in view of the present disclosure expand such embodiments to correspond with the subject matter of the invention claimed below.

CLAIMS



We claim:

1. A method of fabricating a Ti-comprising barrier layer structure on a semiconductor substrate, to enable control of the $\langle 111 \rangle$ crystal orientation content of an aluminum layer subsequently deposited thereover, said method comprising: depositing a first layer of Ti or TiN upon said semiconductor substrate, wherein said first layer of Ti exhibits a $\langle 002 \rangle$ normalized XRD intensity of at least about 0.75, or said first layer of TiN exhibits a $\langle 111 \rangle$ normalized XRD intensity of at least about 0.85, for at least 70 % of said semiconductor structures processed in a continuous series through a barrier layer structure fabrication chamber.
2. The method of Claim 1, wherein the thickness of said first layer of Ti or TiN is at least 150 Å thick.
3. The method of Claim 2, wherein a pressure in said fabrication chamber during the deposition of said first layer of Ti or TiN is less than about 30 mT.
4. The method of Claim 3, wherein said pressure is less than about 20 mT.
5. The method of Claim 4, wherein said pressure is less than about 10 mT.
6. The method of Claim 1, wherein a pressure within said fabrication chamber during the deposition of said first layer of Ti or TiN is less than about 10 mT.

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1 7. A method of fabricating a Ti-comprising barrier layer structure on a semiconductor
2 substrate, to enable control of the $\langle 111 \rangle$ crystal orientation content of an aluminum layer
3 subsequently deposited thereover, wherein a series of substrates is processed within a
4 fabrication chamber, said method comprising: depositing a first layer of Ti-comprising
5 material upon said semiconductor substrate to a thickness of at least about 150 Å.

1 8. The method of Claim 7, wherein said Ti-comprising material is selected from the
2 group consisting of Ti, TiN, and TiN_x.

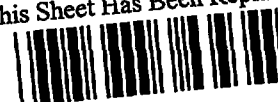
1 9. The method of Claim 8, wherein said first layer is Ti and wherein a second layer of
2 Ti-comprising material is deposited over said Ti layer, wherein said second layer is TiN
3 or TiN_x.

1 10. A method of fabricating a Ti-comprising barrier layer structure on a semiconductor
2 substrate, to enable control of the $\langle 111 \rangle$ crystal orientation content of an aluminum layer
3 subsequently deposited thereover, wherein a series of substrates is processed within a
4 fabrication chamber, said method comprising: depositing a first layer of Ti-comprising
5 material on said semiconductor substrate at a pressure of about 20 mT or less.

1 11. The method of Claim 10, wherein said Ti-comprising material is selected from the
2 group consisting of Ti, TiN, and TiN_x.

1 12. The method of Claim 11, wherein said first layer is Ti and wherein a second layer of
2 Ti-comprising material is deposited over said Ti layer, wherein said second layer is TiN
3 or TiN_x.

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1 13. The method of Claim 10 wherein said deposition pressure for said first layer of
2 Ti-comprising material is less than about 10 mT.

1 14. The method of Claim 11 wherein said deposition pressure for said first layer of
2 Ti-comprising material is less than about 10 mT.

1 15. The method of Claim 12, wherein said deposition pressure for said first layer of
2 Ti-comprising material is less than about 10 mT.

1 16. A method of fabricating a Ta-comprising barrier layer structure on a semiconductor
2 substrate, to enable control of the <111> crystal orientation content of a copper layer
3 subsequently deposited thereover, said method comprising: depositing a first layer of Ta
4 or TaN upon said semiconductor substrate, wherein said first layer of Ta exhibits a
5 <111> normalized XRD intensity of at least about 0.75, or said first layer of TaN
6 exhibits a <111> normalized XRD intensity of at least about 0.85, for at least 70% of
7 said semiconductor structures processed in a continuous series through a barrier layer
8 structure fabrication chamber.

1 17. The method of Claim 16, wherein the thickness of said first layer of Ta or TaN is at
2 least 150 Å thick.

1 18. The method of Claim 17, wherein a pressure in said fabrication chamber during the
2 deposition of said first layer of Ta or TaN is less than about 30 mT.

1 19. The method of Claim 18, wherein said pressure is less than about 20 mT.



1 20. The method of Claim 19, wherein said pressure is less than about 10 mT.

1 21. The method of Claim 16, wherein a pressure within said fabrication chamber during
2 the deposition of said first layer of Ta or TaN is less than about 10 mT.

1 22. A method of fabricating a Ta-comprising barrier layer structure on a semiconductor
2 substrate, to enable control of the $\langle 111 \rangle$ crystal orientation content of a copper layer
3 subsequently deposited thereover, wherein a series of substrates is processed within a
4 fabrication chamber, said method comprising: depositing a first layer of Ta-comprising
5 material upon said semiconductor substrate to a thickness of at least about 150 Å.

1 23. The method of Claim 22, wherein said Ta-comprising material is selected from the
2 group consisting of Ta, TaN, and TaN_x.

1 24. The method of Claim 23, wherein said first layer is Ta and wherein a second layer of
2 Ta-comprising material is deposited over said Ta layer, wherein said second layer is TaN
3 or TaN_x.

1 25. A method of fabricating a Ta-comprising barrier layer structure on a semiconductor
2 substrate, to enable control of the $\langle 111 \rangle$ crystal orientation content of a copper layer
3 subsequently deposited thereover, wherein a series of substrates is processed within a
4 fabrication chamber, said method comprising: depositing a first layer of Ta-comprising
5 material on said semiconductor substrate at a pressure of about 20 mT or less.

1 26. The method of Claim 25, wherein said Ta-comprising material is selected from the
2 group consisting of Ta, TaN, and TaN_x.



1 27. The method of Claim 26, wherein said first layer is Ta and wherein a second layer of
2 Ta-comprising material is deposited over said Ta layer, wherein said second layer is TaN
3 or TaN_x.

1 28. The method of Claim 25 wherein said deposition pressure for said first layer of
2 Ta-comprising material is less than about 10 mT.

1 29. The method of Claim 26 wherein said deposition pressure for said first layer of
2 Ta-comprising material is less than about 10 mT.

1 30. The method of Claim 27, wherein said deposition pressure for said first layer of
2 Ta-comprising material is less than about 10 mT.