CLAIMS

1. An equalizer circuit, comprising a first input buffer circuit, a second input buffer circuit and a selecting and sampling circuit,

wherein the first input buffer circuit and the second input buffer circuit are respectively connected with the selecting and sampling circuit, and a reference voltage used in the first input buffer circuit is different from that used in the second input buffer circuit, and

the selecting and sampling circuit selects to perform data sampling on a data signal outputted by the first input buffer circuit or a data signal outputted by the second input buffer circuit according to data outputted previously by the equalizer circuit, and takes sampled data as data outputted currently by the equalizer circuit;

wherein the selecting and sampling circuit comprises a selecting circuit and a sampling circuit, and the selecting circuit is connected with the sampling circuit,

wherein the selecting circuit is configured to select to input the data signal outputted by the first input buffer circuit or the data signal outputted by the second input buffer circuit into the sampling circuit according to data transmitted by the sampling circuit;

the sampling circuit is configured to perform data sampling on the data signal inputted by the selecting circuit;

wherein the selecting circuit comprises a first selecting circuit and a second selecting circuit, and the sampling circuit comprises a first sampling circuit and a second sampling circuit,

wherein two input terminals of the first selecting circuit are respectively connected with an output terminal of the first input buffer circuit and an output terminal of the second input buffer circuit, and two input terminals of the second selecting circuit are respectively connected with the output terminal of the first input buffer circuit and the output terminal of the second input buffer circuit, and

an output terminal of the first selecting circuit is connected with an input terminal of the first sampling circuit, a control terminal of the first selecting circuit is connected with an output terminal of the second sampling circuit, an output terminal of the second selecting circuit is connected with an input terminal of the second sampling circuit, and a control terminal of the second selecting circuit is connected with an output terminal of the first sampling circuit;

wherein

the first sampling circuit transmits currently-sampled data to the control terminal of the second selecting circuit, and the second selecting circuit selects to input data in the first input buffer circuit or the second input buffer circuit into the second sampling circuit based on the data transmitted by the first sampling circuit, and

the second sampling circuit transmits currently-sampled data to the control terminal of the first selecting circuit, and the first selecting circuit selects to input the data in the first input buffer circuit or the second input buffer circuit into the first sampling circuit based on the data transmitted by the second sampling circuit;

wherein

when the data transmitted by the first sampling circuit to the control terminal of the second selecting circuit is 1, the second selecting circuit selects to input output data of the first input buffer circuit into the second sampling circuit, and when the data transmitted by the first sampling circuit to the control terminal of the second selecting circuit is 0, the second selecting circuit selects to input output data of the second input buffer circuit into the second sampling circuit, and

when the data transmitted by the second sampling circuit to the control terminal of the first selecting circuit is 1, the first selecting circuit selects to input the output data of the first input buffer circuit into the first sampling circuit, and when the data transmitted by the second sampling circuit to the control terminal of the first selecting circuit is 0, the first selecting circuit selects to input the output data of the second input buffer circuit into the first sampling circuit.

2. The equalizer circuit of claim 1, further comprising a double reference voltage generator,

wherein the double reference voltage generator comprises a first reference voltage output terminal and a second reference voltage output terminal, the first reference voltage output terminal is connected with a reference voltage input terminal of the first input buffer circuit, and the second reference voltage output terminal is connected with a reference voltage input terminal of the second input buffer circuit.

3. The equalizer circuit of claim 1, wherein the equalizer circuit further comprises a sampling clock input circuit, and an output terminal of the sampling clock input circuit is respectively connected with sampling clock input terminals of the first sampling circuit and the second sampling circuit;

the sampling clock input circuit is configured to provide a sampling clock signal to the first sampling circuit and the second sampling circuit.

4. The equalizer circuit of claim 3, wherein the first sampling circuit performs data sampling on data inputted by the first selecting circuit by using a rising edge of the sampling clock signal received by the equalizer circuit;

the second sampling circuit performs data sampling on data inputted by the second selecting circuit by using a falling edge of the sampling clock signal received by the equalizer circuit.

5. The equalizer circuit of claim 4, wherein

in response to that the data outputted currently by the equalizer circuit is the data sampled by the first sampling circuit using the rising edge of the sampling clock signal received by the equalizer circuit, data outputted previously by the equalizer circuit is data

sampled by the second sampling circuit when the sampling clock signal received by the equalizer circuit is at a previous falling edge adjacent to the rising edge; and

in response to that the data outputted currently by the equalizer circuit is the data sampled by the second sampling circuit using the falling edge of the sampling clock signal received by the equalizer circuit, data outputted previously by the equalizer circuit is data sampled by the first sampling circuit when the sampling clock signal received by the equalizer circuit is at a previous rising edge adjacent to the falling edge.

6. The equalizer circuit of claim 2, wherein the first input buffer circuit comprises a first comparator circuit and a first delay circuit, the first comparator circuit is connected in series with the first delay circuit, and a reference voltage input terminal of the first comparator circuit is connected with the first reference voltage output terminal,

the second input buffer circuit comprises a second comparator circuit and a second delay circuit, the second comparator circuit is connected in series with the second delay circuit, and a reference voltage input terminal of the second comparator circuit is connected with the second reference voltage output terminal; and

a signal input terminal of the first comparator circuit and a signal input terminal of the second comparator circuit are connected with a same input data signal.

7. The equalizer circuit of claim 6, wherein the first comparator circuit and the second comparator circuit have a same circuit structure.

8. The equalizer circuit of claim 6, wherein the first delay circuit and the second delay circuit have a same circuit structure.

9. The equalizer circuit of any one of claims 1 to 6, wherein the first selecting circuit and the

second selecting circuit have a same circuit structure.

10. The equalizer circuit of any one of claims 1 to 6, wherein the first sampling circuit and the second sampling circuit have a same circuit structure.

11. The equalizer circuit of any one of claims 1 to 6, wherein the reference voltage used in the first input buffer circuit is greater than the reference voltage used in the second input buffer circuit.

12. A memory, comprising an equalizer circuit, wherein the equalizer circuit is the equalizer circuit of any one of claims 1 to 11.