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A SEMICONDUCTOR DEVICE LAYOUT AND CHANNELING IMPLANT

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PROCESS

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Background of Invention

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1) Field of the Invention

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This invention relates generally to fabrication of semiconductor devices particularly to the fabrication of implanted doped regions in a semiconductor device that has a graded junction

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2) Description of the Related Art

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With higher levels of integrated circuits on semiconductor chips and the need for faster transistors in these circuits, the FET transistor must maximize all aspects of semiconductor physics to fabricate transistors in these circuits with faster switching speed.

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As the transistor scaling to smaller dimension, the inventor have found that high V_t NMOS transistor is facing a problem with voltage limitation. Thermal cycle was limited because of the consideration of logic device in the wafer. An aspect of this invention address issue.

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2 In crystalline solids, such as monocrystalline silicon, the atoms which
3 make up the solid are spatially arranged in a periodic fashion. This periodic arrangement of
4 atoms in a crystal is called a lattice. The crystal lattice always contains a volume which is
5 representative of the entire lattice and it is regularly repeated throughout the crystal. The
6 directions in a lattice are expressed as a set of three integers with the same relationship as
7 the components of a vector in that direction. The three vector components are given in
8 multiples of the basic vectors. For example, in cubic lattices, such as silicon which has a
9 diamond crystal lattice, the body diagonal has the components of 1a, 1b, and 1c and this
10 diagonal exist along the [111] direction with the [] brackets being used to denote a specific
11 direction. However, many directions in a crystal are equivalent, depending on the arbitrary
12 choice of orientation of the axes. Such equivalent directions are denoted with < > brackets
13 and, for example, crystal directions in the cubic lattice [100], [010], and [001] are all
14 crystallographically equivalent and are <100> directions. Since these directions will also
15 be on the negative side of the origin, as arbitrarily defined, they also are identified with a
16 (-) over the specific negative integer, such as $[\bar{1}00]$, $[0\bar{1}0]$, and $[00\bar{1}]$ for <100> directions.
17 Unless specifically stated or shown in the following description in this application, a
18 crystal direction includes both positive and negative integers.

19

20 Planes in a crystal also can be determined with a set of three integers h,
21 k, and l. They are used to define a set of parallel planes and each set of three integers in ()
22 parentheses identify a specific plane. As in the case of directions, many planes in a lattice

1 are equivalent and the indices of such equivalent planes are denoted by $\{ \}$ parentheses.
2 For cubic lattices, direction $[k,l,m]$ is perpendicular to a plane with the identical three
3 integers (k,l,m) . Thus, if either a direction or a plane of a cubic lattice is known, its
4 perpendicular counterpart can be quickly determined without calculation. For example, for
5 planes of equivalent symmetry such as $\{100\}$ plane, the equivalent planes are (100) , (010) ,
6 (001) , $(\bar{1}00)$, $(0\bar{1}0)$, and $(00\bar{1})$. Like the crystal direction, the crystal plane in the following
7 description in this application includes both positive and negative integers unless
8 specifically stated otherwise.

9 General terminology is: $()$ for a certain plane; $\{ \}$ for a group of
10 planes; $[]$ for a certain direction; $\langle \rangle$ for a group of directions.

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12 Ion implant processes are important to forming doped regions in
13 substrates. The depth to which an ion becomes implanted is proportional to its kinetic
14 energy. The implanted distribution in an amorphous target is roughly a Gaussian
15 distribution characterized by a mean, known as the range, and a standard deviation, known
16 as the straggle. In a single crystal target, the range and straggle for a given implant may be
17 different than that in amorphous material, due to a phenomena known as *channeling*.
18 Higher ion energy, higher silicon temperature, and the growth of silicon dioxide layers on
19 the silicon all tend to dechannel implants. In any event, range and straggle data for various
20 materials including silicon, silicon dioxide, and photoresist have been determined.

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1 The more relevant technical art in the patent literature is as follows:
2 US 5,970,300(Buynoski) shows an alignment of a FET on a wafer.
3 US 6,566,204(Wang, et al.) teaches the use of mask shadowing and
4 angled implantation in fabricating asymmetrical field-effect transistors.
5 US 6,599,804(Bulucea, et al.)shows a fabrication of field-effect
6 transistor for alleviating short-channel effects.
7 US 4,728,617(Woo, et al.) shows a method of fabricating a MOSFET
8 with graded source and drain regions using a high tilt I/I.
9 However, there is a need for an improved process and device.
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4 **Summary of the Invention**

5 It is an object of an embodiment the present invention to provide a
6 device and method for fabricating a transistor with a graded doped region.

7 It is an object of an embodiment the present invention to provide a high
8 voltage MOS device that has a higher breakdown voltage.

9
10 Some embodiments of the invention comprise implanting ions into said
11 silicon substrate to form doped regions adjacent to said gate. The orientation of the channel
12 region in the Si crystal structure (channel direction $\langle 100 \rangle$) in combination with the large
13 angle tilt and twist implant process that increases channeling (described below) produces
14 doped regions that have a more graded (gradual) junction.

15 With the embodiment's (a) transistor with a channel direction at $\langle 100 \rangle$
16 and (b) the 45 tilt and 45 twist implant, the implanted ions enter the substrate at the $\langle 110 \rangle$
17 direction. This direction increases the channeling of the ion to create a graded junction.

18
19 An embodiment is a method of fabrication of doped regions in a
20 semiconductor device; comprising the steps of :

21 a) providing a $\{001\}$ silicon substrate;

1 b) forming a gate over said silicon substrate; said gate having a width and a length;
2 a channel under the gate; said channel having a channel direction parallel
3 with the direction of said gate width; said channel direction is [100] or [010]
4 direction;

5 c) implanting ions into said silicon substrate to form a doped region adjacent to said
6 gate; the implantation of ions comprises a large angle tilt implant with a twist
7 of between about 40 and 50 degrees and a tilt angle of 40 and 50 degrees.

8 Another aspect of the embodiment is where said doped region is a N-
9 LDD in an offset LDMOS FET.

10 Another aspect of the embodiment is where said ions being implanted
11 about along the [110] directions of the silicon substrate.

12 Another aspect of the embodiment is where the implanting of said ions
13 is performed in one implant step at an about 45 degree twist implant and a tilt angle of
14 about 45 degrees.

15 Another aspect of the embodiment is where said silicon substrate has a notch/flat at a
16 [110] direction.

17 Another aspect of the embodiment is where the implanting of ion further
18 comprises: said silicon substrate has a notch/flat at a $\langle 110 \rangle$ direction, the implantation
19 comprises an implant with a 45 tilt and 45 twist and the ions enter the substrate aligned at
20 a $\langle 0 -1 -1 \rangle$ direction whereby the direction increases the channeling.

1 Another aspect of the embodiment is where said channel has an annular
2 shape with a doped region on the inside of said channel and a second doped region
3 surrounding the outside of said channel.

4 Another aspect of the embodiment is where said channel has an annular
5 shape with a doped region on the inside of said channel region and a second doped region
6 surrounding the outside of said channel; and the implanting of said ions further comprises
7 a quadra implant at the twist angles of about 45, 135, 225 and 315 degrees with a range of
8 +/- 5 degrees; and a tilt angle between 40 and 50 degrees.

9 Another aspect of the embodiment is where said channel has an annular
10 shape with a doped region on the inside of said channel and a second doped region
11 surrounding the outside of said channel region; and the implanting of said ions further
12 comprises a quadra implant with the ion beams aligned with the $\langle 110 \rangle$ direction within
13 plus/minus 2 degrees.

14 The orientation and implant process creates more channeling of ions.
15 The channeling of ions creates a more graded junction.

16 When implemented on a HV MOS Tx, the graded junction of the LDD
17 increases the drain breakdown voltage.

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19 The above and below advantages and features are of representative
20 embodiments only, and are not exhaustive and/or exclusive. They are presented only to
21 assist in understanding the invention. It should be understood that they are not
22 representative of all the inventions defined by the claims, to be considered limitations on

1 the invention as defined by the claims, or limitations on equivalents to the claims. For
2 instance, some of these advantages may be mutually contradictory, in that they cannot be
3 simultaneously present in a single embodiment. Similarly, some advantages are applicable
4 to one aspect of the invention, and inapplicable to others. Furthermore, certain aspects of
5 the claimed invention have not been discussed herein. However, no inference should be
6 drawn regarding those discussed herein relative to those not discussed herein other than for
7 purposes of space and reducing repetition. Thus, this summary of features and advantages
8 should not be considered dispositive in determining equivalence. Additional features and
9 advantages of the invention will become apparent in the following description, from the
10 drawings, and from the claims.

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3 **Brief Description of the Drawings**

4 The features and advantages of a semiconductor device according to the
5 present invention and further details of a process of fabricating such a semiconductor
6 device in accordance with the present invention will be more clearly understood from the
7 following description taken in conjunction with the accompanying drawings in which like
8 reference numerals designate similar or corresponding elements, regions and portions and
9 in which:

10 Figure 1A is a top down view of a wafer having a transistor according to
11 a process known to the inventor.

12 Figure 1B shows a schematic view of a twist and tilted ion implant
13 according to the prior art for use in understand the terms “twist” and “tilt”.

14 Figure 2A shows a FET with a channel direction 202 in a <100>
15 direction according to an embodiment of the invention.

16 Figure 2B shows a FET with a channel direction 204 in a <110>
17 direction according to an embodiment of the invention.

18 Figure 3A is a top down view of a wafer showing the channel
19 orientation in a 45 degree twist and 45 degree tilt implant according to an embodiment of
20 the invention.

1 Figure 3B is a top down view of a wafer showing the channel
2 orientation $\langle 010 \rangle$ in a 45 degree twist and 45 degree tilt implant according to an
3 embodiment of the invention.

4 Figure 3C illustrates a top down view of a quad implant according
5 to an embodiment of the invention.

6 Figure 4A shows a top down view of a embodiment of a closed
7 shaped transistor according to an embodiment of the invention.

8 Figure 4B shows a cross sectional view of the closed FET shown in
9 figure 4A along the axis 4B according to an embodiment of the invention.

10 Figure 5 shows a plot of the phosphorus concentration of the graded
11 junction N- LDD of the embodiment in a normal V MOS TX compared to a
12 conventional Ph profile.

13 Figure 6 shows both a standard 0 degree channel 102 104 FET and
14 the embodiments' 45 degree angled channel 202 204 FETs formed on a wafer.

15 Figure 7 shows an example of an offset LDMOS TX according to an
16 embodiment of the invention. The channel for the LDNMOS TX is preferably a p-
17 well.

18 Figure 8 shows an example of a non-offset LDMOS TX formed
19 using the embodiment's channel maximizing implant process for the source and drain.

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3 **Detailed Description of the Preferred Embodiments**

4 **II. INTRODUCTION - CURRENT INDUSTRY CHANNEL**
5 **DIRECTION WITH RESPECT TO THE CRYSTAL DIRECTION**

6 Referring now to the drawing and more particularly to Fig 1A, there is
7 shown a structure over which the present invention is an improvement.

8 Figure 1A is a top down view of a wafer having a transistor. The wafer
9 is {001}. The channel direction 102 is $\langle 110 \rangle$. The channel direction is the direction
10 between source and drain or drain and source. The channel direction is the direction
11 current flows between the source and drain or drain and source. In current 8 inch P-type
12 wafer technology, the notch is along the $\langle 110 \rangle$ direction as shown in figure 1A.

13 In manufacturing the FET with the source (S) and drain (D) separated
14 by the gate (G) and having a channel (C) thereunder, the notch permits alignment of the
15 wafer relative to the exposure masks so that the gate width and the channel length
16 thereunder will be parallel or perpendicular with $[110]$ crystal direction.

17
18 **Problem of voltage limitation on Hi Vt NMOS**

19 As the transistor scaling to smaller dimension, our high Vt NMOS
20 transistor is facing a problem with voltage limitation. Thermal cycle was limited because
21 of the consideration of logic device in the wafer.

1
2 Currently for high voltage transistor, we need to use high tilt
3 implantation and long time diffusion in order to make the lateral junction of the LDD more
4 graded. For example a lateral diffusion metal oxide semiconductor {LDMOS} was used
5 for high voltage usage. However the LDD regions of the LDMOS need long time (several
6 hours) diffusion to get a graded junction which can sustain high voltage. For sub-micron
7 technology, because of the thermal cycle become more critical. Lower thermal cycle was
8 needed because of the transistor dimension. In this case, LDMOS is not popular for small
9 dimension high voltage transistor. There are mainly two high voltage transistors in the
10 foundry for sub-micron transistors, offset transistor and non-offset transistor. Offset
11 transistor use asymmetrical structure to get higher breakdown voltage. Non-offset
12 structure use higher tilt angle for lateral doped drain (LDD) implantation to increase the
13 breakdown voltage.

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15 ***Overview of embodiments of the invention***

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17 In this example embodiment, a special layout for a high voltage
18 transistor is introduced. A set of specific implantation method is given accordingly. A
19 main advantage of this embodiment is to use the silicon crystallography to get higher
20 channeling effect through special implantation angle and rotation. Accordingly the layout
21 for this implantation was optimized in order to get a more graded junction.

1 We implant ions into the {0 0 1} silicon substrate to form doped regions
2 adjacent to the gate. The orientation of the channel region in the Si crystal structure
3 (channel direction $\langle 100 \rangle$) in combination with the large angle tilt and twist implant
4 process (describe below) produces doped regions that have a more graded (gradual)
5 junction. The orientation and implant process creates more channeling of ions. The
6 channeling of ions creates a more graded (less abrupt) junction.

7 Embodiments of the invention include open and closed shaped
8 transistors and doped regions. An example of a closed shaped Tx is shown in figure 4A.
9 Other embodiments include 45 degree twist / 45 degree tilt implants. Other embodiment
10 include quadra twist and tilt implants.

11

12 With the embodiments of the invention, we can improve breakdown
13 voltage of HV transistor. More graded junction LDD can be obtained without using long
14 diffusion time.

15 In accordance with the present invention, a standard {001} silicon wafer
16 with a primary notch of $\langle 110 \rangle$ direction is used and, before exposure to an image by a
17 lithographic exposure apparatus, the relative relationship between the mask and the {001}
18 silicon wafer is changed so that the relationship, in the same plane, is approximately forty-
19 five degrees (45 degree) from the normal relationship in the same plane. Thus, the [110]
20 crystal direction is aligned approximately 45 degrees to the gate width and will be aligned
21 parallel with channel length direction when voltage is applied to the gate.

1 This 45 degree change is preferably accomplished by either modifying
2 the mask holder or the wafer holder of an optical lithographic system so the mask holder
3 and the wafer holder are in a relationship of approximately forty-five degrees (45°) from
4 their normal relationship using the $\langle 001 \rangle$ crystal direction. The target of the relationship
5 change is exactly 45 degree, because the mobility of the carriers in channel will be
6 optimum when the channel and $[110]$ crystal direction are parallel. However, due to slight
7 imperfection of the lithographic apparatus wafer and mask holders, the change may vary
8 by $\pm 2\%$ of the 45 degree change. The remaining fabrication steps, such as plasma or
9 anisotropic etching, oxidation, chemical vapor deposition, sputtering and planization, are
10 performed without any modification of the wafer holders, because the exposed surface of
11 the silicon wafer to these processes remains in the $\langle 001 \rangle$ direction.

12 Referring to figure 6, on the same wafer, both standard 0 degree and the
13 embodiments' 45 degree angled channel FETs can be formed. For example, Figure 6
14 shows both standard 0 degree channel 102 104 FET and the embodiments' 45 degree
15 angled channel 202 204 FETs formed on a wafer (source/drain regions not shown).

16 Another aspect of the present invention is a novel FET with its gate
17 formed perpendicular to the $\langle 100 \rangle$ crystal direction so that the channel will be parallel
18 with this direction with a voltage applied to the gate.

19 In another aspect of the present invention, annular shaped FETs are
20 formed. Figure 6 shows annual FETs 602 and 612. FET 612 is has the embodiments
21 channel $\langle 100 \rangle$ direction. FET 602 has the $\langle 110 \rangle$ channel directions. Any combination of

1 annular and linear FETs with different channel directions can be formed on the same
2 wafer.

3 The embodiment's $\langle 100 \rangle$ channel direction is useful for MOS TX's and
4 can reduce punchthrough.

5 **III. Method of LATID with channel orientated in the $\langle 100 \rangle$ or**
6 **$\langle 010 \rangle$ direction**

7 A preferred embodiment of the invention is a method to form a doped
8 region in a semiconductor device. The doped region preferably is a source or drain region
9 in a FET and is more preferably a S or D region in a high voltage transistor such as a
10 LDMOS transistor.

11 A feature of the process is that a more graded junction is formed by the
12 large angled implant process.

13 ***$\{001\}$ silicon substrate having $[110]$ reference direction***

14 Referring to figure 2A and 2b, an orientation of the channel (C) of an
15 FET is shown. We provide a $\{001\}$ silicon substrate having $[110]$ reference direction
16 (direction from substrate center to primary notch/flat).

17 Figure 2A shows a FET with a channel direction 202 in a $\langle 100 \rangle$
18 direction.

19 Figure 2B shows a FET with a channel direction 204 in a $\langle 110 \rangle$
20 direction.

21 Devices with both channel directions can be formed on the same wafer.

1 ***Gate, Source/ Drain and Channel***

2 Next, a gate (G) is formed over the silicon substrate; the gate having a
3 width and a length; a channel under the gate.

4 The channel (C) has a channel direction (202 204) parallel with the
5 direction of the gate width. The channel direction is the direction of current flow direction.
6 The channel direction is preferably about [100] or [010] crystal direction.

7

8 ***Large Angle implant with Twist to form Source and Drain***

9 We implant ions into the silicon substrate to form doped regions
10 adjacent to the gate. The orientation of the channel region in the Si crystal structure
11 (channel direction $\langle 100 \rangle$) in combination with the large angle tilt and twist implant
12 process (describe below) produces doped regions that have a more graded (gradual)
13 junction. The orientation and implant process creates more channeling of ions. The ions are
14 preferably implanted along the $\langle 110 \rangle$ direction to maximize channeling. The channeling
15 of ions creates a more graded junction. Channeling is when implanted ions are not slowed
16 by collisions with silicon atoms. It is controlled by three different techniques: wafer tilt,
17 screen oxide layer or preamorphization. This embodiment preferably does not use these
18 techniques to reduce channeling.

19

20 When implemented on a HV MOS Tx, the graded junction of the LDD
21 increases the drain breakdown voltage.

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Figure 1B shows a schematic view of a twist and tilted ion implant according to the prior art for use in understand the terms “twist” and “tilt”.

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Tilt is the angle between the wafer surface and the ion beam.

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Twist is the angle between the vertical plane containing the ion beam and the vertical plane perpendicular to the reference direction (primary notch direction).

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Single Implant at 45 tilt and 45 twist

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As shown in figure 3A, the implantation of ions preferably comprises a tilt/twist implant with a twist of about 45 degree from the $\langle 110 \rangle$ reference direction (notch) of the crystal substrate and a tilt angle between 40 and 50 degrees (from the normal plane of the substrate surface) and more preferably a tilt angle of 45 degrees with a preferred tolerance of ± 5 degrees.

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For a (001) wafer (e.g., with a notch of $\langle 110 \rangle$) direction, a implant with a 45 tilt and 45 twist, the ions enter the substrate at a $\langle 0 -1 -1 \rangle$ (or $\langle 0\bar{1}1 \rangle$) direction (or $[110]$ group direction). This direction increases the channeling.

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The 45 tilt and 45 twist single implant is preferably performed by implanting Ph ions at an energy between 40 and 400 and a dose between $1E12$ and $1E15$ at tilt angle between 40 and 50 degrees and more preferably about 45 degrees and a twist angle of between 40 and 50 degrees and more preferably 45 degrees.

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22

This 45 degree twist and 45 degree tilt implant preferably forms a (symmetric) LDD.

1 **FET with a Source (S) and Drain (D) and gate (G) with a**
2 **channel direction of $\langle 100 \rangle$**

3 Figure 3B shows a top down view of a FET with a Source (S) and Drain
4 (D) and gate (G) with a channel direction of $\langle 100 \rangle$ and a reference direction $\langle 110 \rangle$ (also
5 for the primary notch).

6
7 For a 45 degree twist implant and a 45 degree tilt, the ions are implanted
8 into the S/D region along direction B. Direction B is parallel to the $\langle 0\bar{1}1 \rangle$ (or $\langle 0 -1 -1 \rangle$).

9 **“quadra” implant for open shaped tx**

10 In a preferred embodiment the implanting of ions into further comprises
11 an quadra implant. The quadra implant is performed by 4 implants of Ph ions at an
12 energy between 40 and 400 Kev and a dose between $1E12$ and $1E15$ ions/sq-cm at tilt
13 angle between 40 and 50 degrees and a twist angles of between 40 and 50 degrees

14 Figure 3C illustrates the embodiment’s quad implant. The 4 implants at
15 45, 135, 225, and 315 degrees.

16 In the quadra implant, the implanted ions are aligned in the $[0, -1, -1]$,
17 $[1, 0, -1]$, $[0, 1, -1]$, $[-1, 0, -1]$ or $\langle 110 \rangle$ directions. (the negative signs represent bars over the
18 1’s, e.g. -1 is equivalent to $\bar{1}$) This maximizes channeling.

1 ***Closed shaped (or annular shaped) channel region***

2 Referring to figure 4A and figure 4B, an embodiment is shown where
3 the transistor has a channel region with a “closed shape” so that S/D region on the inside
4 of the channel region and a second doped region surrounding the outside of the channel
5 region.

6 Figure 4A shows a top down view of an embodiment of a closed shaped
7 transistor (e.g., with annular shaped channel region). Figure 4 shows field oxide regions
8 402, LDD regions 406 414, source/drain regions 407 415 (see Fig 4B) and gate 410. The
9 LDD regions are preferably formed by the embodiment’s implant process. The “closed
10 shape” means that the active region has no beginning or end. The channel under the gate
11 410 is surrounded by the LDD 406. The channel is preferably annular shaped and is more
12 preferably rectangular or square shaped.

13 Figure 4B shows a cross sectional view of the closed FET shown in
14 figure 4A along the axis 4B according to an embodiment of the invention. Figure 4B
15 show a gate dielectric layer 412 under the gate 410.

16 The embodiments of the annular channel Tx can be a normal voltage Tx
17 or a offset LDMOS or a Non-offset LDMOS.

18 ***Quadra Implant method for closed (e.g., annular) channel***
19 ***region***

20 For the closed shaped doped region, for example as shown in figure 4A,
21 preferably a quadra implant is performed.

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HV LDMOS TX with offset transistor and non-offset transistors

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The channel orientations and implant embodiments of the invention on can be used to form HV LDMOS TX with offset transistor and non-offset transistors.

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Figure 7 shows an example of an offset LDMOS TX. The channel is a diffused p-well for the LDNMOS TX.

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In the offset LDMOS TX (figure 7), only the N-LDD is formed using the embodiment's ion implant at [110] to maximize the ion channeling.

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In the non- offset LDMOS TX (figure 8), preferably the N+ source and the N+ drain are simultaneously formed in the same implant step using the embodiment's ion implant at [110] to maximize the ion channeling.

13

Process for offset LDMOS TX (figure 7)

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The process to form the OFFset LDMOS TX is as follows:

15

□ form p-epi on substrate

16

□ form p-well

17

□ form (poly) gate

18

□ form N-LDD (using embodiments' channeling maximizing ion implant)

19

□ form spacers on gate

20

□ form source (S) and drain (D) using a standard I/I .

21

1 Currently, the offset LDMOS Tx operates at a voltage between about
2 18V and 60 V. In comparison a normal voltage Tx operates between about 1V to 18V.

4 ***non-offset LDMOS TX***

5 Figure 8 shows an example of a non-offset LDMOS TX. Usually we
6 use a lot of diffusion to get a smooth and graded junction between the N+ and p- well.
7 With the embodiment's wafer alignment and drain implant process, a good graded junction
8 can be obtained. The breakdown voltage decreases with the embodiment because of the
9 graded junction.

10 ***Process for non-offset LDMOS TX***

11 The process to form the figure 8, non-offset LDMOS TX is as follows:

- 12 □ form p-epi on substrate
- 13 □ form p-well
- 14 □ form poly gate
- 15 □ form N-LDD (using embodiments' channeling max ion implant)
- 16 □ form spacers
- 17 form N+ source and drain using invention's maximizing channeling ion implant.

18 Currently, the non-offset LDMOS Tx operates at a voltage between
19 about 12V and 25 V. In comparison a normal voltage Tx operates between about 1V to
20 18V.

21

1 **IV. EXAMPLES**

2 The following non-limiting examples represent preferred forms and best
3 modes contemplated by the inventor for practice of his invention, as well as illustrating the
4 results obtained through its use.

5 High Voltage LDMOS transistor were fabricated using the standard
6 transistor orientation shown in figure 1 and an embodiments orientation shown in figure
7 2A (e.g., channel in <100> direction). Ph ions were implanted at the conditions shown in
8 the table below to form the N-LDD.

9 **TABLE: comparison of embodiment and standard LDD implants**

parameter	45° tilt and 45°twist implant	30° tilt and 0° twist implant
dose	1E12 atoms/sq-cm	1E12 atoms/sq-cm
energy	80 Kev	80 Kev
Junction depth	0.75µm	0.5 µm
Breakdown voltage	16.2 V	14.0 V

10
11 As shown in the table above, the embodiment's 45° tilt and 45°twist
12 LDD implant had a deeper junction depth and a higher breakdown voltage.

13 The LDD implant on the embodiment's transistor orientation has
14 increased channeling of ion that creates a deeper and more graded junction. The reduces
15 the breakdown voltage. This is important especially on the HV transistor.

16
17 Figure 5 shows a plot of the phosphorus concentration of the graded
18 junction N- LDD of the embodiment in a normal V MOS TX compared to a conventional
19 Ph profile. The boron concentration of about 1E18 is the concentration of the p-well. (See
20 e.g., figure 7 and 8.)

1 **V. Ending**

2 In summary, a new set of layout and implantation methods was given in
3 the embodiments of this invention. A purpose is to use crystal structure of silicon to
4 improve the junction or the LDD or S/D to obtain high breakdown voltage. It can be used
5 for DMOS and HVNMOS and other high voltage transistor and normal MOS Transistors.

6 The embodiments' implant process can be performed on any wafer so
7 that the ions enter the wafer in the [110] direction. The embodiments are not dependents on
8 any configuration of wafer notches and/or flats. The orientation of notches and flat change
9 with wafer technology.

10 Given the variety of embodiments of the present invention just
11 described, the above description and illustrations show not be taken as limiting the scope
12 of the present invention defined by the claims.

13 While the invention has been particularly shown and described with
14 reference to the preferred embodiments thereof, it will be understood by those skilled in
15 the art that various changes in form and details may be made without departing from the
16 spirit and scope of the invention. It is intended to cover various modifications and similar
17 arrangements and procedures, and the scope of the appended claims therefore should be
18 accorded the broadest interpretation so as to encompass all such modifications and similar
19 arrangements and procedures.

20

What is claimed is:

1. A semiconductor device comprised of at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by a channel under the gate, comprising:
 - a {001} silicon substrate;
 - a gate having a gate length and a gate width; said gate having the gate width in the [100] or [010] crystal directions;
 - a source on one side of said gate and a drain on the other side of gate, with impurities of the source and drain being disposed in the {001} silicon substrate; and
 - a channel under the gate between the source and drain when voltage is applied and being aligned in a direction parallel with the direction of the gate width, whereby the performance of the FET is enhanced.

2. The semiconductor device of claim 1 which further comprises said channel has an annular shape.
3. The semiconductor device of claim 1 which further comprises a second gate over said silicon substrate; said second gate having a width and a length; a second channel under the second gate; said second channel having a second channel direction parallel with the direction of width of said second gate; said second channel direction is parallel or perpendicular with the $\langle 110 \rangle$ direction.
4. The semiconductor device of claim 1 wherein the field effect transistor is a LDMOS device comprised of said source, said drain, said gate and said channel.
5. An integrated circuit with at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by a channel under the gate, comprising:
 - a {100} monocrystalline silicon substrate having (100) and (110) crystal planes and [100] and [110] crystal directions;
 - a gate having a length and a width and being insulated from the substrate by a gate dielectric layer, said gate having a gate width in the [100] or [010] crystal direction;
 - a source on one side of the gate width and a drain on the other side of the gate width, and
 - a channel being formed under the gate between the source and drain when voltage is applied and being aligned in a direction parallel with the direction of the gate width.

6. The integrated circuit of claim 5 wherein the said channel has a closed shape with either said source or said drain surrounding the outside of said channel region.
7. The integrated circuit of claim 5 which further comprises a second FET over said {001} monocrystalline silicon substrate, said second FET comprised of a second gate over said {001} monocrystalline silicon substrate; said second gate having a second gate width and a second gate length; a second channel under the second gate; said second channel having a second channel direction parallel with the direction of width of said second gate; said second channel direction is parallel or perpendicular with the $\langle 110 \rangle$ direction.
8. The integrated circuit of claim 5 wherein said {001} monocrystalline silicon substrate has a notch/flat at a $[110]$ direction.
9. The integrated circuit of claim 5 wherein the field effect transistor is a LDMOS device comprised of said source, said drain, said gate and said channel.
10. The integrated circuit of claim 5 which further comprises a second FET over said {001} monocrystalline silicon substrate, said second FET comprised of a second gate over said {001} monocrystalline silicon substrate; said second gate having a second gate width and a second gate length; a second channel under the second gate; said second channel having a second channel direction parallel with the direction of width of said second gate; said second channel direction is parallel or perpendicular with the $\langle 110 \rangle$ direction; and
a third FET with an annular channel.

11. The integrated circuit of claim 5 wherein said gate has a gate width in the [100] crystal direction so that the gate width is aligned approximately orthogonal to the (100) crystal plane and parallel with the [100] crystal direction.
12. The integrated circuit of claim 5 wherein the {001} monocrystalline silicon substrate is comprised of a wafer having a <110> reference direction from a substrate center to a primary notch/flat.
13. The semiconductor device of claim 1 wherein said {001} silicon substrate is comprised of a wafer having a <110> reference direction from a substrate center to a primary notch/flat.
14. The semiconductor device of claim 1 which further includes a second FET having a second channel with a closed shape with either a second source or a second drain surrounding the outside of said second channel.
15. The semiconductor device of claim 1 which further includes a second FET having a rectangular shaped channel with a closed shape with either a second source or a second drain surrounding the outside of said second channel.
16. The semiconductor device of claim 1 which further includes a second FET having a second channel having a closed shape; said second channel has a second channel direction in the <100> or <110> directions.

17. The semiconductor device of claim 1 which further includes a second FET having a second channel with a rectangular shape; the second channel has a second channel direction in the $\langle 110 \rangle$ directions.

18. A semiconductor device comprised of at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by a channel under the gate, comprising:

a {001} silicon substrate;

a gate comprised of a first gate portion; said first gate portion having a first gate portion length and a first gate portion width; said first gate portion width in the [100] or [010] crystal directions;

a source on one side of said gate and a drain on the other side of the gate, with impurities of the source and drain being disposed in the {001} silicon substrate; and

a first channel region under the first gate portion between the source and drain; the first channel region aligned in a direction parallel with [100] or [010] crystal directions, whereby the performance of the FET is enhanced.

19. The semiconductor device of claim 18 wherein the gate is comprised of a second gate portion;

a second channel region under the second gate portion between the source and drain; the second channel region aligned in a direction perpendicular with said first gate portion.

20. The semiconductor device of claim 18 wherein the gate has a closed shape.

21. The semiconductor device of claim 1 wherein said channel has an annular shape; and said source or said drain has an annular shape.

22. The semiconductor device of claim 1 wherein said channel has an annular shape; and said source and said drain both have an annular shape.

23. The semiconductor device of claim 1 wherein said channel has an annular shape; and said source or said drain has an annular rectangular shape.