CLAIMS

What is claimed is:

1. A method implemented by a video decoder and comprising:

receiving, by the video decoder, a video bitstream comprising a sequence parameter set (SPS) raw byte sequence payload (RBSP), wherein the SPS RBSP comprises a first SPS level flag, wherein the first SPS level flag equal to 1 specifies that an affine inter flag is present in coding unit syntax, wherein the first SPS level flag equal to 0 specifies that the affine inter flag is not present in the coding unit syntax, and wherein the affine inter flag equal to 1 specifies that for a current coding unit, when decoding a P or a B slice, affine model based motion compensation is used to generate prediction samples of the current coding unit, and wherein the affine inter flag equal to 0 specifies that the current coding unit is not predicted by affine model based motion compensation; and

wherein a second SPS level flag is conditionally signaled, wherein when the first SPS level flag is equal to 0, the second SPS level flag is not signaled, and when first SPS level flag is equal to 1, the second SPS level flag is signaled;

when the second SPS level flag is equal to 0 or when the affine inter flag is equal to 0, affine_ type _flag is not signaled in the coding unit syntax, and when the second SPS level flag is equal to 1 and when the affine inter flag is equal to 1, the affine_type_flag is signaled in the coding unit syntax, wherein the affine_type_flag equal to 0 specifies that, for the current coding unit, when decoding the P or B slice, 4-parameter-affine-model-based motion compensation is used to generate the prediction samples of the current coding unit, and wherein the affine_type_flag equal to 1 specifies that, for the current coding unit, when decoding the P or B slice, 6-parameter-affine-model-based motion compensation is used to generate the prediction samples of the current coding unit; and

decoding, based on the first SPS level flag, a video sequence from the video bitstream.

2. A method implemented by a video encoder and comprising:

generating, by the video encoder, a first sequence parameter set (SPS) level flag, wherein the first SPS level flag equal to 1 specifies that an affine inter flag is present in coding unit syntax, wherein the first SPS level flag equal to 0 specifies that the affine inter flag is not present in the coding unit syntax, and wherein the affine inter flag equal to the first value specifies that for a current coding unit, when decoding a P or a B slice, affine model based motion compensation is used to generate prediction samples of the current coding unit, and wherein the affine inter flag equal to 0 specifies that the current coding unit is not predicted by affine model based motion compensation;

wherein a second SPS level flag is conditionally signaled, wherein when the first SPS level flag is equal to 0, the second SPS level flag is not signaled, and when first SPS level flag is equal to 1, the second SPS level flag is signaled;

when the second SPS level flag is equal to 0 or when the affine inter flag is equal to 0, affine_ type _flag is not signaled in the coding unit syntax, and when the second SPS level flag is equal to 1 and when the affine inter flag is equal to 1, the affine_type_flag is signaled in the coding unit syntax, wherein the affine_type_flag equal to 0 specifies that, for the current coding unit, when decoding the P or B slice, 4-parameter-affine-model-based motion compensation is used to generate the prediction samples of the current coding unit, and wherein the affine_type_flag equal to 1 specifies that, for the current coding unit, when decoding the P or B slice, 6-parameter-affine-model-based motion compensation is used to generate the prediction samples of the current coding unit; and

encoding the first SPS level flag into an SPS raw byte sequence payload (RBSP); and

encoding the SPS RBSP into a video bitstream.

3. An encoding apparatus comprising:

a memory; and

a processor coupled to the memory and configured to perform the method of claim 2.

4. A decoding apparatus comprising:
a memory; and
a processor coupled to the memory and configured to perform the method of claim 1.

5. A computer program product comprising computer-executable instructions stored on a non-transitory medium that when executed by a processor cause an apparatus to perform the method of claim 1 or 2.