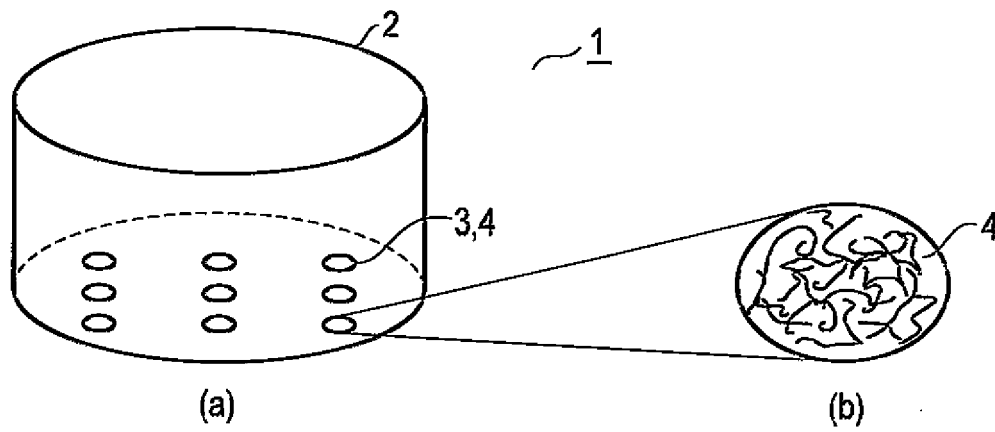
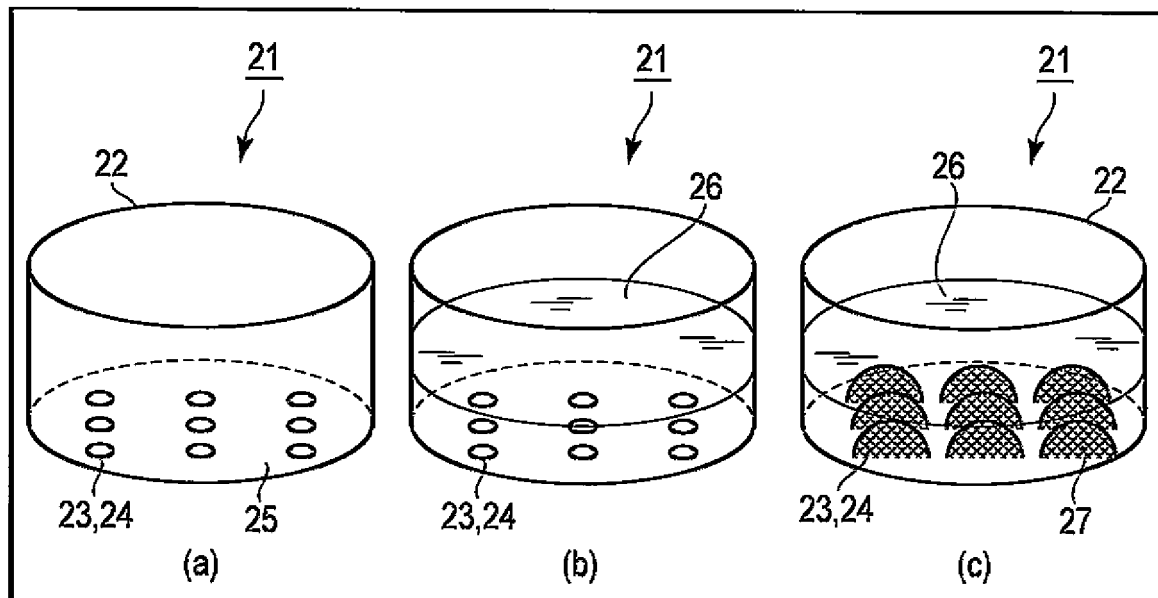


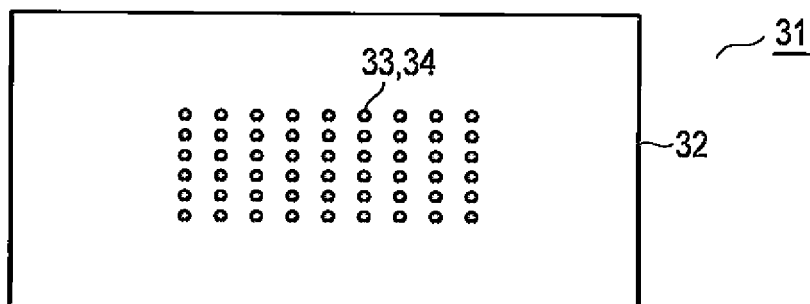
[図1]



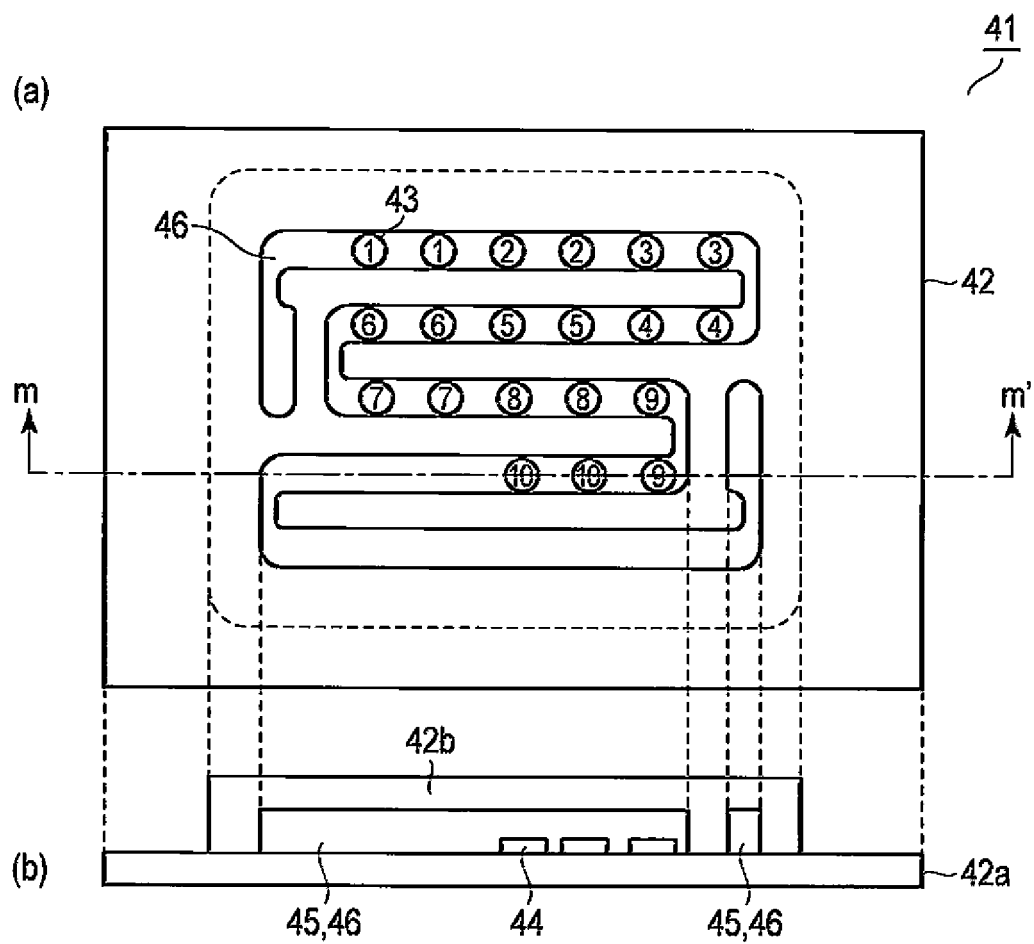
[図2]



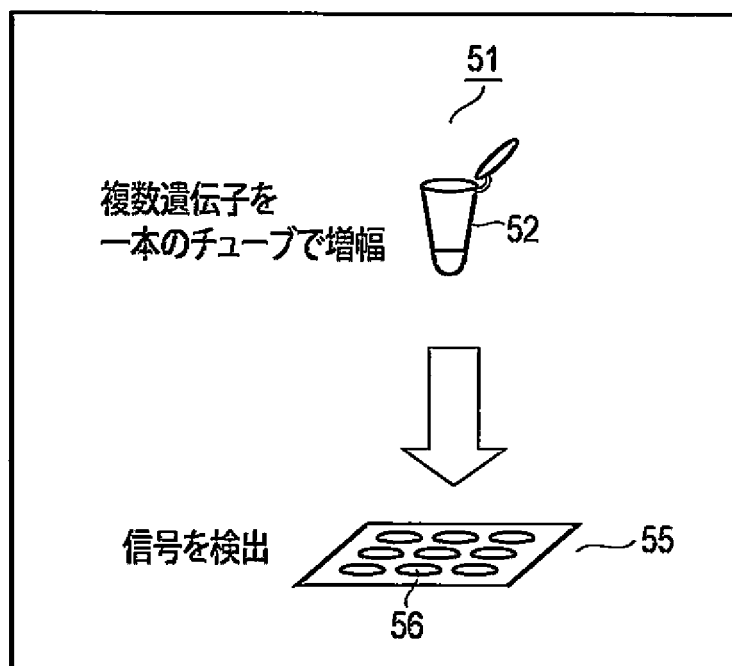
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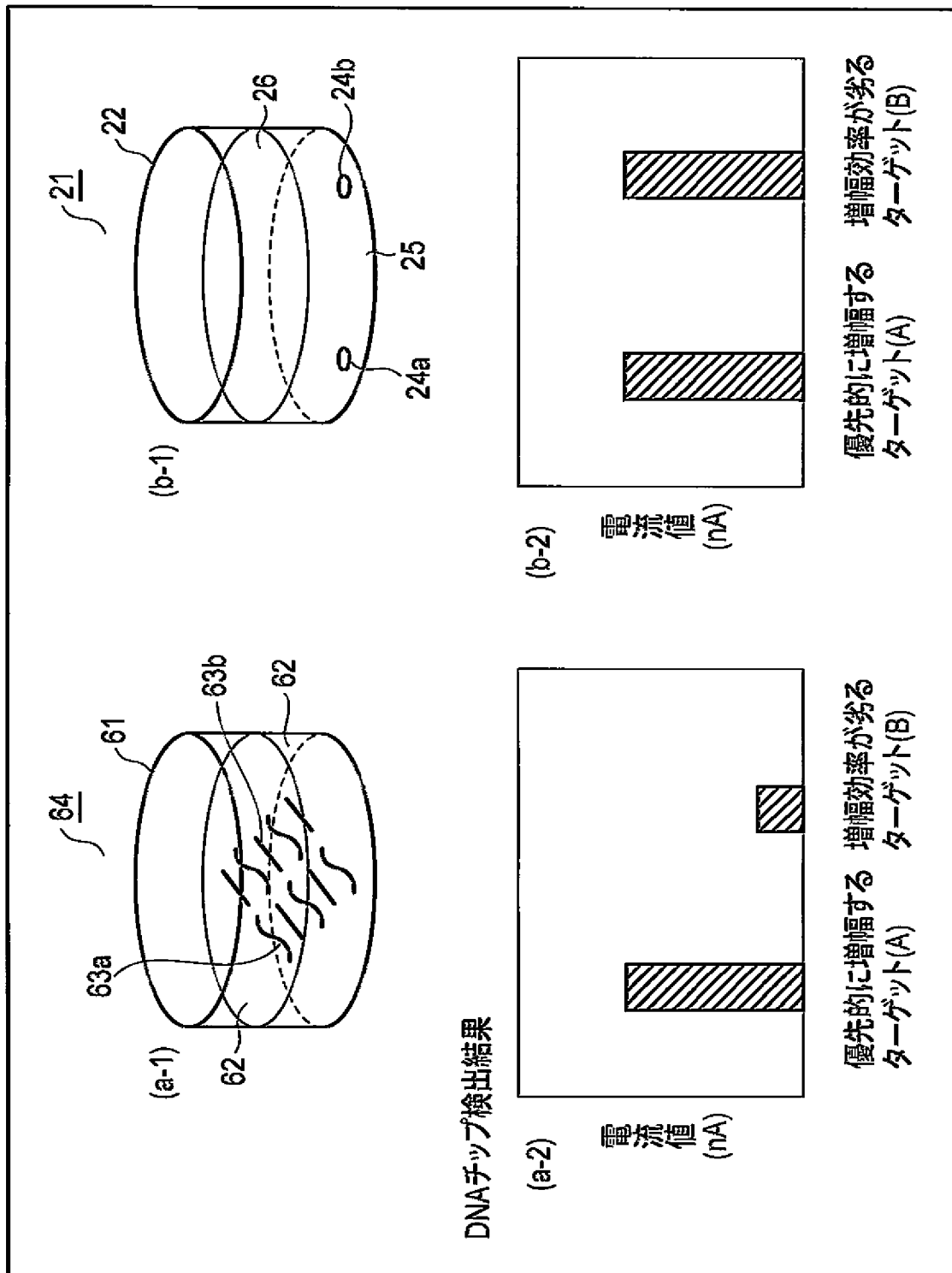
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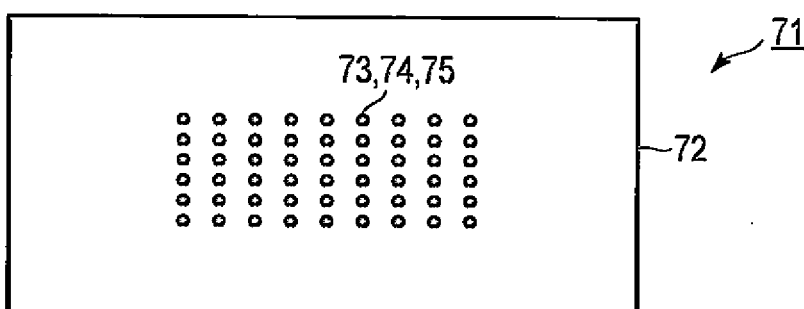
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[図6]

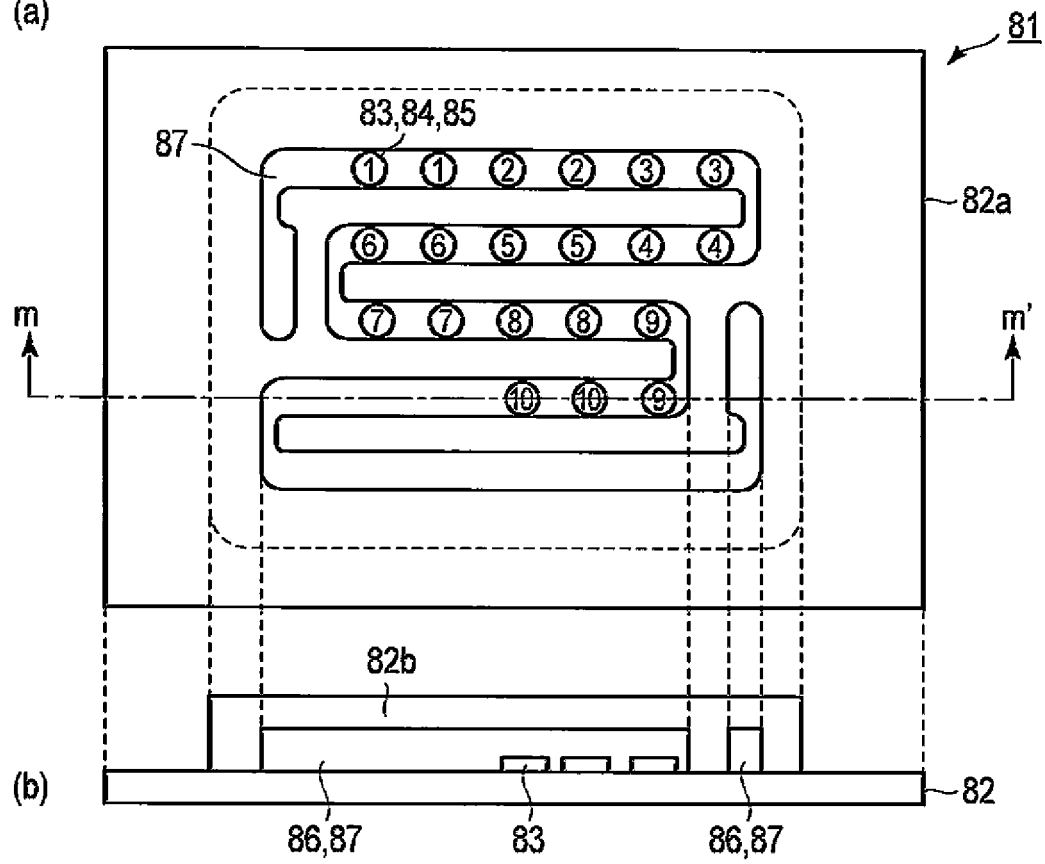


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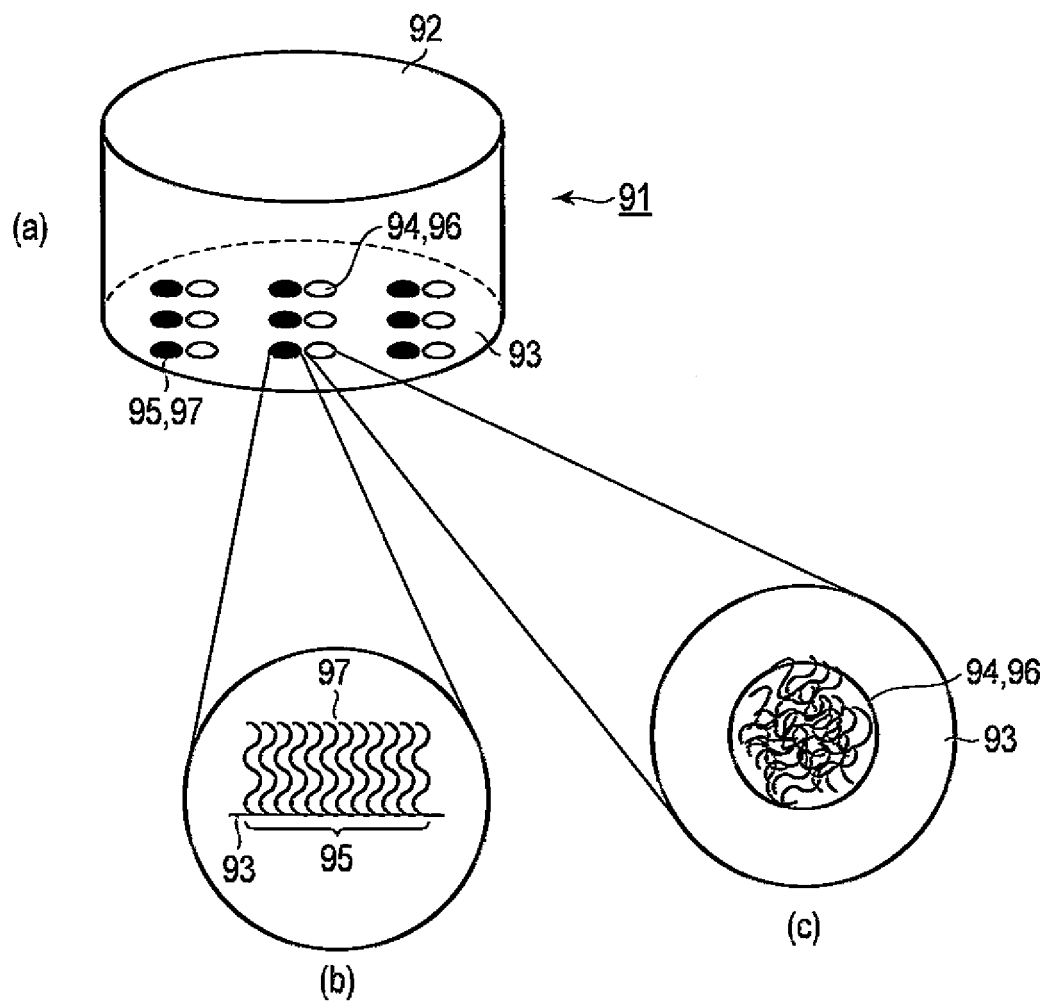


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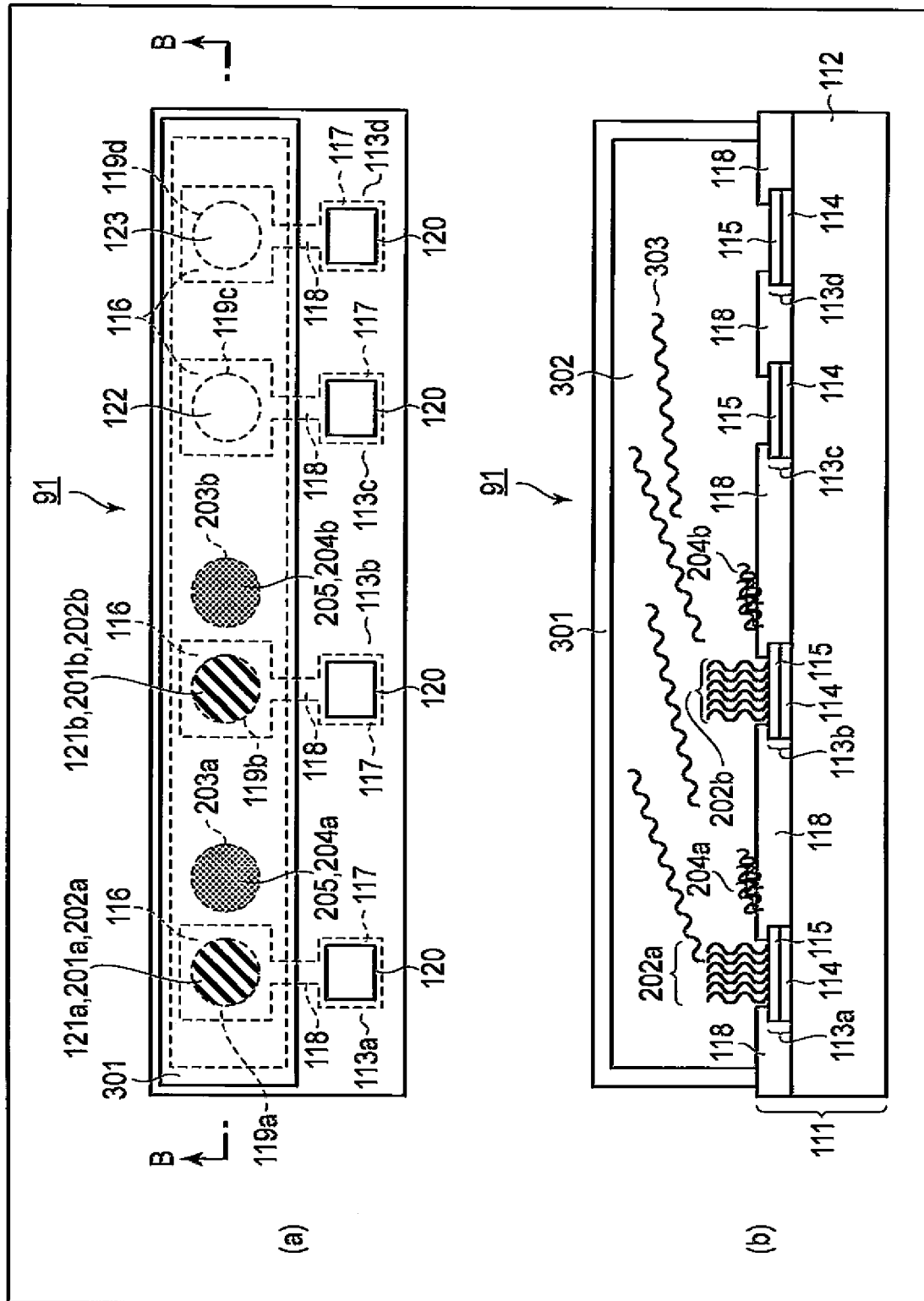
(a)



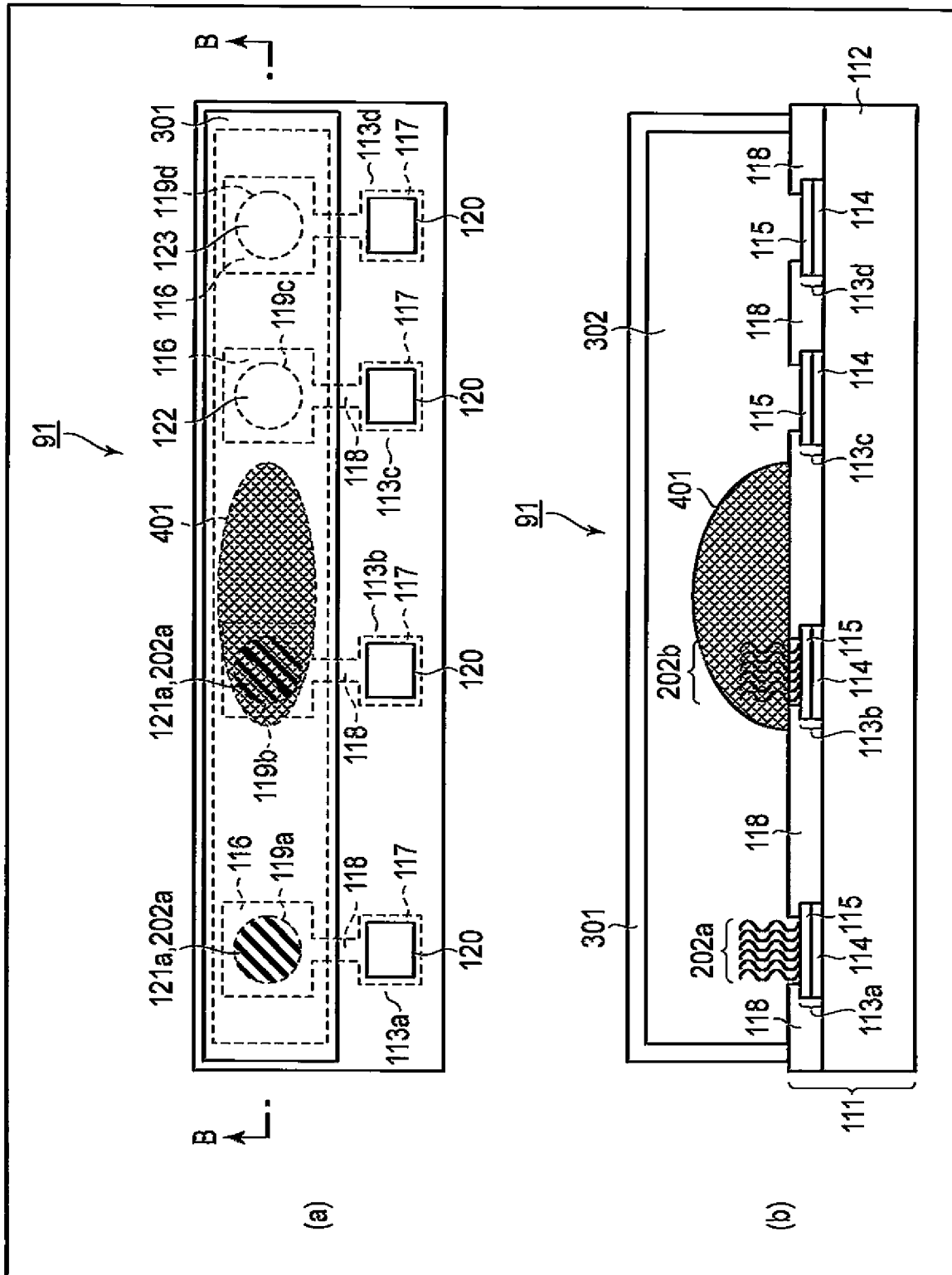
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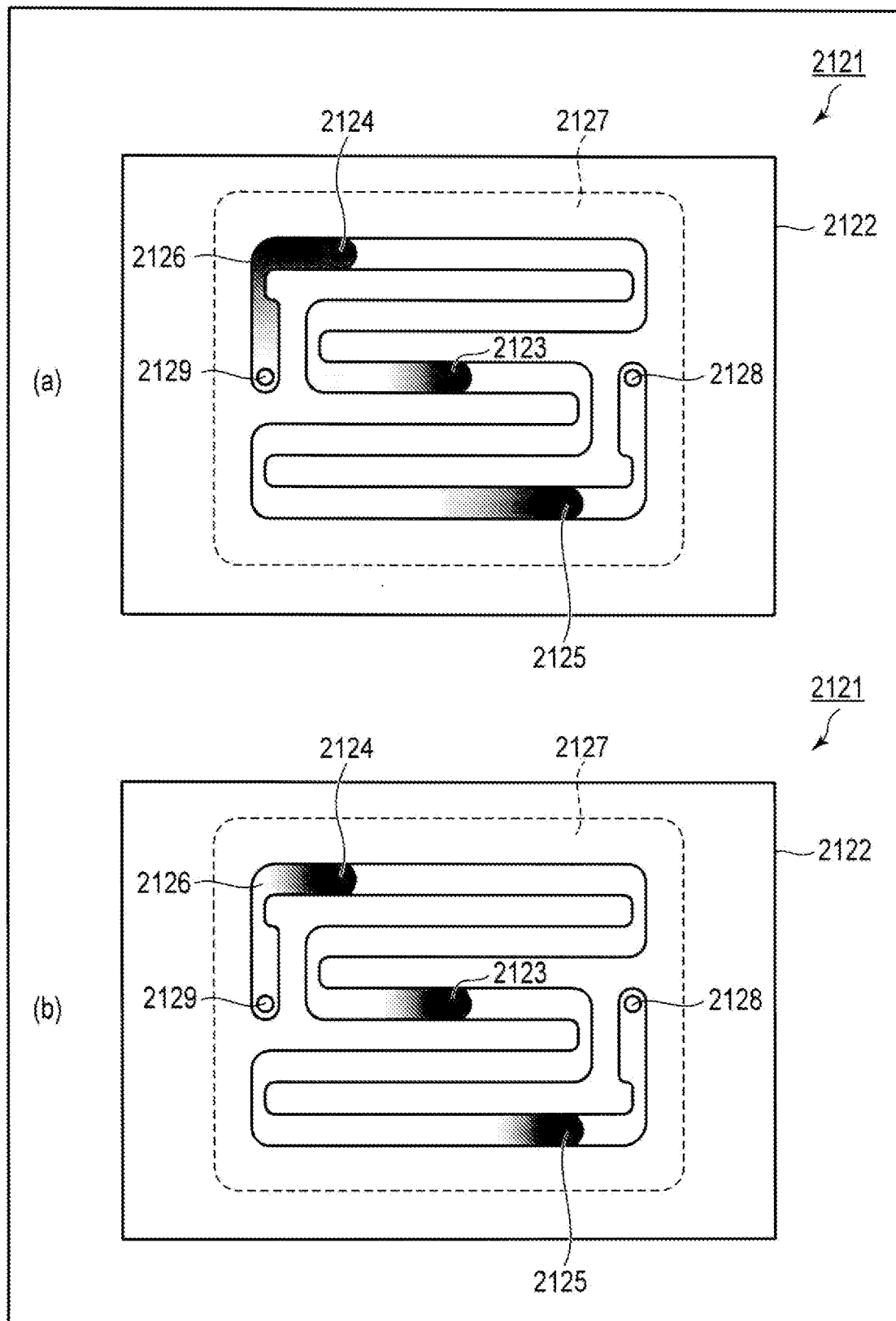
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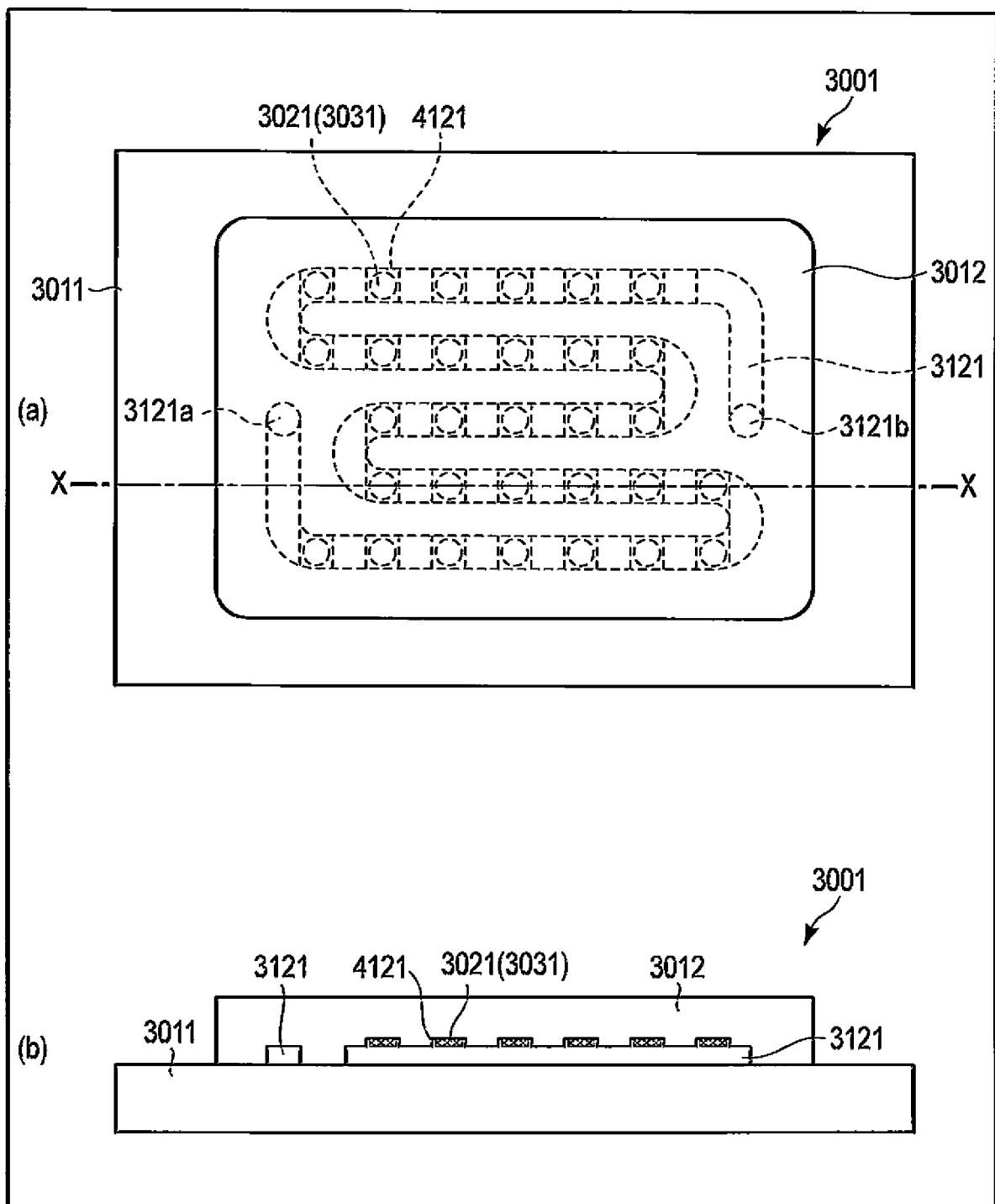
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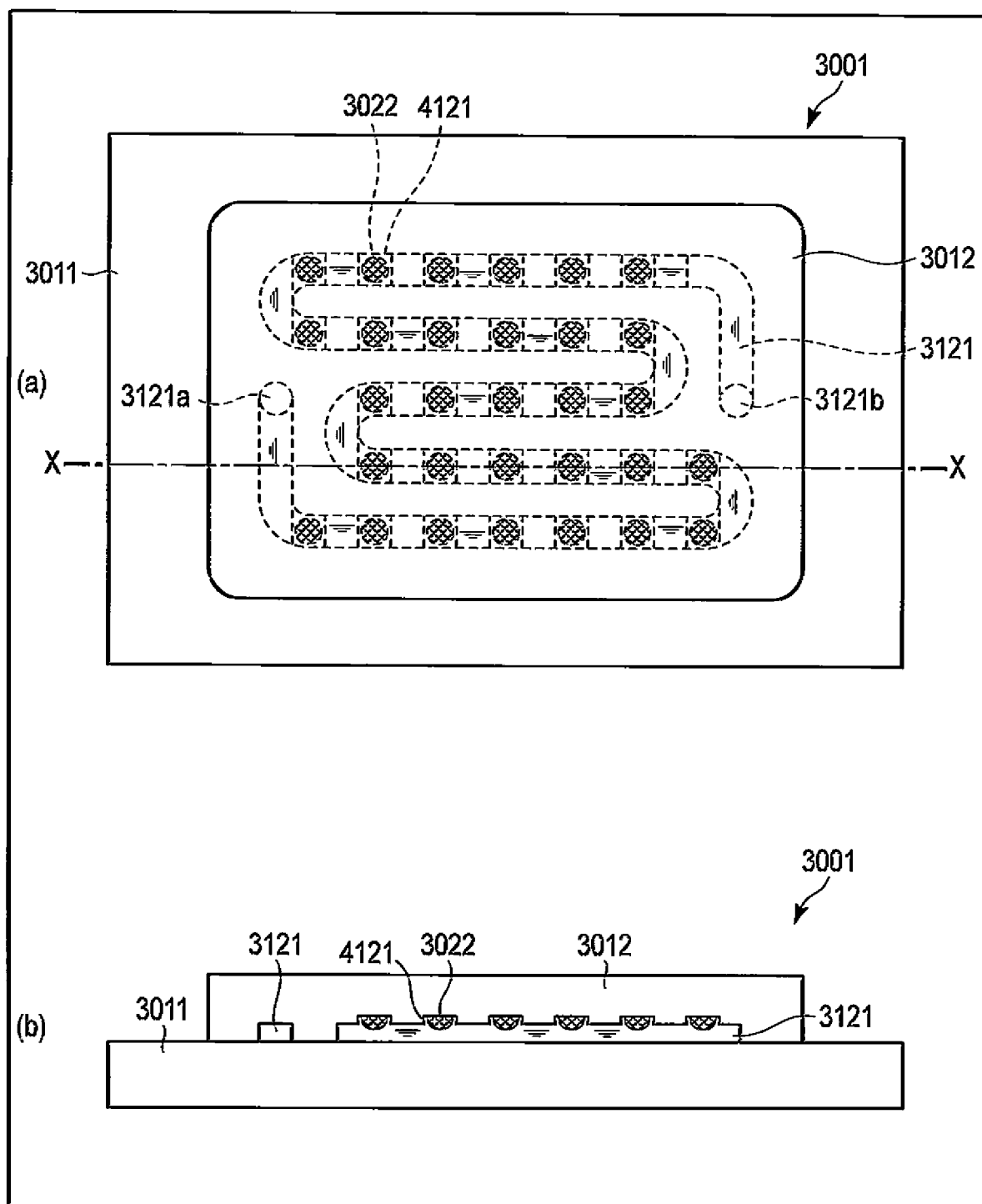
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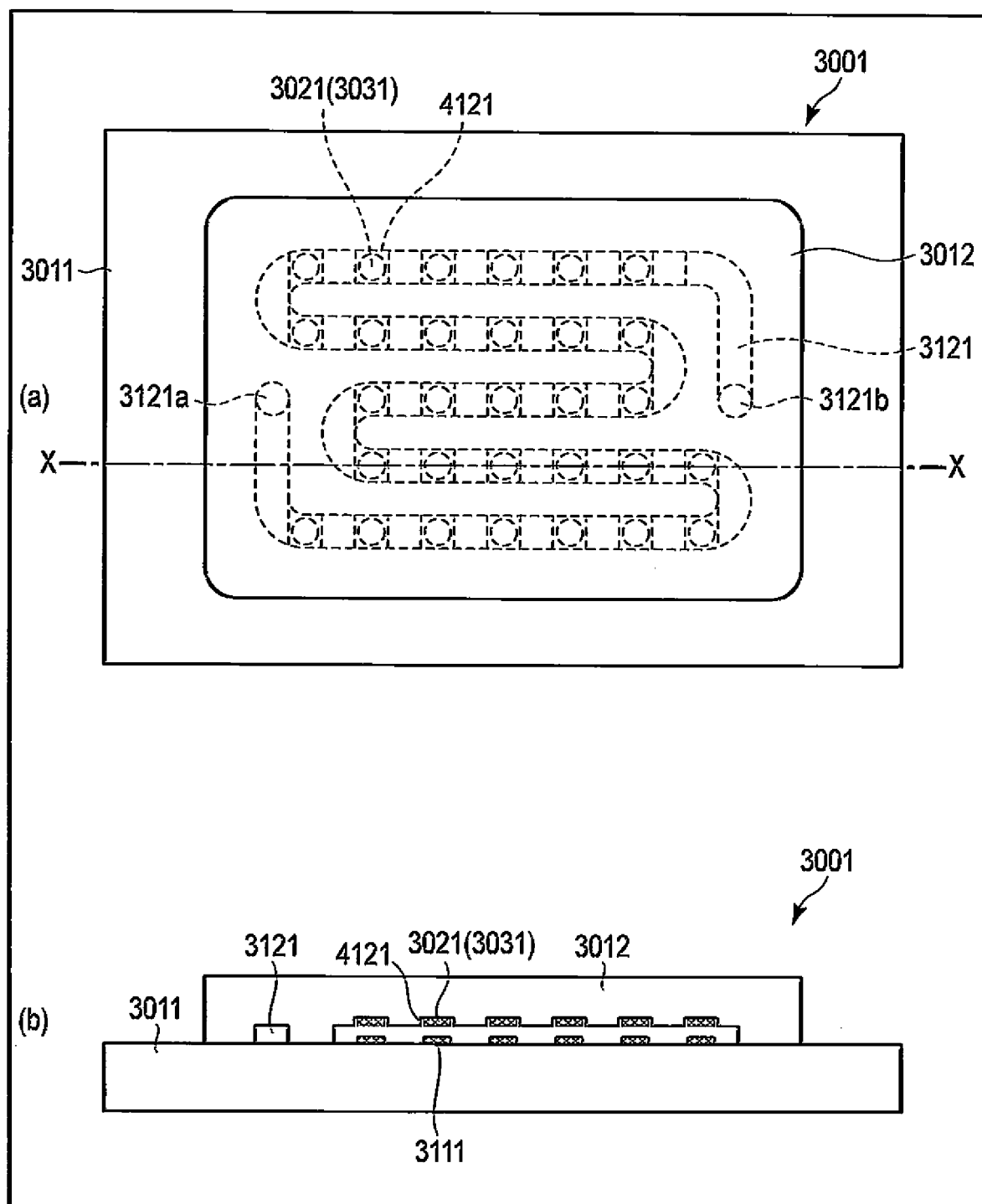
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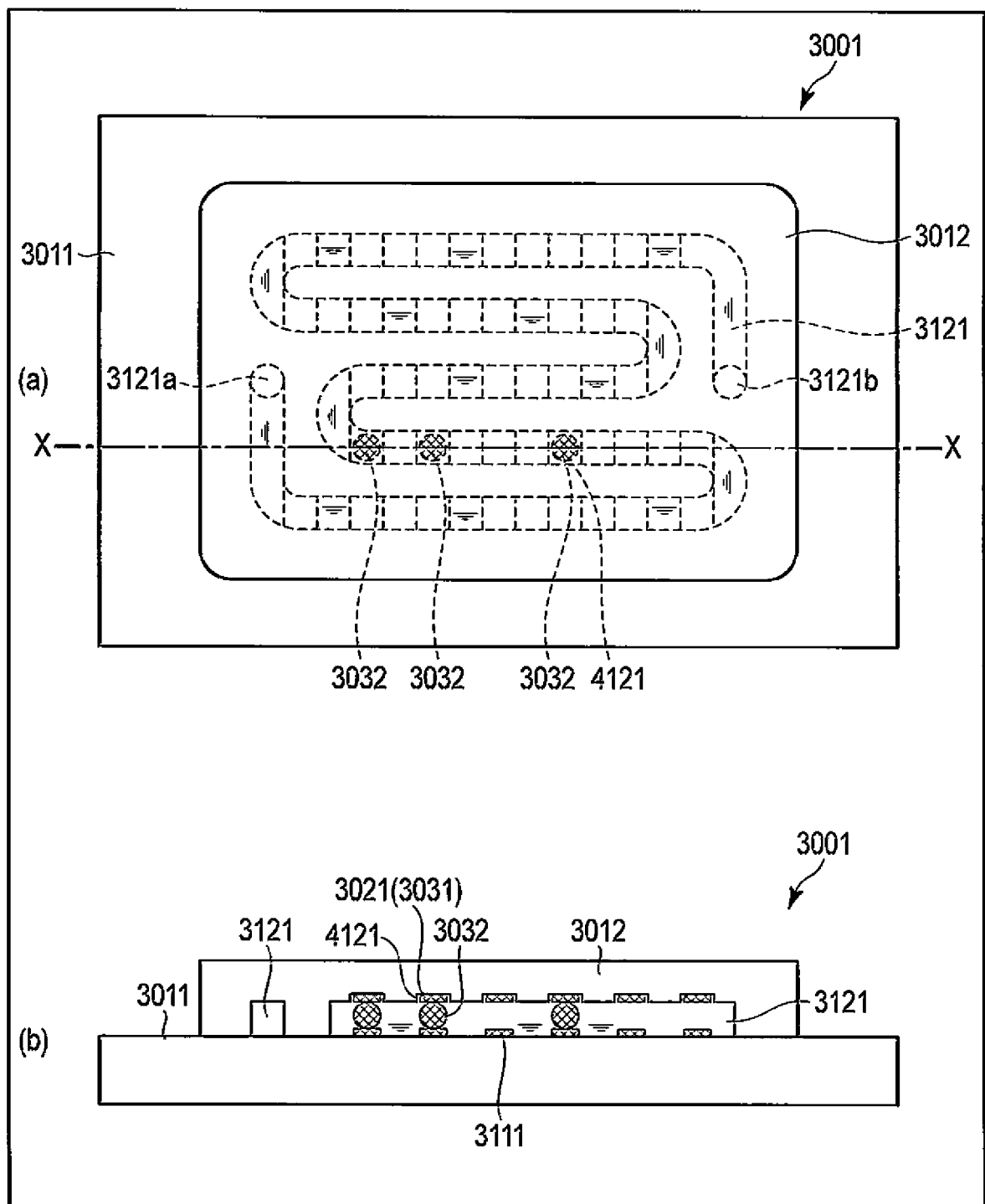
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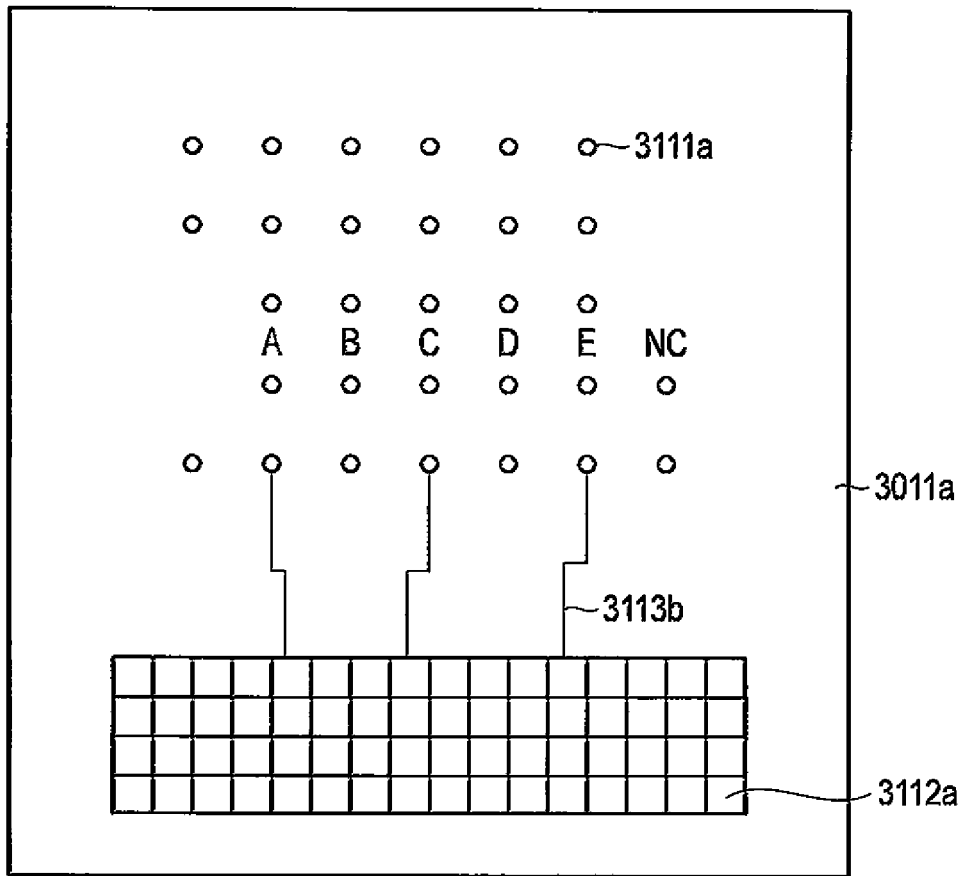
[図19]



[図20]



[図21]



[図22]

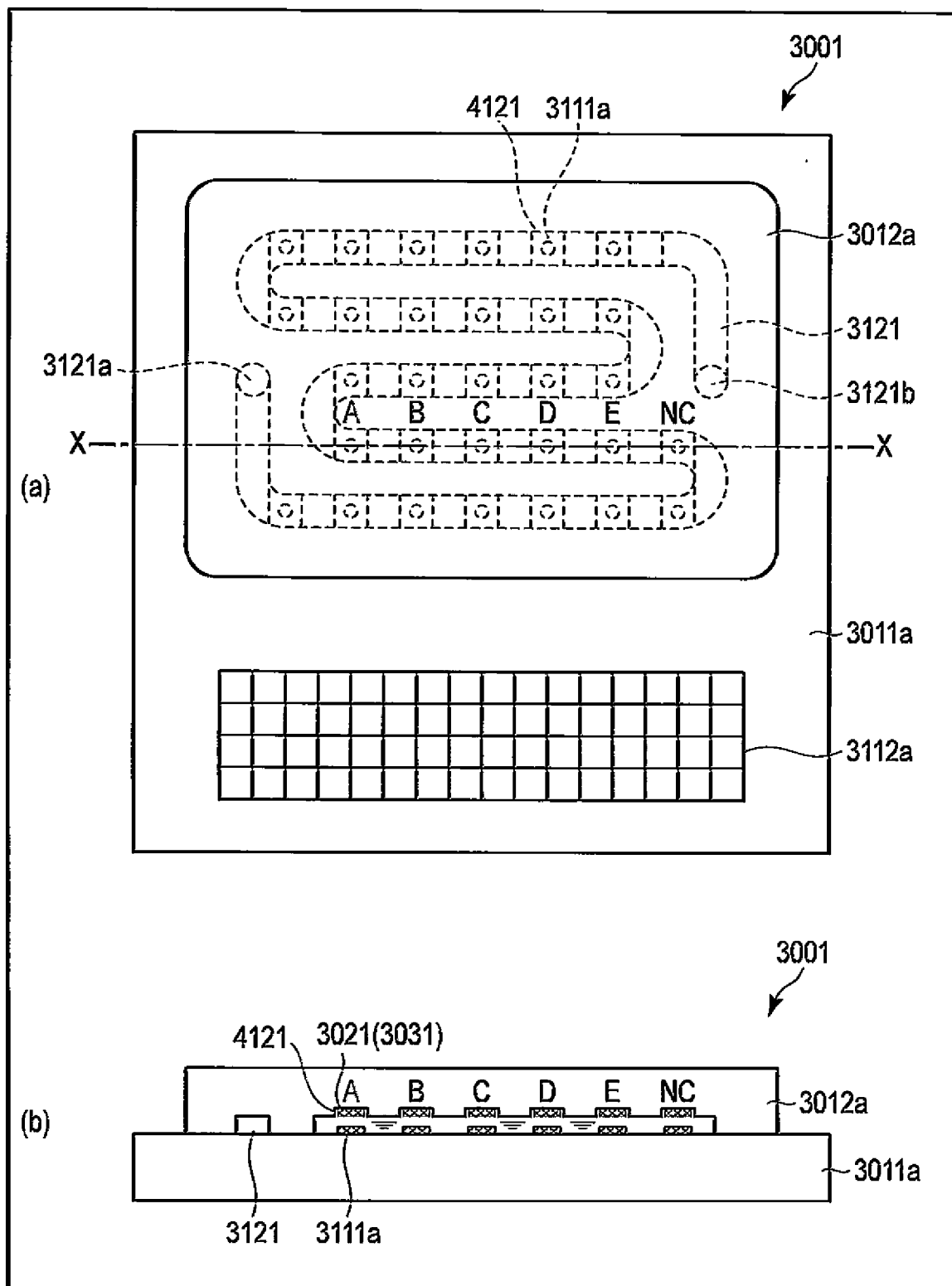
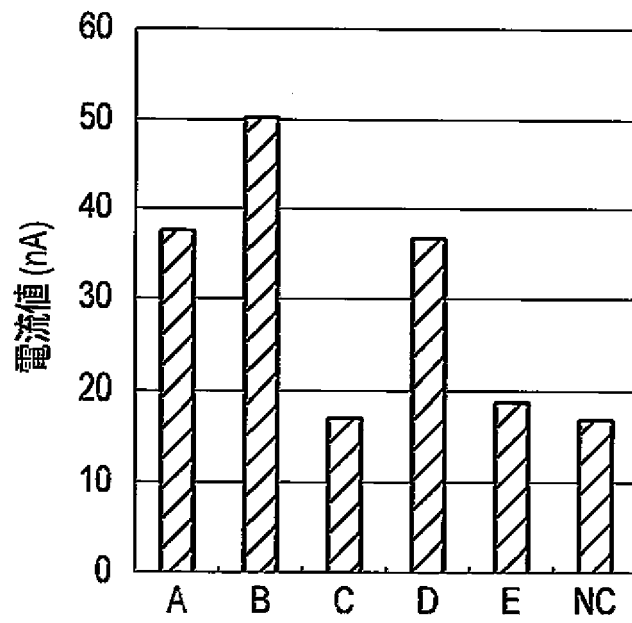
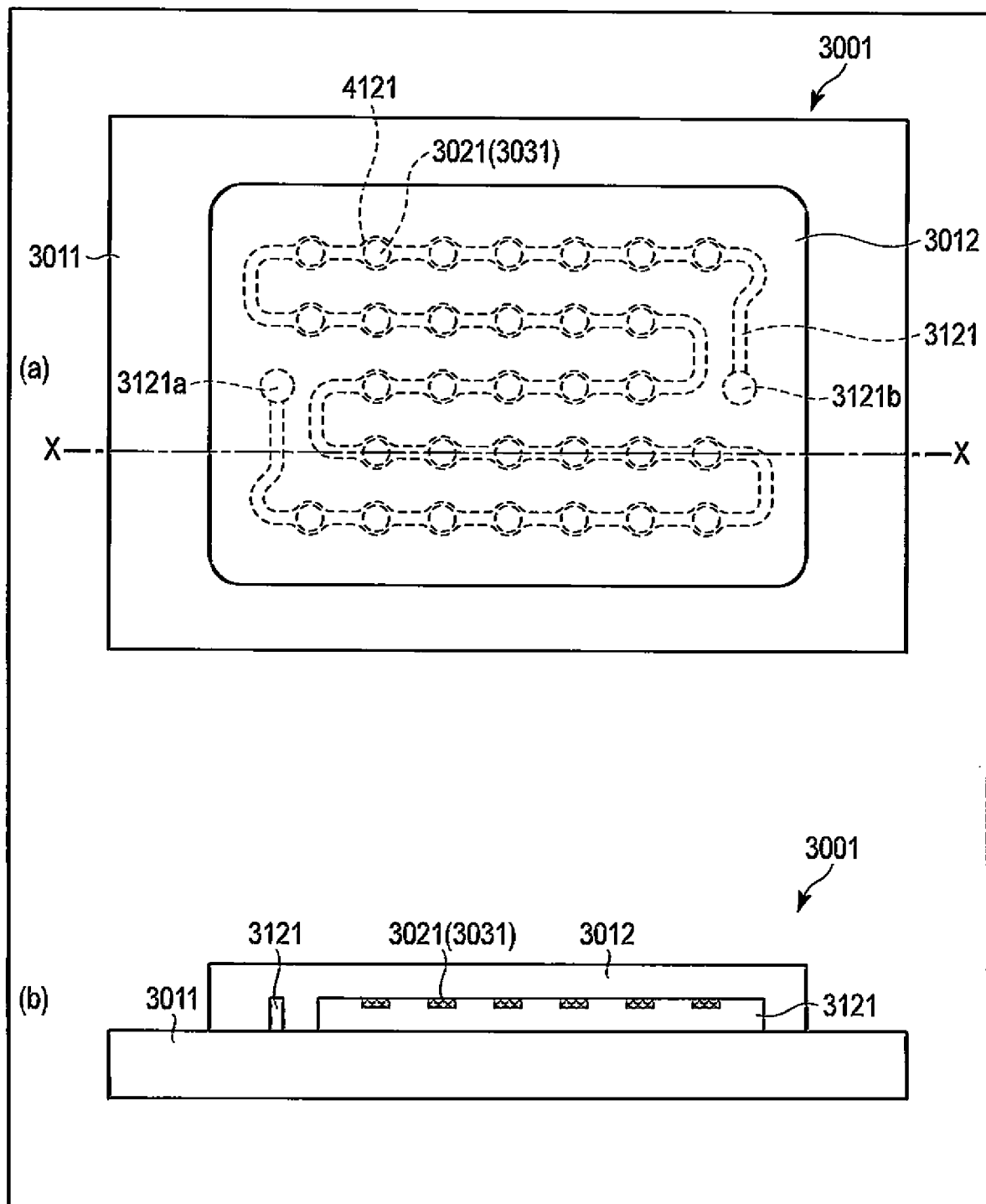


Figure 1 consists of two views of a semiconductor device 3001.
 (a) Plan view: The device 3001 is shown as a rectangular substrate. A central region 3011a contains a serpentine circuit 3121. The circuit has two main segments, 3121a and 3121b, which are connected at several points labeled 3032. A dashed line X-X indicates the cross-section. Below the central region is a grid-like structure 3112a.
 (b) Cross-sectional view: This view is taken along the line X-X. It shows the substrate 3011a and a layer 3021(3031) on top. The serpentine circuit 3012a is formed on the layer. The circuit has segments 3121 and 3111a, and connection points 3032. The connection points are labeled A, B, C, D, E, and NC.

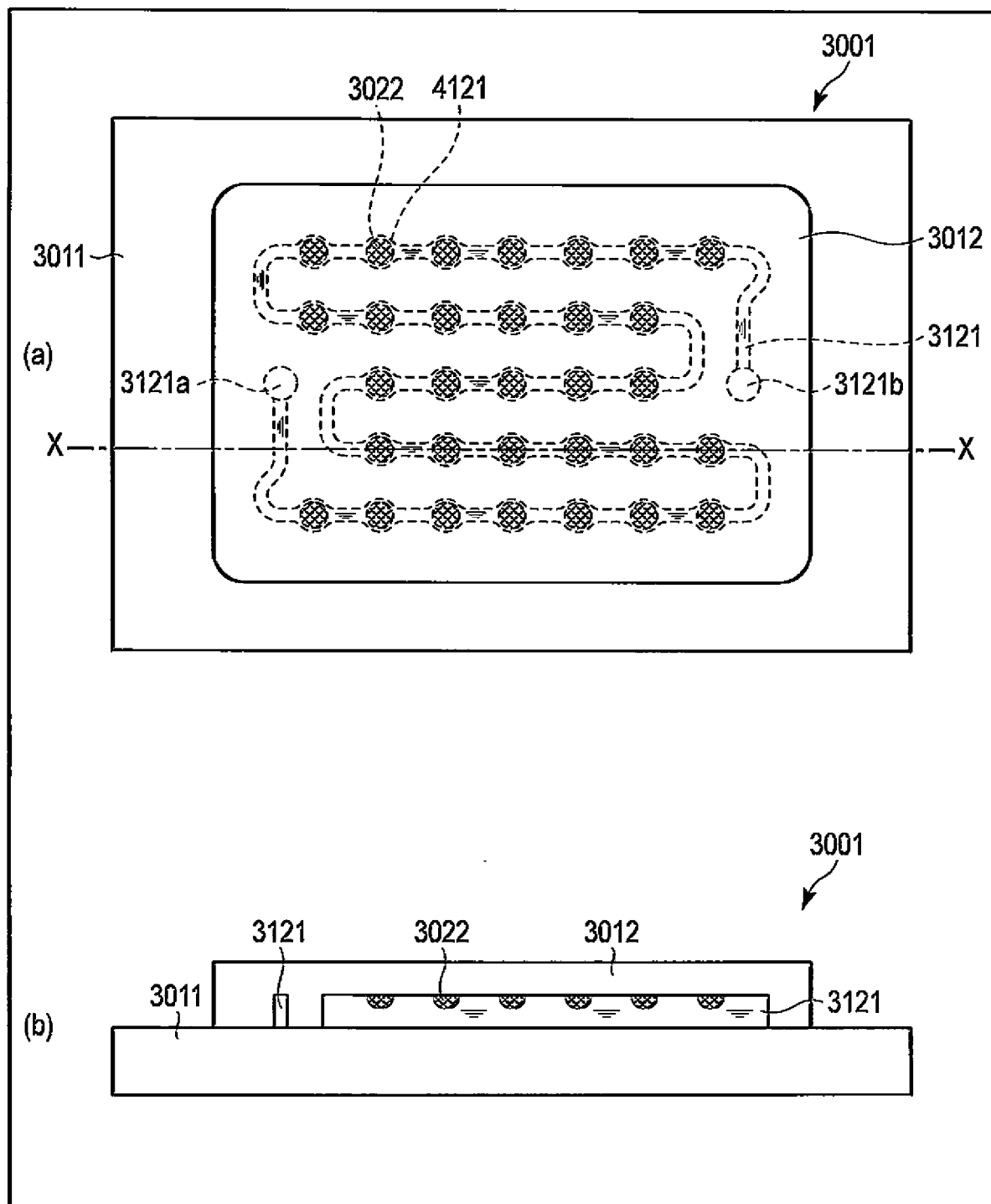
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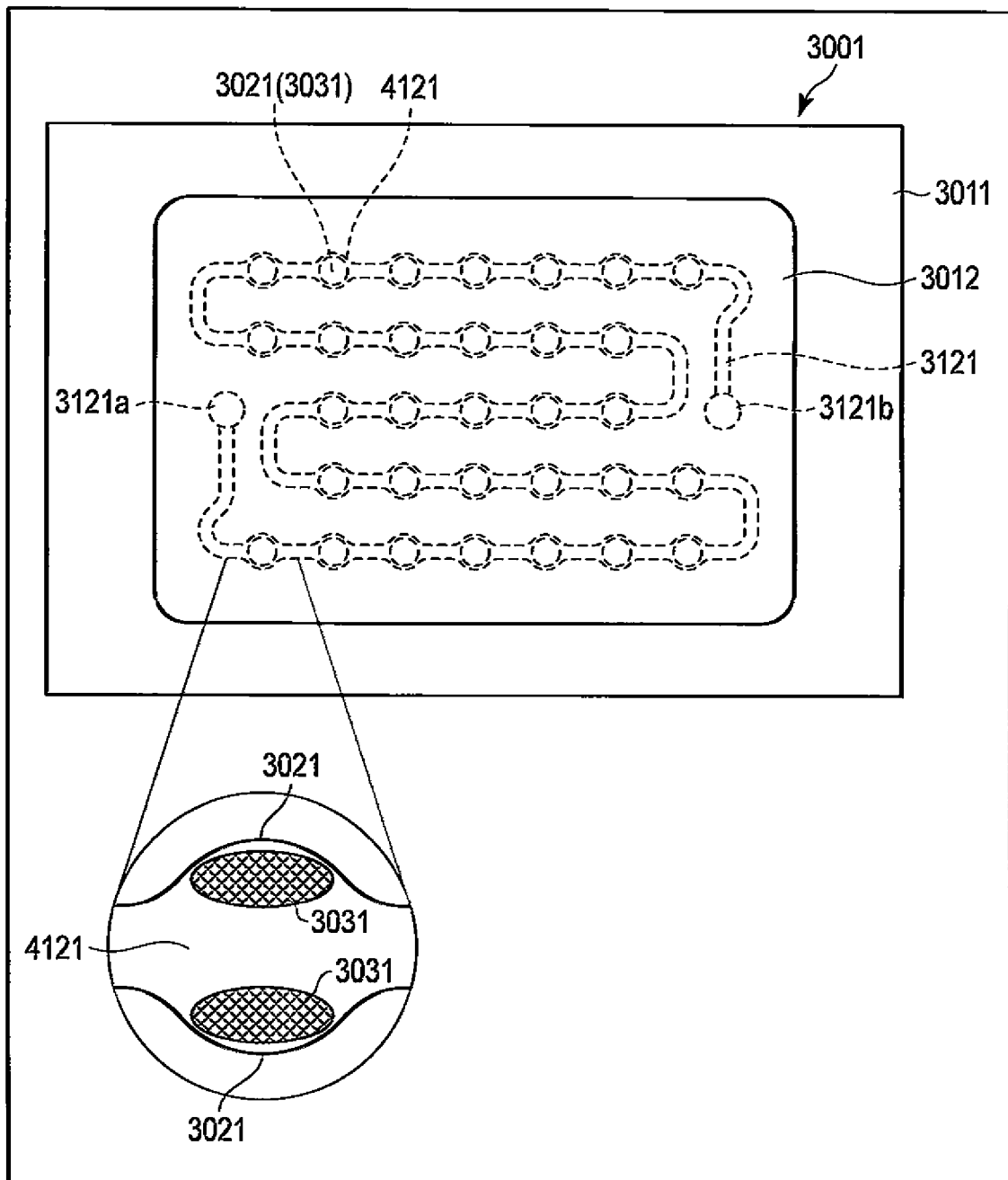
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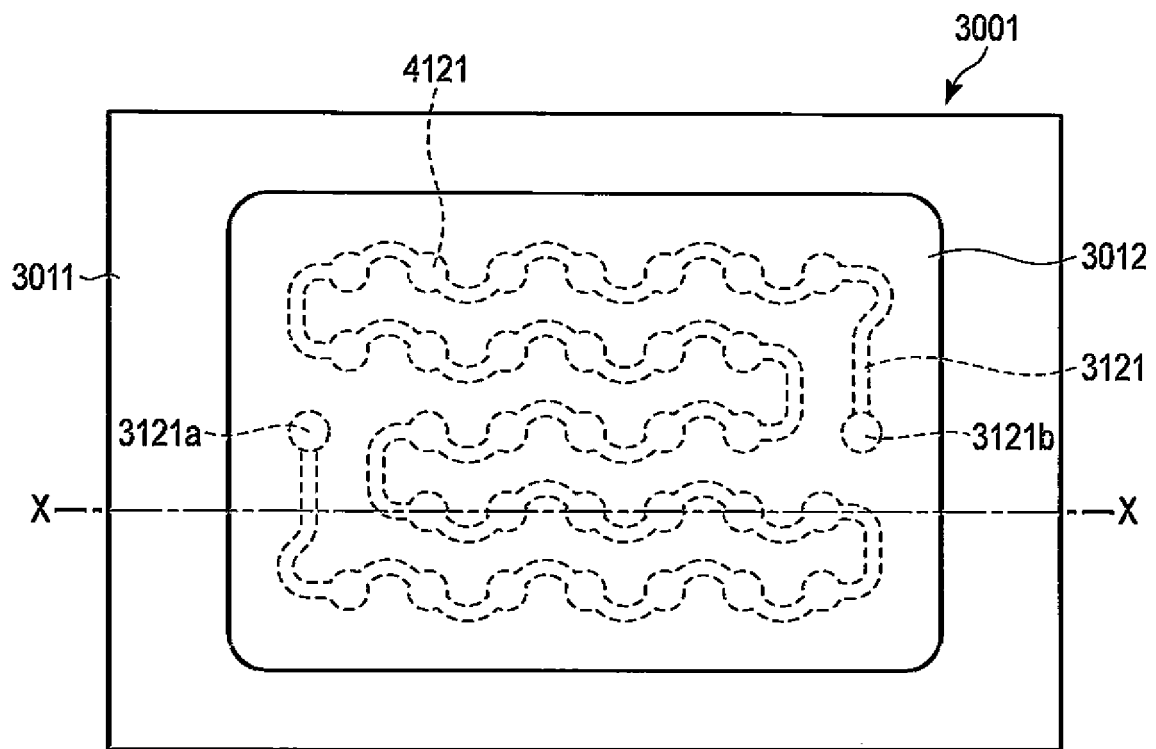
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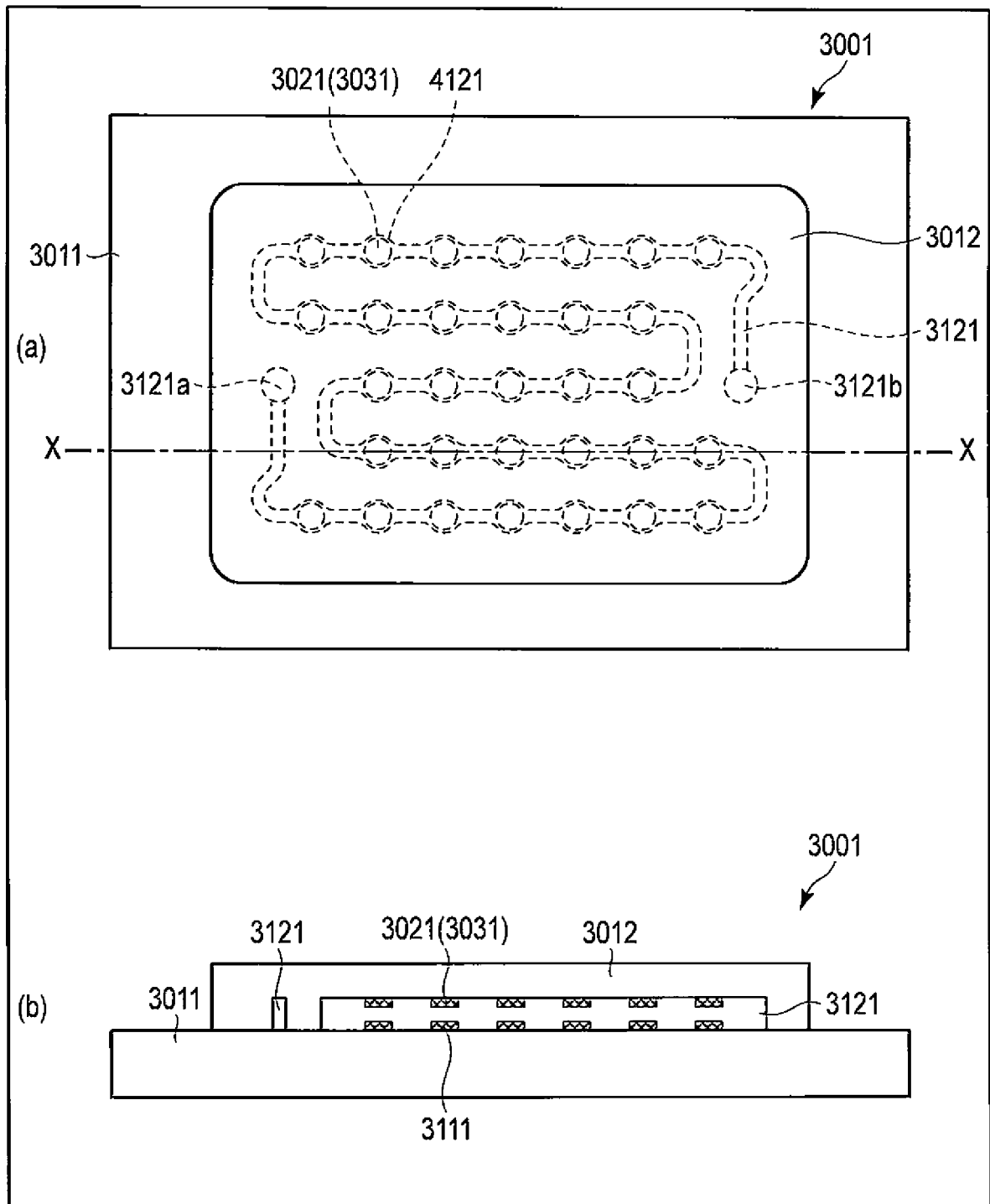
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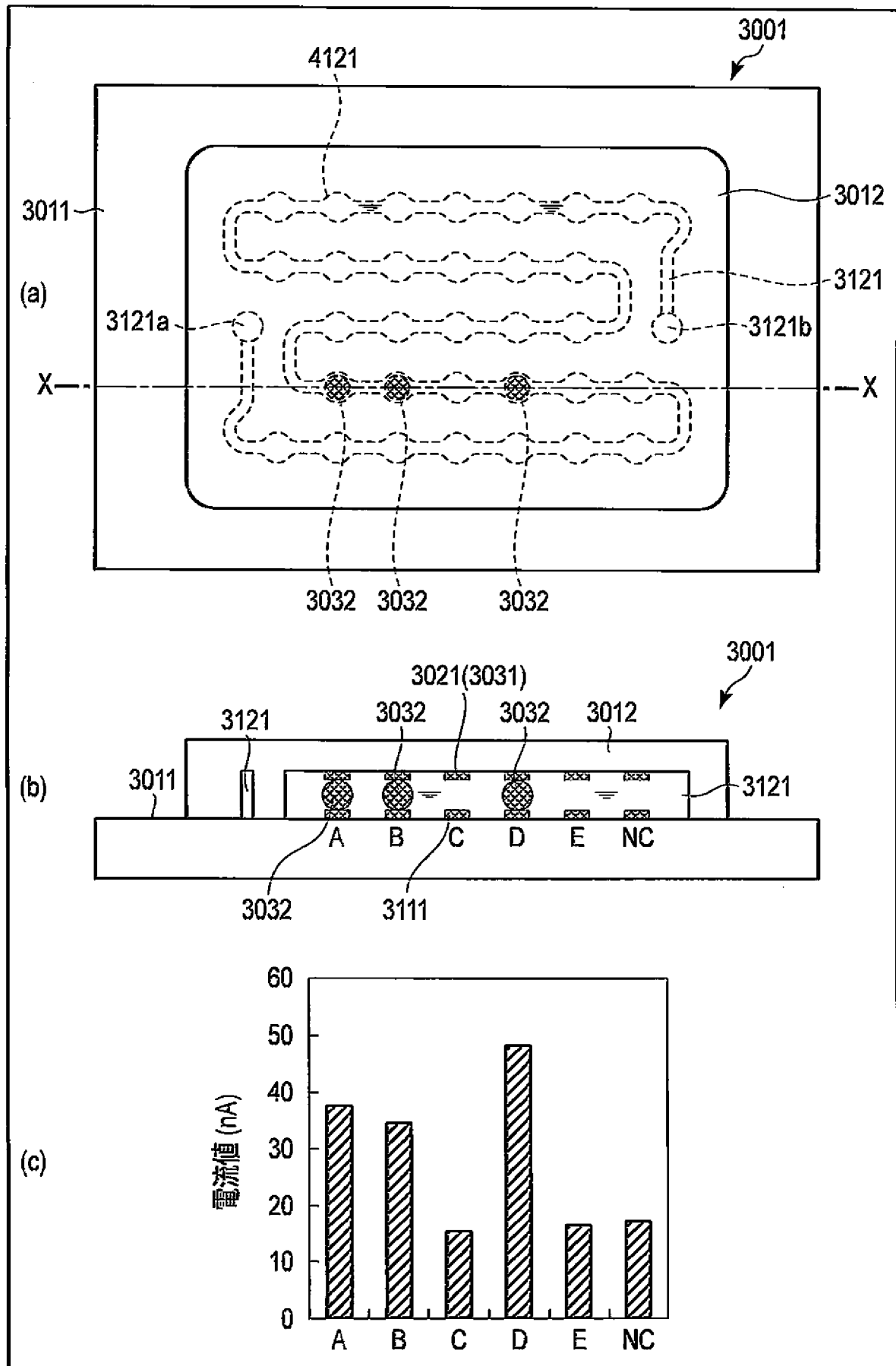
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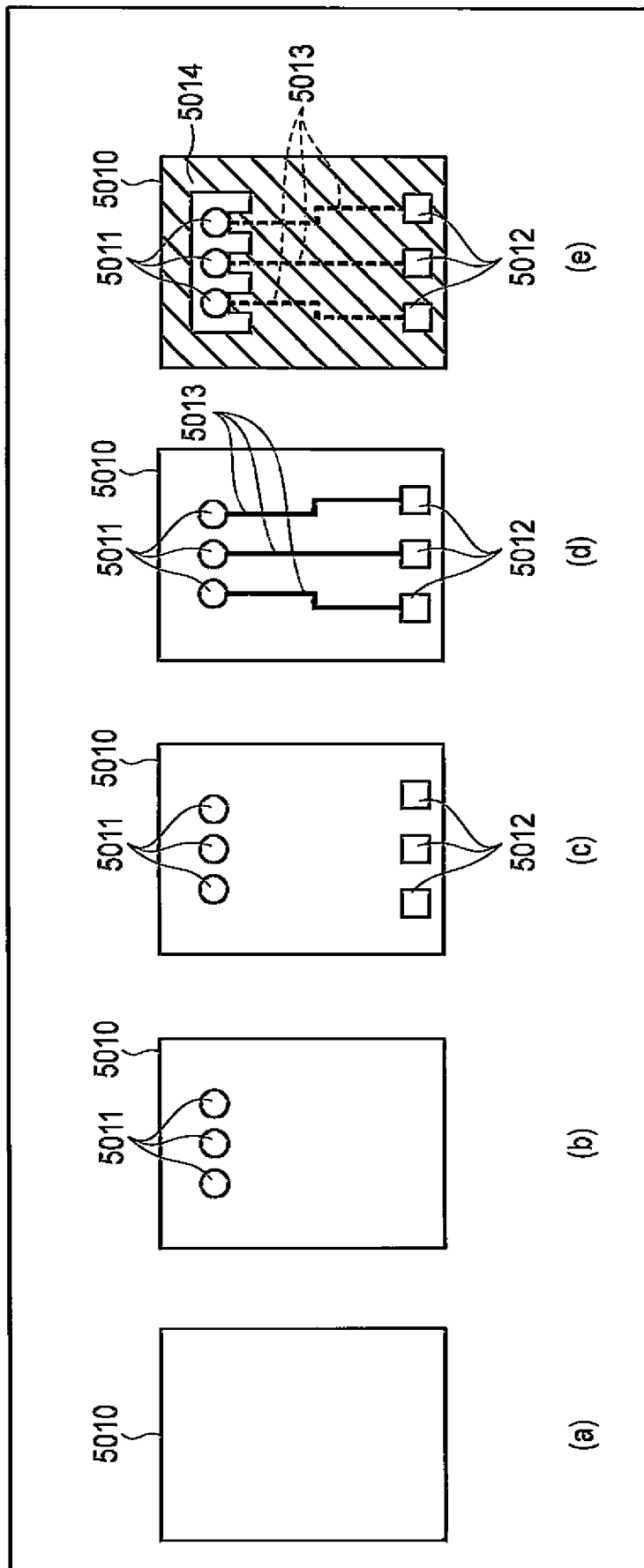
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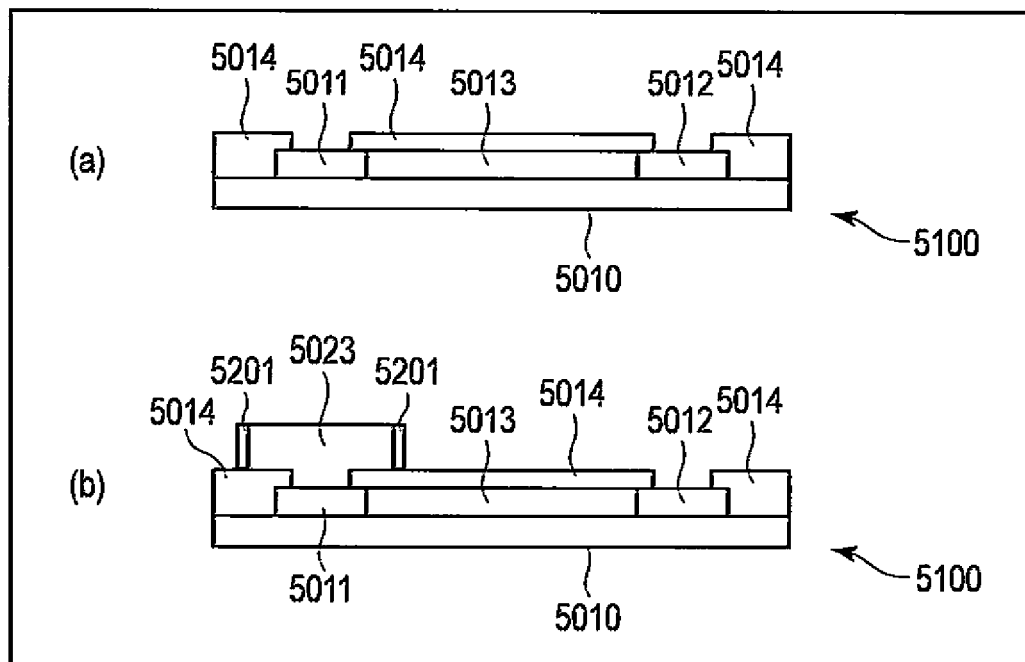
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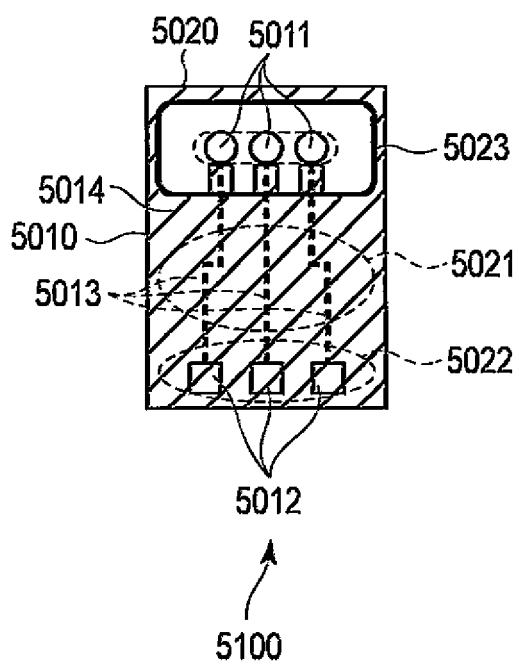
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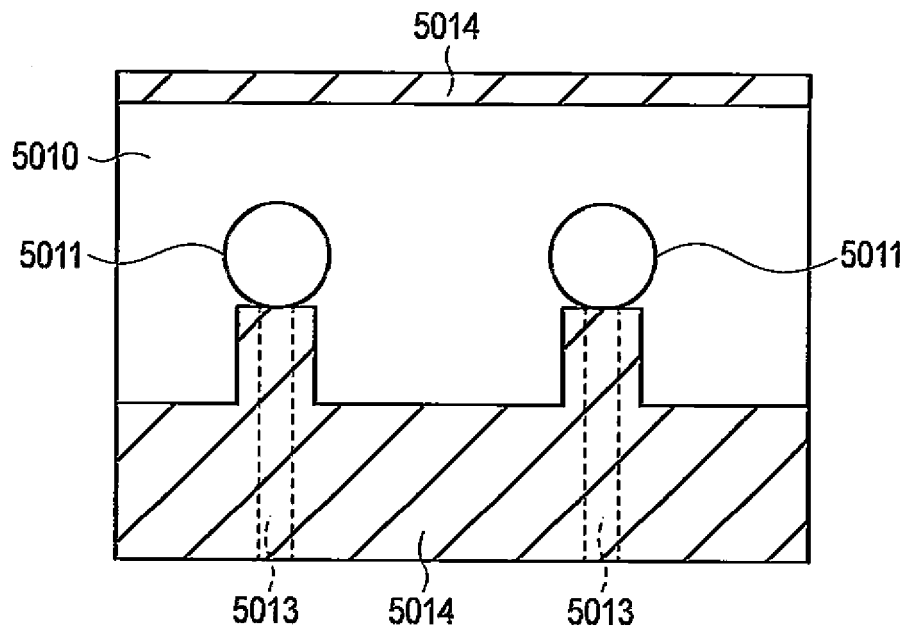
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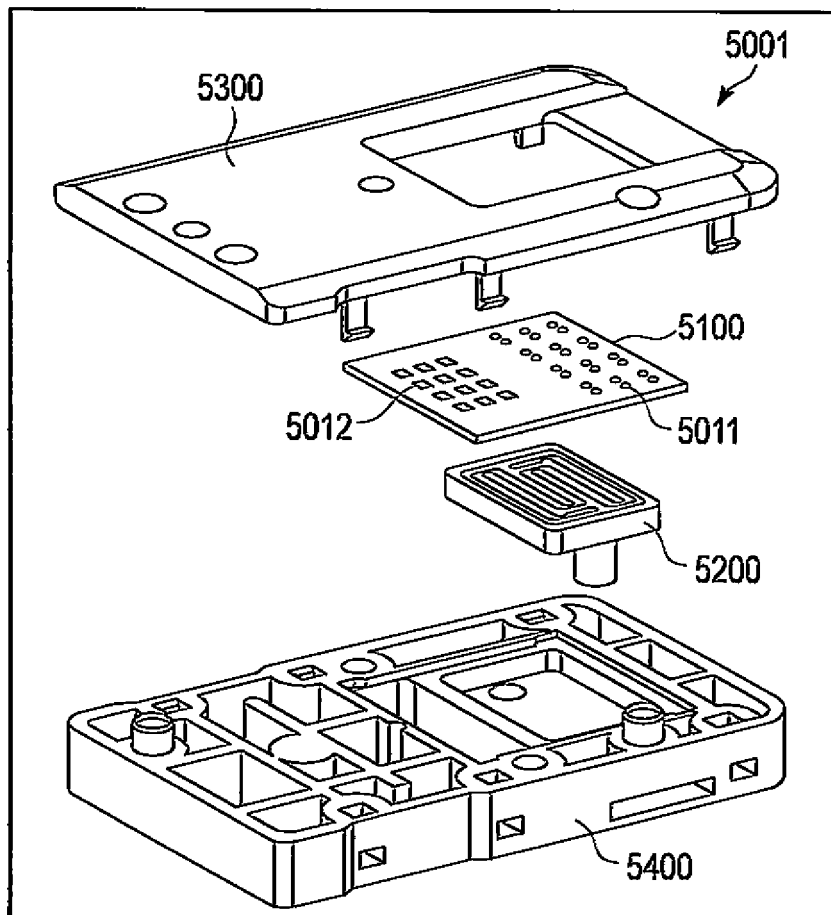
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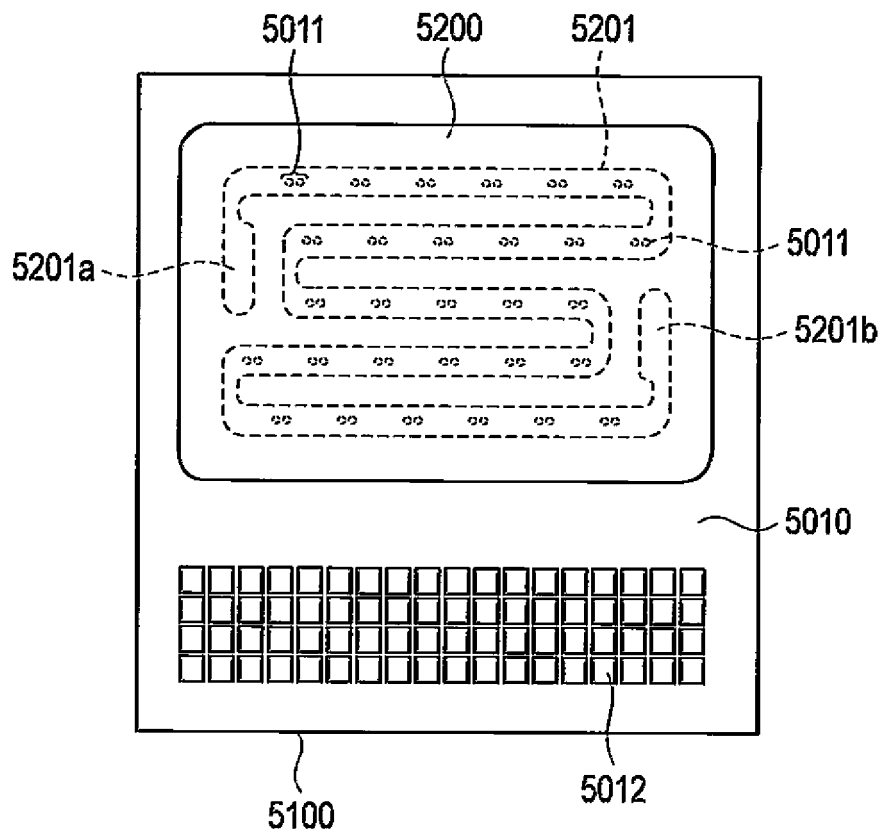
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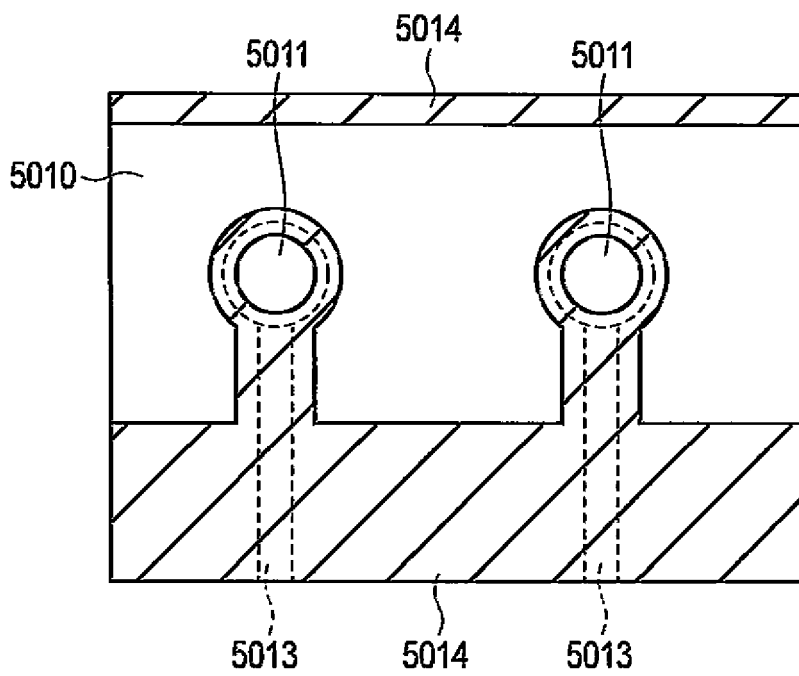
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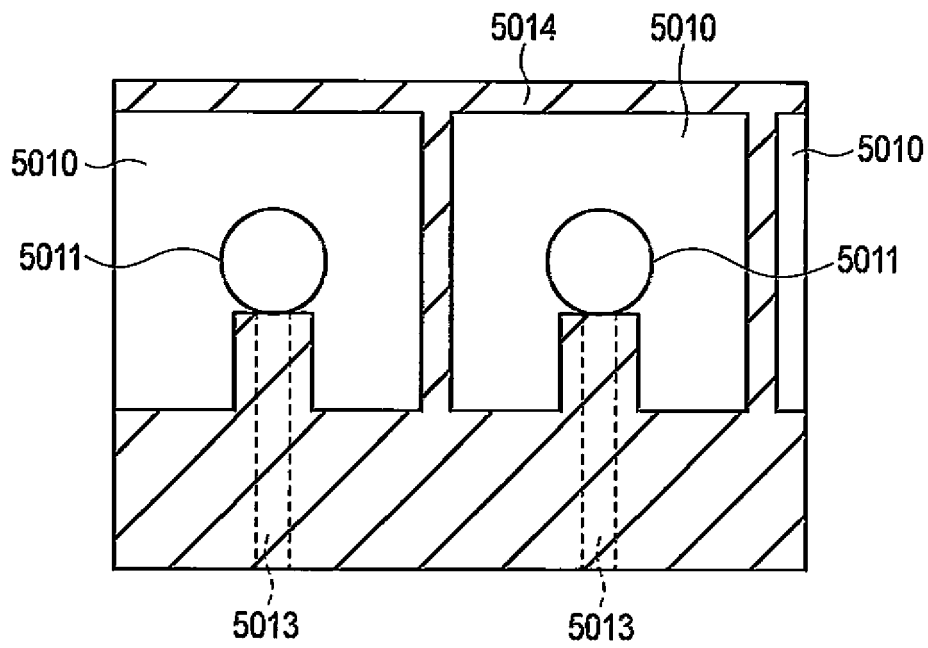
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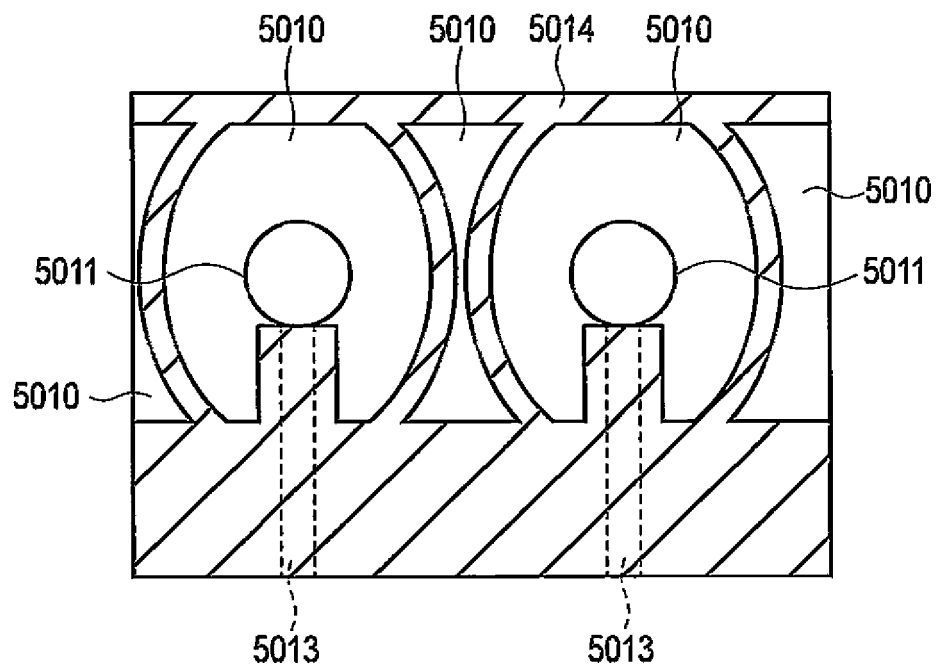
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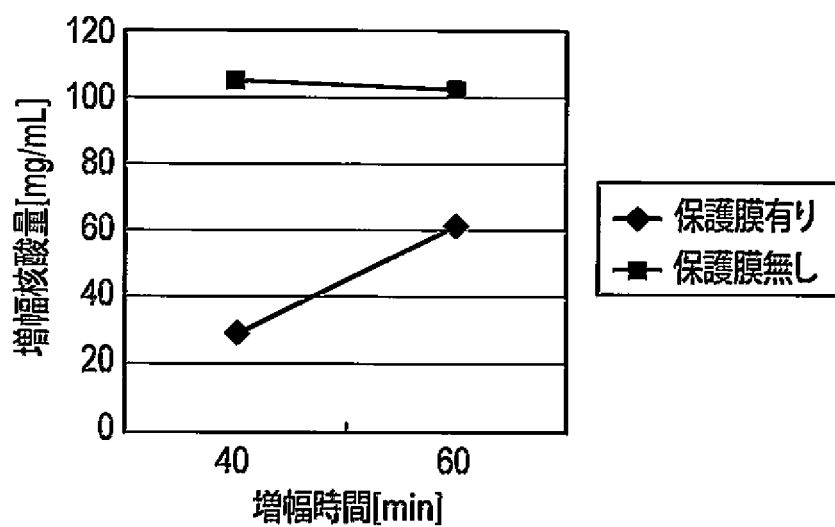
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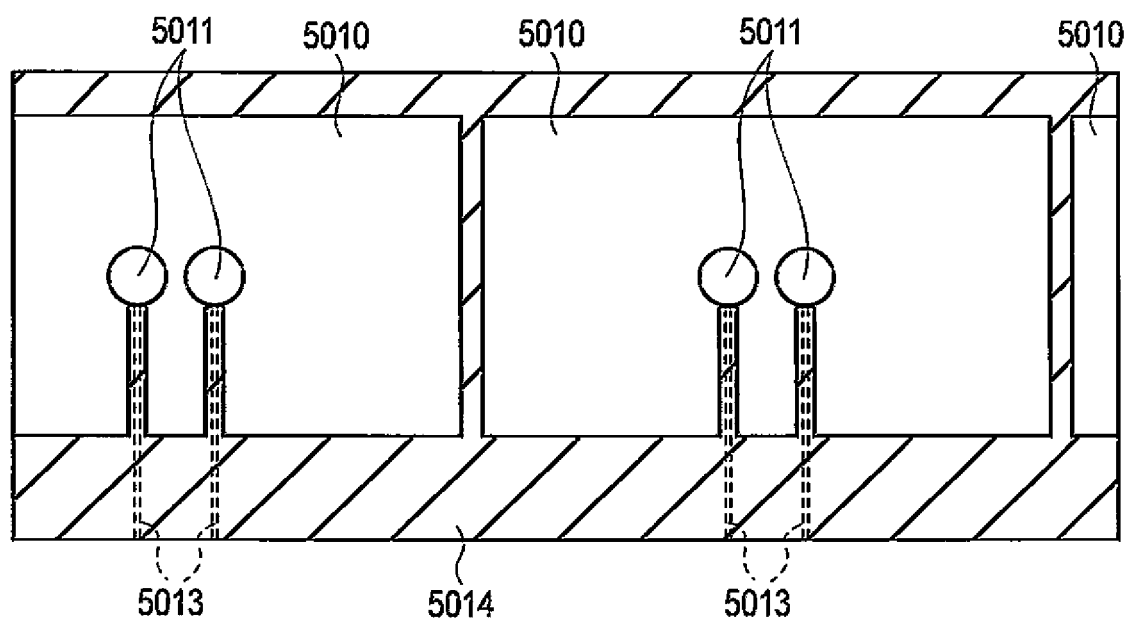
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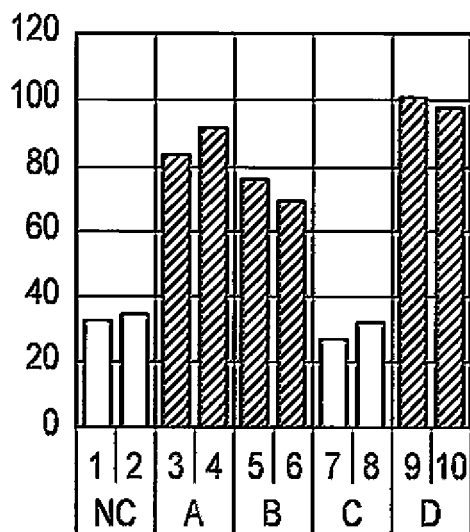
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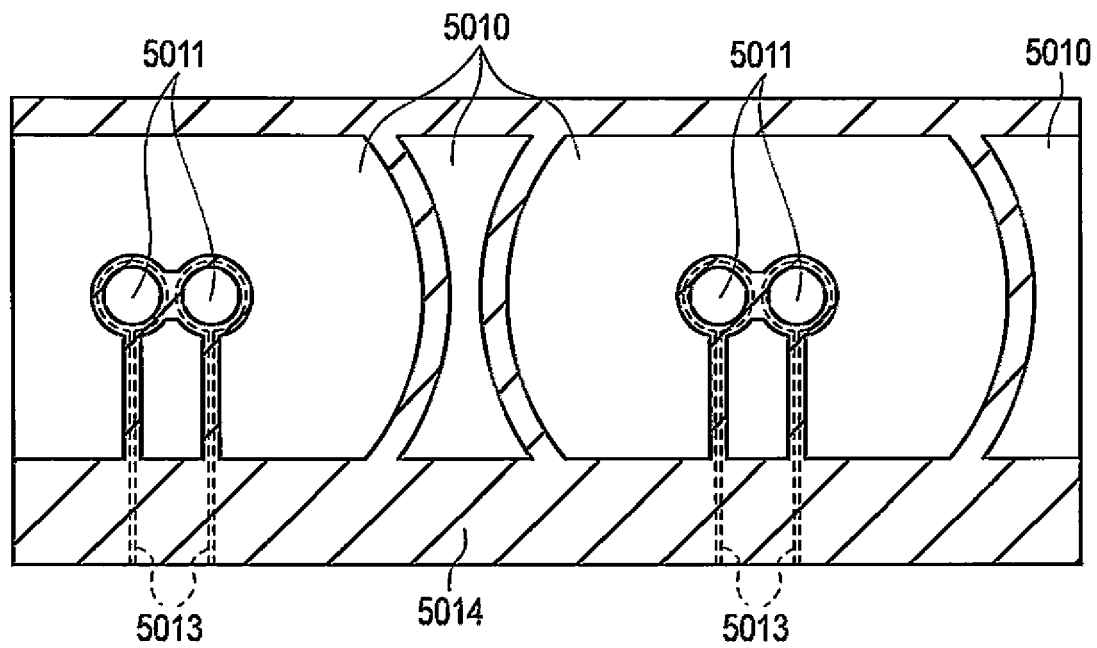
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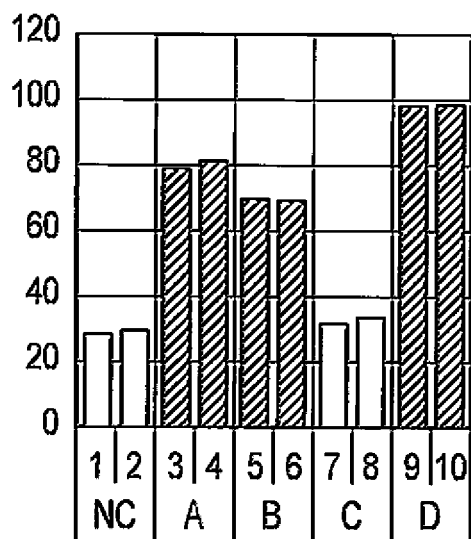
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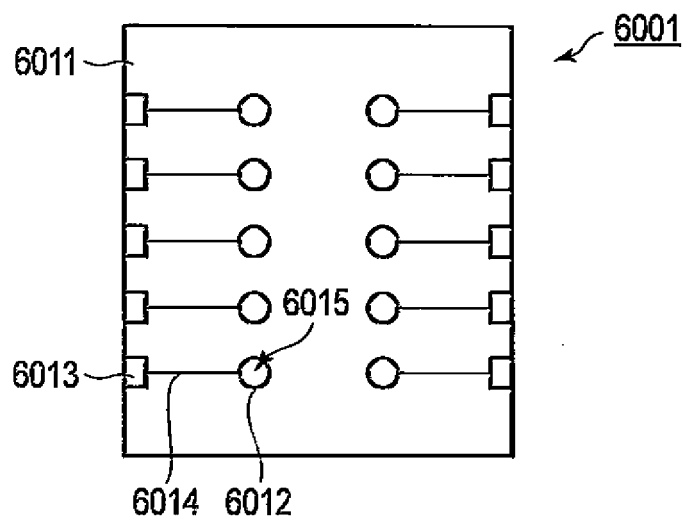
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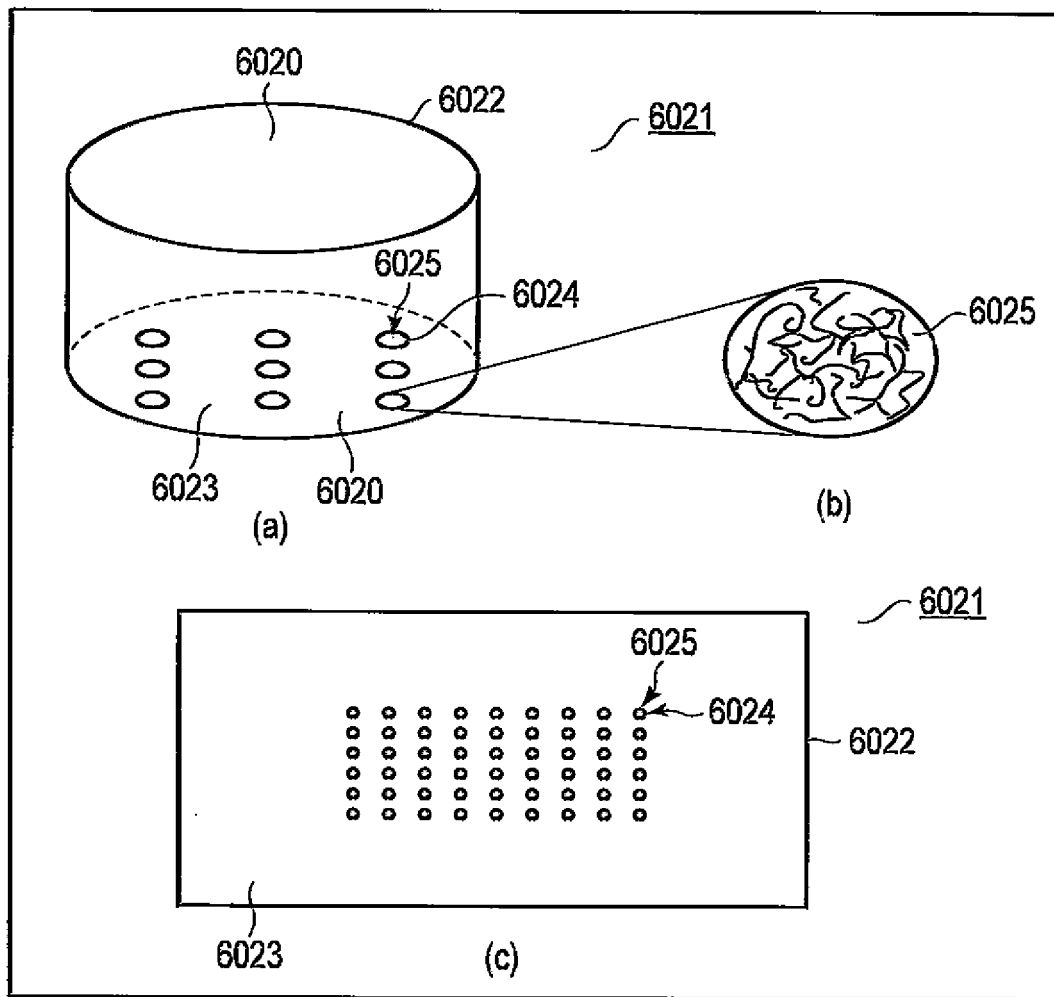
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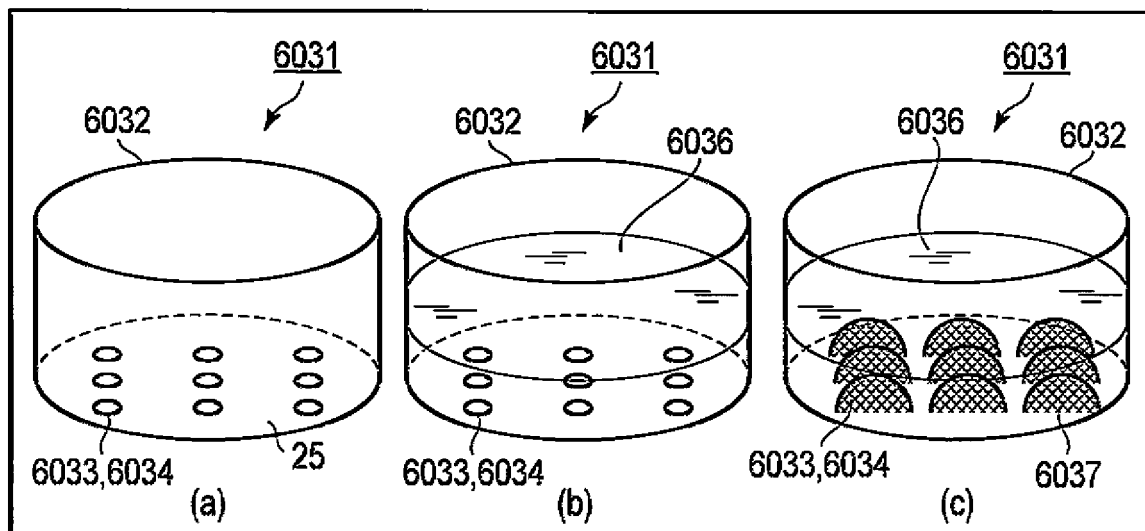
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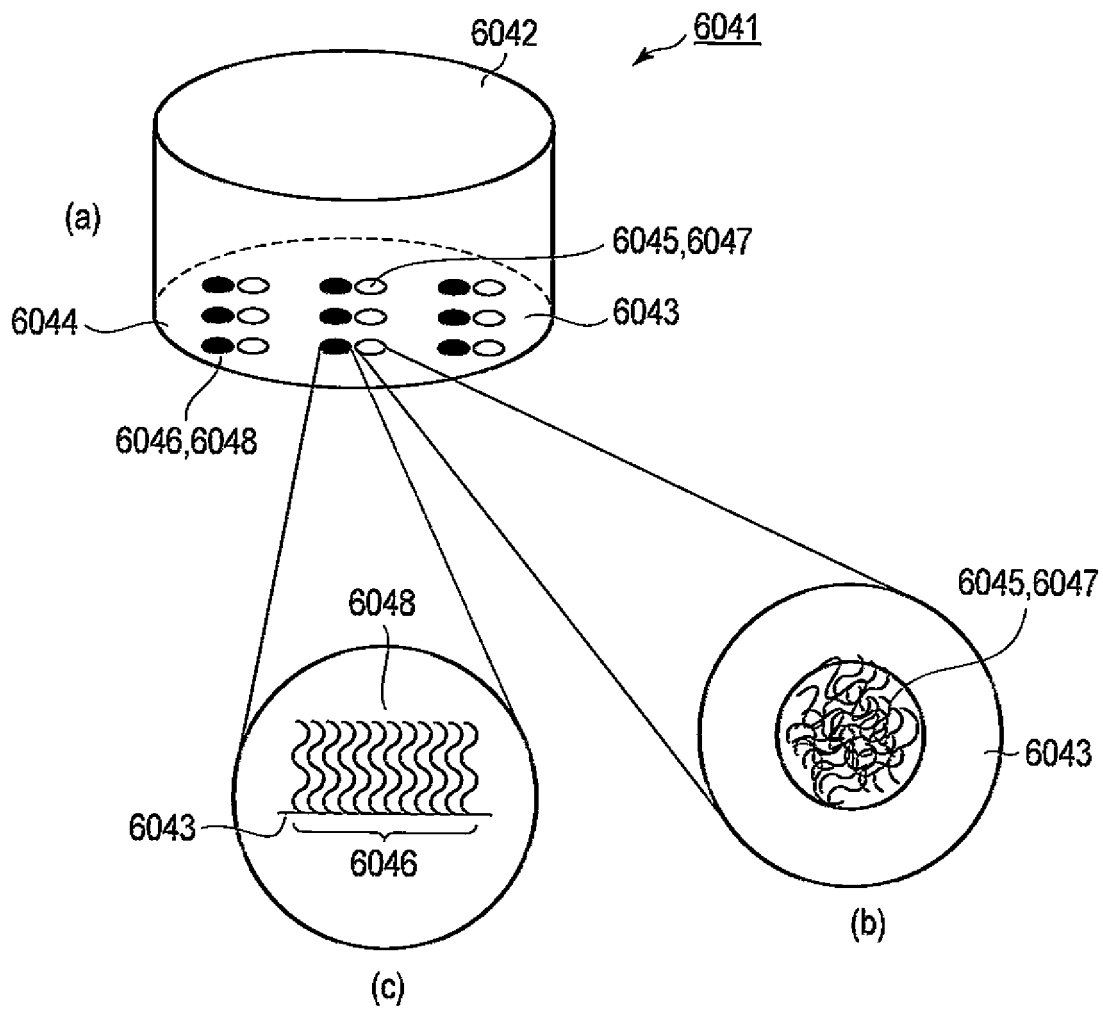
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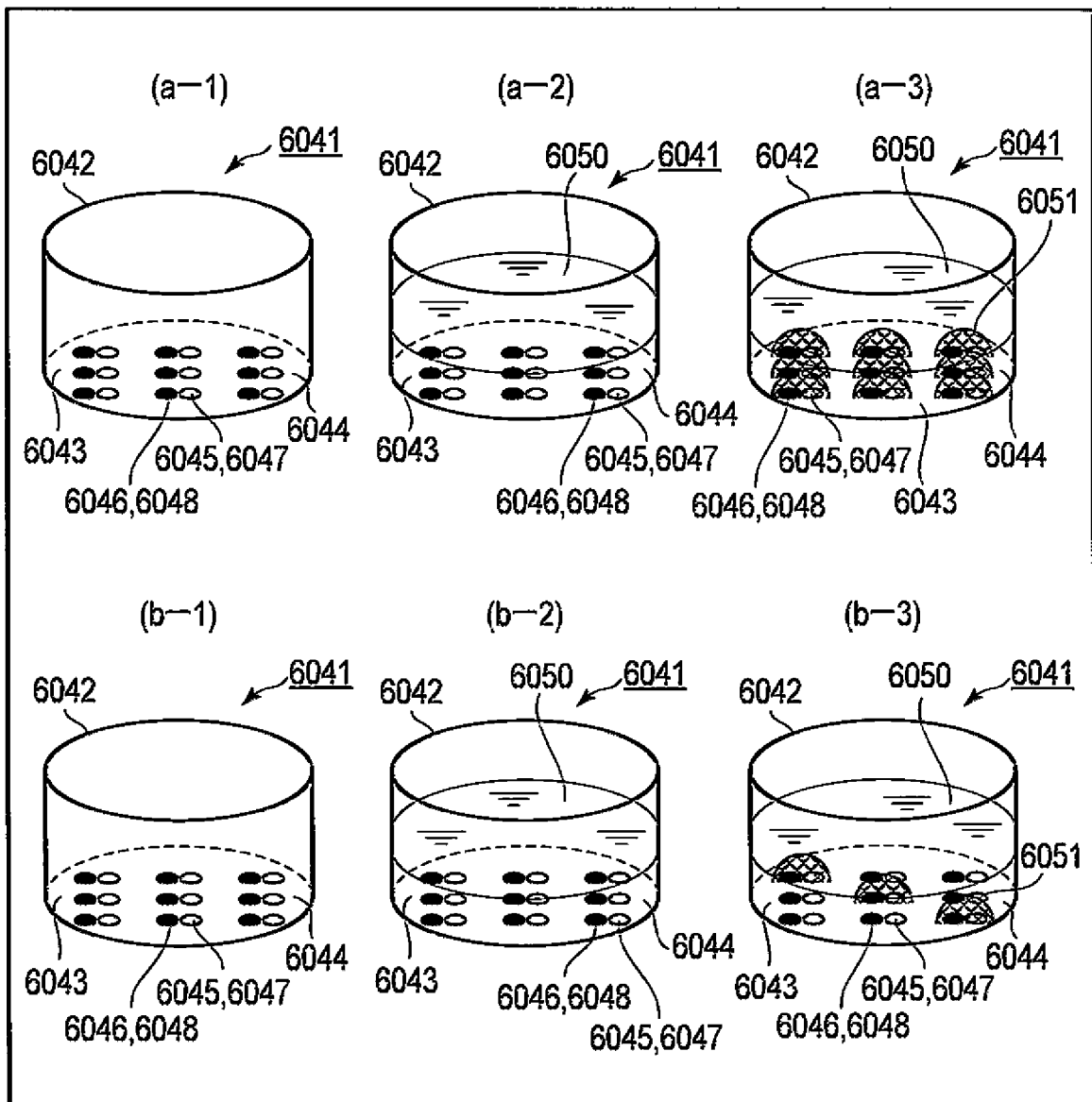
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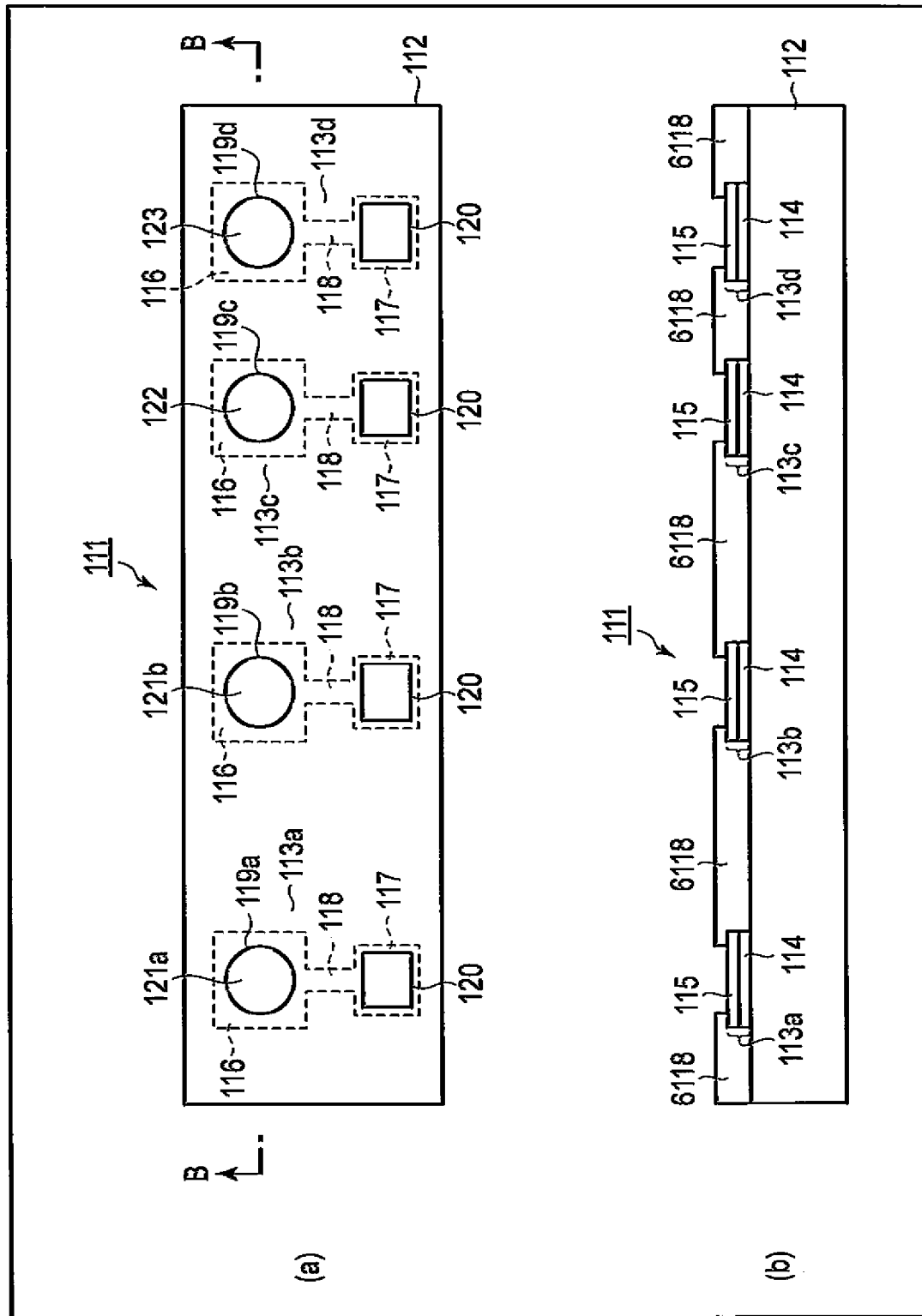
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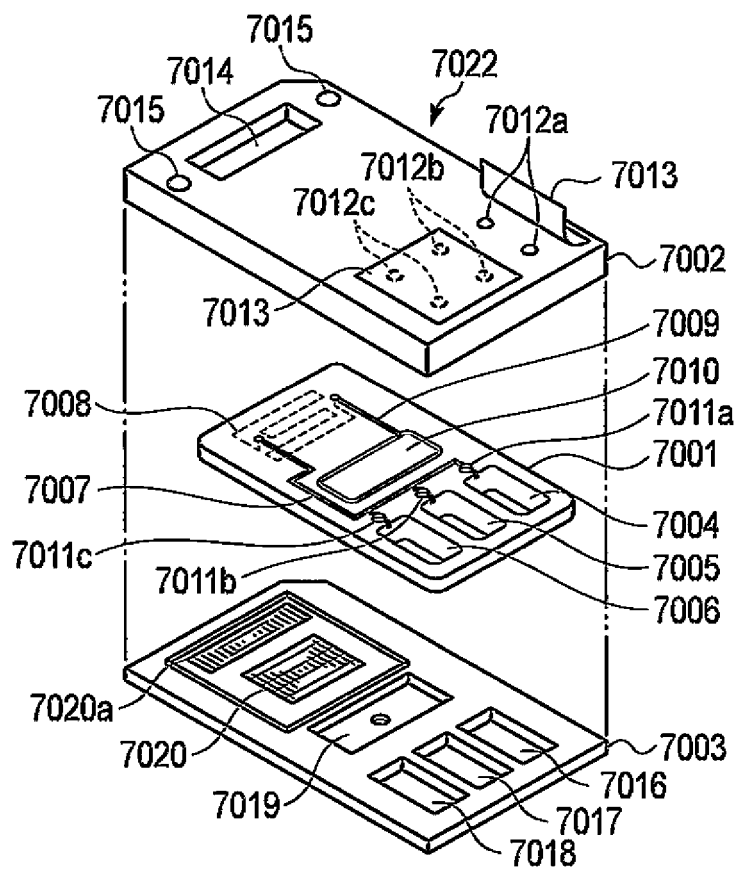
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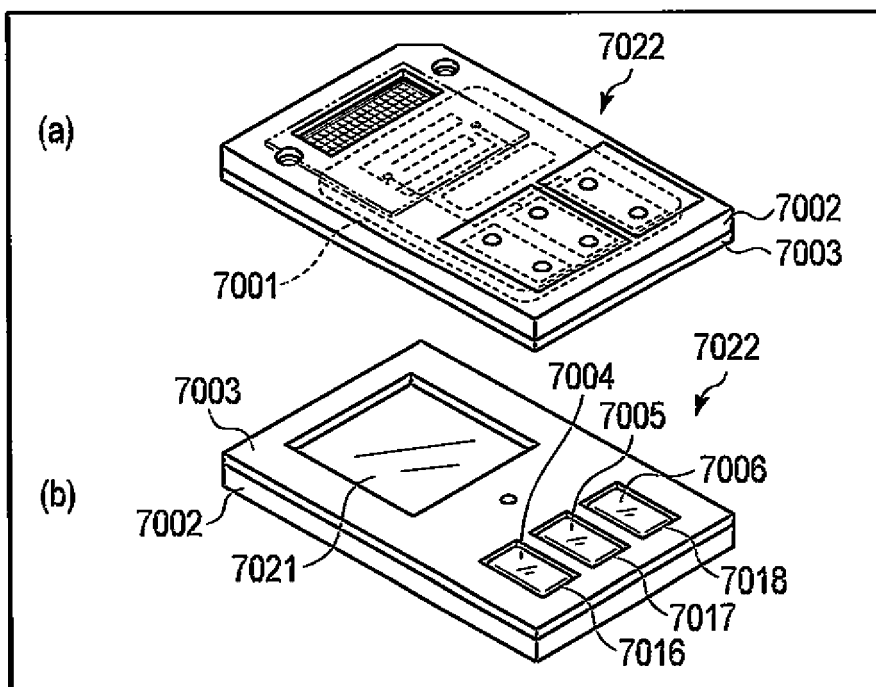
[図50]



[図54]



[図55]



[図56]

