PACKAGED MICROELECTRONIC DEVICES AND METHODS FOR MANUFACTURING PACKAGED MICROELECTRONIC DEVICES

TECHNICAL FIELD

[0001] The present disclosure is related to packaged microelectronic devices and methods for manufacturing packaged microelectronic devices.

BACKGROUND

[0002] Processors, memory devices, imagers and other types of microelectronic devices are often manufactured on semiconductor workpieces or other types of workpieces. In a typical application, several individual dies (e.g., devices) are fabricated on a single workpiece using sophisticated and expensive equipment and processes. Individual dies generally include an integrated circuit and a plurality of bond-pads coupled to the integrated circuit. The bond-pads provide external electrical contacts on the die through which supply voltage, signals, etc., are transmitted to and from the integrated circuit. The bond-pads are usually very small, and they are arranged in an array having a fine pitch between bond-pads. The dies can also be quite delicate. As a result, after fabrication, the dies are packaged to protect the dies and to connect the bond-pads to another array of larger terminals that is easier to connect to a printed circuit board.

[0003] Conventional processes for packaging dies include electrically coupling the bond-pads on the dies to an array of pins, ball-pads, or other types of electrical terminals, and then encapsulating the dies to protect them from environmental factors (e.g., moisture, particulates, static electricity, and physical impact). In one application, the

bond-pads are electrically connected to contacts on an interposer substrate that has an array of ball-pads. For example, Figure 1A schematically illustrates a conventional packaged microelectronic device 6 including a microelectronic die 10, an interposer substrate 60 attached to the die 10, a plurality of wire-bonds 90 electrically coupling the die 10 to the interposer substrate 60, and a casing 70 protecting the die 10 from environmental factors.

[0004] Electronic products require packaged microelectronic devices to have an extremely high density of components in a very limited space. For example, the space available for memory devices, imagers, processors, displays, and other microelectronic components is quite limited in cell phones, PDAs, portable computers, and many other products. As such, there is a strong drive to reduce the surface area or "footprint" of the microelectronic device 6 on a printed circuit board. Reducing the size of the microelectronic device 6 is difficult because high performance microelectronic dies 10 generally have more bond-pads, which result in larger ball-grid arrays and thus larger footprints. One technique used to increase the density of microelectronic dies 10 within a given footprint is to stack one microelectronic die on top of another.

[0005] Figure 1B schematically illustrates another conventional packaged microelectronic device 6a having two stacked microelectronic dies 10a-b. The microelectronic device 6a includes a substrate 60a, a first microelectronic die 10a attached to the substrate 60a, a spacer 30 attached to the first die 10a with a first adhesive 22a, and a second microelectronic die 10b attached to the spacer 30 with a second adhesive 22b. The spacer 30 is a precut section of a semiconductor wafer. One drawback of the packaged microelectronic device 6a illustrated in Figure 1B is that it is expensive to cut semiconductor wafers to form the spacer 30. Moreover, attaching the spacer 30 to the first and second microelectronic dies 10a-b requires additional equipment and steps in the packaging process.

[0006] To address these concerns, some conventional packaged microelectronic devices include an epoxy spacer, rather than a section of a semiconductor wafer, to space

apart the first and second microelectronic dies 10a and 10b. The epoxy spacer is formed by dispensing a discrete volume of epoxy onto the first die 10a and then pressing the second die 10b downward into the epoxy. One drawback of this method is that it is difficult to position the second die 10b parallel to the first die 10a. As a result, microelectronic devices formed with this method often have "die tilt" in which the distance between the first and second dies varies across the device. If the second die 10b is not parallel to the first die 10a, but rather includes a "high side," the wire-bonds on the high side may be exposed after encapsulation. Moreover, the "low side" of the second die may contact the wire-bonds electrically connecting the first die to the substrate. This can cause an electrical short that renders the device defective. Accordingly, there is a need to improve the process of packaging multiple dies in a single microelectronic device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figure 1A schematically illustrates a conventional packaged microelectronic device in accordance with the prior art.

[0008] Figure 1B schematically illustrates another conventional packaged microelectronic device in accordance with the prior art.

[0009] Figures 2-8 illustrate stages of a method of manufacturing a packaged microelectronic device in accordance with one embodiment of the disclosure.

[0010] Figure 2 is a schematic top plan view of a semiconductor workpiece.

[0011] Figure 3 is a schematic side cross-sectional view of a portion of the workpiece of Figure 2.

[0012] Figure 4 is a schematic side cross-sectional view of the portion of the semiconductor workpiece after forming an adhesive layer on the stand-off layer.

[0013] Figure 5 is a schematic side cross-sectional view of the portion of the semiconductor workpiece after removing sections of the stand-off and adhesive layers.

[0014] Figure 6 is a schematic side cross-sectional view of the portion of the semiconductor workpiece after inverting the workpiece and reattaching the workpiece to the support member.

[0015] Figure 7 is a schematic side cross-sectional view of a microelectronic device assembly including a lead frame, a microelectronic die attached to the lead frame, and a first singulated microelectronic device attached to the die.

[0016] Figure 8 is a schematic side cross-sectional view of the microelectronic device assembly after attaching a second singulated microelectronic device to the first singulated microelectronic device.

[0017] Figure 9 is a schematic side cross-sectional view of a packaged microelectronic device in accordance with another embodiment of the disclosure.

[0018] Figures 10 and 11 illustrate stages of a method of manufacturing a packaged microelectronic device in accordance with another embodiment of the disclosure.

[0019] Figure 10 is a schematic side cross-sectional view of a portion of a workpiece including a stand-off structure and first and second adhesive layers formed on the stand-off structure.

[0020] Figure 11 is a schematic side cross-sectional view of a packaged microelectronic device in accordance with another embodiment of the disclosure.

[0021] Figure 12 is a schematic illustration of a system in which the microelectronic devices may be incorporated.

DETAILED DESCRIPTION

[0022] Specific details of several embodiments are described below with reference to packaged microelectronic devices including two or three stacked microelectronic dies,

but in other embodiments the packaged microelectronic devices can have a different number of stacked dies and/or may include other components. For example, the microelectronic devices can include micromechanical components, data storage elements, optics, read/write components, or other features. The microelectronic dies can be SRAM, DRAM (e.g., DDR-SDRAM), flash-memory (e.g., NAND flash-memory), processors, imagers, and other types of devices. Moreover, several additional embodiments of the invention can have different configurations, components, or procedures than those described in this section. A person of ordinary skill in the art, therefore, will accordingly understand that the invention may have other embodiments with additional elements, or the invention may have other embodiments without several of the elements shown and described below with reference to Figures 2-12.

[0023] Figures 2-8 illustrate stages of a method of manufacturing a packaged microelectronic device in accordance with one embodiment of the disclosure. For example, Figure 2 is a schematic top plan view of a semiconductor workpiece 100, and Figure 3 is a schematic side cross-sectional view of a portion of the workpiece 100. The illustrated semiconductor workpiece 100 is a wafer 101 in and on which devices are constructed. Specifically, referring only to Figure 3, the workpiece 100 includes a substrate 102 and a plurality of microelectronic dies 110 (only three are shown) formed in and/or on the substrate 102. The individual dies 110 include an active side 112, a backside 114 opposite the active side 112, a plurality of terminals 116 (e.g., bond-pads) arranged in an array on the active side 112, and an integrated circuit 118 (shown schematically) operably coupled to the terminals 116. Although the illustrated dies 110 have the same structure, in other embodiments the dies may have different features to perform different functions.

[0024] After constructing the microelectronic dies 110, a stand-off layer 120 is formed across the semiconductor workpiece 100 at the backsides 114 of the dies 110. The stand-off layer 120 can be formed on the workpiece 100 by molding, spin-on techniques, film lamination, screen printing, spraying, brushing, a dip bath, or other

suitable processes. The stand-off layer 120 has a precise and generally uniform thickness and may be generally incompressible. For example, the stand-off layer 120 can be approximately 60 microns, but in other embodiments the stand-off layer 120 can have a thickness greater than or less than 60 microns. In several applications, the stand-off layer 120 can be made of a generally non-compressible material. The stand-off layer 120 may be composed of epoxy, epoxy acrylic, polyimide, or other suitable materials.

[0025] Figure 4 is a schematic side cross-sectional view of the portion of the semiconductor workpiece 100 after forming an adhesive layer 140 on the stand-off layer 120. The adhesive layer 140 can be a die attach film or other suitable member for connecting the dies 110 to other dies as described below. The combination of the stand-off and adhesive layers 120 and 140 has a precise thickness T within the range of the desired distance between pairs of stacked microelectronic dies in a packaged microelectronic device as described in greater detail below. In other embodiments, the workpiece 100 may not include the adhesive layer 140. In either case, the semiconductor workpiece 100 can be removably attached to a support member 190 during several processing procedures to provide support to the workpiece 100. The support member 190 may include a dicing support having an annular frame 192 carrying a replaceable film 194 that can include an attachment device 196 (e.g., UV tape) for releasably adhering the support member 190 to the active side 112 of the dies 110.

[0026] Figure 5 is a schematic side cross-sectional view of the portion of the semiconductor workpiece 100 after removing sections of the stand-off and adhesive layers 120 and 140 to form a plurality of discrete stand-offs 130 with adhesive sections 142 on corresponding dies 110. Sections of the stand-off and adhesive layers 120 and 140 can be removed via etching, cutting (e.g., with a wafer saw or dicing blade), or other suitable methods. In other embodiments, the stand-off and/or adhesive layer 120 and/or 140 can be composed of a photoactive material, and sections of these layers 120 and/or 140 can be exposed and developed to form the stand-offs 130. In either case, the individual stand-offs 130 include a first surface 132 facing a corresponding die 110, a

second surface 134 opposite the first surface 132, and a plurality of ends 136 extending between the first and second surfaces 132 and 134. The first surfaces 132 are attached to corresponding dies 110 without an adhesive because the stand-offs 130 themselves adhere to the dies 110. The second surfaces 134 are generally planar and oriented parallel to the backsides 114 of the dies 110. The ends 136 are spaced apart so that the illustrated stand-offs 130 are positioned inboard the terminals 116 (i.e., between the terminals 116 and the center of the particular die 110) and over the central portion of the corresponding dies 110. Although in the illustrated embodiment the stand-offs 130 have a rectangular cross-sectional shape and are positioned on the dies 110 in a one-to-one correspondence, in other embodiments the stand-offs can have other cross-sectional shapes and/or a plurality of stand-offs can be formed on each die 110. In either case, the position of the stand-offs 130 is driven by the configuration of the dies to which the particular stand-offs 130 are attached. The individual adhesive sections 142 include a first surface 144 facing the second surface 134 of the corresponding stand-off 130 and a second surface 146 opposite the first surface 144. The second surfaces 146 are generally planar and oriented parallel to the backsides 114 of the dies 110.

[0027] Figure 6 is a schematic side cross-sectional view of the portion of the semiconductor workpiece 100 after inverting the workpiece 100 and reattaching the workpiece 100 to the support member 190 with the stand-offs 130 positioned between the dies 110 and the support member 190. Specifically, the workpiece 100 is removably attached to the support member 190 with the second surface 146 of the adhesive sections 142 contacting the attachment device 196 (e.g., UV tape). The workpiece 100 is then cut along lines A-A to singulate a plurality of microelectronic devices 104. The individual microelectronic devices 104 can be removed from the support member 190 via a conventional pick-and-place apparatus.

[0028] Figure 7 is a schematic side cross-sectional view of a microelectronic device assembly 103 including a support member or lead frame 150, a microelectronic die 110a attached to the lead frame 150, and a first singulated microelectronic device 104a

attached to the die 110a. For purposes of brevity and clarity, hereinafter the die 110a will be referred to as a first die 110a, and the die 110 of the first singulated microelectronic device 104a will be referred to as a second die 110b. The lead frame 150 includes (a) a die paddle 152 for carrying the first die 110a and the first singulated microelectronic device 104a, and (b) a plurality of leads 154 (only two are shown) for providing external electrical contacts. The first die 110a can be either generally similar to the second die 110b or have different features to perform different functions. For example, the illustrated first die 110a includes an active side 112, a backside 114 opposite the active side 112, a plurality of terminals 116 (e.g., bond-pads) arranged in an array on the active side 112, and an integrated circuit 118 (shown schematically) operably coupled to the terminals 116. The backside 114 of the first die 110a is attached to the die paddle 152 with an adhesive 148. After attaching the first die 110a to the die paddle 152, the terminals 116 can be electrically coupled to corresponding leads 154 with a plurality of first wire-bonds 160a.

[0029] After connecting the first die 110a to the lead frame 150, the first singulated microelectronic device 104a can be attached to the first die 110a with the stand-off 130 positioned between the first and second dies 110a and 110b. Specifically, the second surface 146 of the adhesive section 142 is placed against the active side 112 of the first die 110a such that the first microelectronic device 104a adheres to the first die 110a. In the illustrated embodiment, the stand-off 130 and adhesive section 142 are positioned inboard the terminals 116 of the first die 110a so as not to interfere with the first wire-bonds 160a. Moreover, the combined thickness T of the stand-off 130 and the adhesive section 142 is sized to space the first and second dies 110a-b apart by a sufficient distance so that the first wire-bonds 160a can electrically couple the first die 110a to the leads 154 without contacting the second die 110b. As such, the combined thickness T of the stand-off 130 and the adhesive section 142 is greater than a distance D that the first wire-bonds 160a project from the active surface 112 of the first die 110a. After attaching the first microelectronic device 104a to the first die 110a, the terminals 116 of the second

die 110b are electrically coupled to corresponding leads 154 with a plurality of second wire-bonds 160b.

[0030] Figure 8 is a schematic side cross-sectional view of the microelectronic device assembly 103 after attaching a second singulated microelectronic device 104b to the first singulated microelectronic device 104a. The second microelectronic device 104b can be attached to the first microelectronic device 104a in generally the same manner as the first microelectronic device 104a is attached to the first die 110a. After attachment, the second microelectronic device 104b is electrically connected to corresponding leads 154 with a plurality of third wire-bonds 160c. In other embodiments, such as the embodiment described below with reference to Figure 9, the assembly 103 may not include the second microelectronic device 104b or the assembly 103 may include four or more microelectronic devices attached in a stacked configuration. In either case, a casing 170 is formed over the assembly 103 to encapsulate the first die 110a, the microelectronic devices 104, the wire-bonds 160, and a portion of the lead frame 150. The encased assembly 103 accordingly forms a packaged microelectronic device 103a.

[0031] Several embodiments of the method of manufacturing the packaged microelectronic device 103a illustrated in Figures 2-8 may enhance the quality and performance of the device 103a because the semiconductor fabrication processes can reliably produce and assemble the various components with a high degree of precision. For example, the stand-offs 130 and adhesive sections 142 can be formed with a precise, uniform thickness T so that the second and third microelectronic dies 110b-c are oriented generally parallel to the first microelectronic die 110a. As a result, the packaged microelectronic device 103a is expected to not have problems with die tilt and the concomitant exposure and/or shorting of wire-bonds. Moreover, the stand-offs 130 can be formed with relatively inexpensive materials, rather than expensive sections of a semiconductor wafer.

[0032] In one embodiment, a method of manufacturing a microelectronic device includes forming a stand-off layer over a plurality of microelectronic dies on a semiconductor workpiece, and removing selected portions of the stand-off layer to form a plurality of stand-offs. The individual stand-offs are positioned on a backside of a corresponding die. The method further includes cutting the semiconductor workpiece to singulate the dies, and attaching the stand-off on a first singulated die to a second die.

[0033] In another embodiment, a method includes forming a stand-off on a first microelectronic die, attaching a second microelectronic die to a support member, and coupling the stand-off to the second die. The stand-off is coupled to the second die after forming the stand-off on the first die and attaching the second die to the support member. The method further includes encapsulating the first and second dies and at least a portion of the support member.

[0034] In another embodiment, a method includes molding a stand-off structure, forming an adhesive layer on the stand-off structure, and cutting the stand-off structure to form a plurality of stand-offs. The method further includes attaching a first microelectronic die to a support member, coupling a first singulated stand-off to the first die, and connecting a second microelectronic die to the first singulated stand-off.

[0035] In another embodiment, a system comprises a microelectronic device including a support member and a first microelectronic die. The first die includes a backside attached to the support member, an active side opposite the backside, a plurality of terminals at the active side, and an integrated circuit operably coupled to the terminals. The device further includes a stand-off attached to the active side of the first die, and a second microelectronic die attached to the stand-off. The second die includes a backside, an active side opposite the backside, a plurality of terminals at the active side, and an integrated circuit operably coupled to the terminals. The backside of the second die is attached to the stand-off without an adhesive positioned between the stand-off and the backside of the second die.

[0036] In another embodiment, a semiconductor workpiece includes a substrate having a plurality of microelectronic dies. The individual dies include an active side, a backside opposite the active side, a plurality of terminals at the active side, and an integrated circuit operably coupled to the terminals. The workpiece further includes a plurality of stand-offs on the backsides of corresponding dies, and a plurality of adhesive sections attached to corresponding stand-offs.

[0037] In another embodiment, a microelectronic device includes a microelectronic die, a stand-off coupled to the die, and an exposed adhesive attached to the stand-off. The die includes an exposed active side, a backside opposite the active side, a plurality of terminals at the active side, and an integrated circuit operably coupled to the terminals. The stand-off is positioned at least partially inboard the terminals of the die and includes a first surface attached to the backside of the die and a second surface opposite the first surface. The exposed adhesive is placed on the second surface of the stand-off.

[0038] Figure 9 is a schematic side cross-sectional view of a packaged microelectronic device 203 in accordance with another embodiment of the disclosure. The packaged microelectronic device 203 is generally similar to the packaged microelectronic device 103a described above with reference to Figures 2-8. For example, the packaged microelectronic device 203 includes a first die 110a and a first microelectronic device 104a attached to the first die 110a. The illustrated packaged microelectronic device 203, however, does not include a second microelectronic device attached to the first microelectronic device 104a. Moreover, the support member of the illustrated packaged microelectronic device 203 includes an interposer substrate 250 in lieu of a lead frame. The interposer substrate 250 includes a first side 252 attached to the backside 114 of the first die 110a and a second side 253 opposite the first side 252. The first side 252 includes (a) a plurality of first contacts 254a arranged in arrays for attachment to corresponding first wire-bonds 160a, and (b) a plurality of second contacts 254 arranged in arrays for attachment to corresponding second wire-bonds 160b. The second side 253 includes (a) a plurality of first pads 256a electrically connected to

corresponding first contacts 254a with a plurality of first conductive traces 258a, and (b) a plurality of second pads 256b electrically connected to corresponding second contacts 254b with a plurality of second conductive traces 258b. The illustrated packaged microelectronic device 203 further includes a plurality of electrical couplers 280 (e.g., solder balls) attached to the first and second pads 256a-b.

[0039] Figures 10 and 11 illustrate stages of a method of manufacturing a packaged microelectronic device in accordance with another embodiment of the disclosure. For example, Figure 10 is a schematic side cross-sectional view of a portion of a workpiece 300 including a stand-off structure 320 and first and second adhesive layers 340a-b formed on the stand-off structure 320. The stand-off structure 320 has a circular, rectangular, or other suitable planform shape and includes a first major surface 322 and a second major surface 324 opposite the first major surface 322. The stand-off structure 320 includes a flowable dielectric material and can be formed via molding or other suitable methods. After forming the stand-off structure 320, the first adhesive layer 340a is placed on the first major surface 322 and the second adhesive layer 340b is placed on the second major surface 324. After attaching the adhesive layers 340, the workpiece 300 is cut along lines B-B to singulate a plurality of individual stand-offs 330 with corresponding adhesive sections 342a-b. In other embodiments, the workpiece 300 may not include one or both of the adhesive layers 340 such that one or both of the major surfaces 322 and 324 are exposed.

[0040] Figure 11 is a schematic side cross-sectional view of a packaged microelectronic device 303 in accordance with another embodiment of the disclosure. The packaged microelectronic device 303 is generally similar to the packaged microelectronic device 103a described above with reference to Figures 2-8. For example, the packaged microelectronic device 303 includes a lead frame 150, a first die 110a attached to the lead frame 150, and a second die 110b attached to the first die 110a. The illustrated packaged microelectronic device 303, however, further includes a first singulated stand-off 330 positioned between the first and second dies 110a-b with the

first adhesive section 342a attached to the active side 112 of the first die 110a and the second adhesive section 342b attached to the backside 114 of the second die 110b. In additional embodiments, the packaged microelectronic device 303 may include three or more microelectronic dies 110 attached in a stacked configuration. In other embodiments, the packaged microelectronic device 303 may include an interposer substrate in lieu of the lead frame 150.

[0041] Any one of the packaged microelectronic devices described above with reference to Figures 2-11 can be incorporated into any of a myriad of larger and/or more complex systems 490, a representative one of which is shown schematically in Figure 12. The system 490 can include a processor 491, a memory 492 (e.g., SRAM, DRAM, Flash, and/or other memory device), input/output devices 493, and/or other subsystems or components 494. Microelectronic devices may be included in any of the components shown in Figure 12. The resulting system 490 can perform any of a wide variety of computing, processing, storage, sensor, imagers, and/or other functions. Accordingly, representative systems 490 include, without limitation, computers and/or other data processors, for example, desktop computers, laptop computers, Internet appliances, hand-held devices (e.g., palm-top computers, wearable computers, cellular or mobile phones, personal digital assistants), multi-processor systems, processor-based or programmable consumer electronics, network computers, and mini computers. Other representative systems 490 include cameras, light or other radiation sensors, servers and associated server subsystems, display devices, and/or memory devices. In such systems, individual dies can include imager arrays, such as CMOS imagers. Components of the system 490 may be housed in a single unit or distributed over multiple, interconnected units, e.g., through a communications network. Components can accordingly include local and/or remote memory storage devices, and any of a wide variety of computer-readable media.

[0042] From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the invention. For example, many of

the elements of one embodiment can be combined with other embodiments in addition to or in lieu of the elements of the other embodiments. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

We claim:

1. A semiconductor workpiece, comprising:

a substrate including a plurality of microelectronic dies, the individual dies having an active side, a backside opposite the active side, a plurality of terminals at the active side, and an integrated circuit operably coupled to the terminals;

a plurality of stand-offs on the backsides of corresponding dies; and

a plurality of adhesive sections attached to corresponding stand-offs.

2. The semiconductor workpiece of claim 1 wherein the stand-offs are positioned at least partially inboard the terminals on the corresponding dies.

3. The semiconductor workpiece of claim 1 wherein the individual adhesive sections comprise a first surface attached to the corresponding stand-off and a second, exposed surface.

4. The semiconductor workpiece of claim 1 wherein adjacent stand-offs are spaced apart by a gap.

5. The semiconductor workpiece of claim 1 wherein the stand-offs are disposed on the backsides of corresponding dies without an adhesive positioned between the stand-offs and the dies.

6. The semiconductor workpiece of claim 1 wherein the individual stand-offs comprise a first surface attached to the corresponding die and a second, generally flat surface attached to the associated adhesive section and opposite the first surface.

7. A microelectronic device, comprising:

a microelectronic die including an exposed active side, a backside opposite the active side, a plurality of terminals at the active side, and an integrated circuit operably coupled to the terminals;

a stand-off coupled to the die and positioned at least partially inboard the terminals of the die, the stand-off including a first surface attached to the backside of the die and a second surface opposite the first surface; and

an exposed adhesive on the second surface of the stand-off.

8. The microelectronic device of claim 7 wherein the stand-off is attached directly to the backside of the die without an adhesive positioned between the stand-off and the die.

9. The microelectronic device of claim 7 wherein the stand-off comprises a molded dielectric material.

10. The microelectronic device of claim 7 wherein the stand-off has a generally uniform thickness.