CLAIMS

1. A semiconductor device comprising:

a substrate defined with a device region;

a buried heavily doped region in the substrate in the device region;

a gate in a trench in the device region, wherein a channel of the device is disposed on a sidewall of the trench, the buried heavily doped region is disposed below the gate and is vertically and laterally displaced away from the channel of the device, wherein a distance from the buried heavily doped region to the channel is a drift length L_D of the device; and

a surface heavily doped region adjacent to the gate.

2. The semiconductor device of claim 1 wherein the device region is surrounded by device isolation region.

3. The semiconductor device of claim 2 wherein the device region comprises one or more internal device regions, dividing the device region into multiple device sub-regions.

4. The semiconductor device of claim 1 wherein the device region comprises:

a first device doped well; and

a second device doped well, the second device doped well has a depth equals to a channel length L_C of the channel,

wherein the first device doped well has a depth greater than the second device doped well.

5. The semiconductor device of claim 4 wherein the first device doped well comprises first polarity type dopants and the second device doped well comprises second polarity type dopants.

6. The semiconductor device of claim 5 wherein the second device doped well is disposed substantially within the first device doped well.

7. The semiconductor device of 6 wherein:

the trench is disposed in the first and second device doped wells and the trench comprises first and second portions.

8. The semiconductor device of claim 7 comprising:

a drain connector disposed in the trench;

gate insulators disposed on either sides of the drain connector in the first portion of the trench; and

gate electrodes on either sides of the gate insulators in the first portion of the trench.

9. The semiconductor device of claim 8 wherein:

the first portion of the trench has a depth greater than an interface of the first and second device doped wells; and comprising

a gate dielectric layer which lines sidewalls and bottom of the first portion of the trench without lining sidewalls of the drain connector.

10. The semiconductor device of claim 8 wherein each of the gate insulators include a primary gate insulator and a secondary gate insulator which comprise different materials.

11. A semiconductor device comprising:

a substrate defined with a device region;

first and second device doped wells in the device region, wherein the first device doped well has a depth greater than the second device doped well;

a buried heavily doped region within the first device doped well;

a gate in a trench in the device region, wherein a channel of the device is disposed on a sidewall of the trench, the buried heavily doped region is disposed below the gate and is vertically and laterally displaced away from the gate and channel of the device, wherein a distance from the buried heavily doped region to the channel is a drift length L_D of the device; and

a surface heavily doped region adjacent to the gate.

12. The semiconductor device of claim 11 wherein the second device doped well has a depth equals to a channel length L_C of the channel.

13. The semiconductor device of claim 11 wherein the first device doped well comprises first polarity type dopants and the second device doped well comprises second polarity type dopants and the first and second device doped wells comprise dopant concentration lesser than the buried and surface heavily doped regions.

14. The semiconductor device of claim 11 comprising:

a drain connector disposed in the trench, wherein the drain connector is disposed adjacent to the gate and extends from a top surface of the substrate to the buried heavily doped region.

15. The semiconductor of claim 14 wherein the drain connector directly contacts the buried heavily doped region.

~~16. The semiconductor device of claim 15 wherein the buried heavily doped region is~~ disposed directly below the drain connector and occupies a portion of the first device doped well.

17. The semiconductor device of claim 14 comprising:

gate insulators disposed on either sides of the drain connector in the trench; and

gate electrodes on either sides of the gate insulators in the trench.

18. The semiconductor device of claim 17 wherein each of the gate insulators include a primary gate insulator and a secondary gate insulator which comprise different materials.

19. The semiconductor device of claim 14 wherein:

the trench has a depth greater than an interface of the first and second device doped wells; and comprising

a gate dielectric layer which lines sidewalls and bottom of the trench without lining sidewalls of the drain connector.

20. The semiconductor device of claim 19 wherein the gate dielectric layer comprises the same thickness.

CLAIMS

1. A semiconductor device comprising:

a substrate defined with a device region;

a buried heavily doped drain region in the substrate in the device region;

a gate in a trench in the device region, wherein a channel of the device is disposed on a sidewall of the trench, the buried heavily doped drain region is disposed below the gate and is vertically and laterally displaced away from the channel of the device, wherein a distance from the buried heavily doped drain region to the channel is a drift length L_D of the device;

a drain connector disposed in the trench and is connected to the buried heavily doped drain region, wherein the drain connector is isolated from the gate; and

a surface heavily doped region adjacent to the gate.

2. The semiconductor device of claim 1 wherein the device region is surrounded by device isolation region.

3. The semiconductor device of claim 2 wherein the device region comprises one or more internal device regions, dividing the device region into multiple device sub-regions.

4. The semiconductor device of claim 1 wherein the device region comprises:

a first device doped well; and

a second device doped well, the second device doped well has a depth equals to a channel length L_C of the channel,

wherein the first device doped well has a depth greater than the second device doped well.

5. The semiconductor device of claim 4 wherein the first device doped well comprises first polarity type dopants and the second device doped well comprises second polarity type dopants.

6. The semiconductor device of claim 5 wherein the second device doped well is disposed substantially within the first device doped well.

7. The semiconductor device of 6 wherein:

the trench is disposed in the first and second device doped wells and the trench comprises first and second portions.

8. The semiconductor device of claim 7 comprising:

the first portion of the trench has a depth greater than an interface of the first and second device doped wells;

gate insulators disposed on either sides of the drain connector in the first portion of the trench; and

gate electrodes on either sides of the gate insulators in the first portion of the trench.

9. A semiconductor device comprising:

a substrate defined with a device region;

a buried heavily doped drain region in the substrate in the device region;

a gate in a trench in the device region, wherein a channel of the device is disposed on a sidewall of the trench, the buried heavily doped drain region is disposed below the gate and is

vertically and laterally displaced away from the channel of the device, wherein a distance from the buried heavily doped drain region to the channel is a drift length L_D of the device;

a drain connector disposed in the trench and is connected to the buried heavily doped drain region, wherein the drain connector is isolated from the gate;

a gate dielectric layer which lines sidewalls and bottom of a first portion of the trench without lining sidewalls of the drain connector; and

a surface heavily doped region adjacent to the gate.

10. The semiconductor device of claim 8 wherein each of the gate insulators include a primary gate insulator and a secondary gate insulator which comprise different materials.

11. A semiconductor device comprising:

a substrate defined with a device region;

first and second device doped wells in the device region, wherein the first device doped well has a depth greater than the second device doped well;

a buried heavily doped region which is disposed within the first device doped well;

a gate in a trench in the device region, the trench has a depth greater than an interface of the first and second device doped wells, wherein a channel of the device is disposed on a sidewall of the trench, the buried heavily doped region is disposed below the gate and is vertically and laterally displaced away from the gate and channel of the device, wherein a distance from the buried heavily doped region to the channel is a drift length L_D of the device;

a drain connector disposed in the trench, wherein the drain connector is disposed adjacent to the gate and extends from a top surface of the substrate to the buried heavily doped region;

a gate dielectric layer which lines sidewalls and bottom of the trench without lining sidewalls of the drain connector; and

a surface heavily doped region adjacent to the gate.

12. The semiconductor device of claim 11 wherein the second device doped well has a depth equals to a channel length L_C of the channel.

13. The semiconductor device of claim 11 wherein the first device doped well comprises first polarity type dopants and the second device doped well comprises second polarity type dopants and the first and second device doped wells comprise dopant concentration lesser than the buried and surface heavily doped regions.

14. The semiconductor of claim 11 wherein the drain connector directly contacts the buried heavily doped region.

15. The semiconductor device of claim 14 wherein the buried heavily doped region is disposed directly below the drain connector and occupies a portion of the first device doped well.

16. The semiconductor device of claim 11 comprising:

gate insulators disposed on either sides of the drain connector in the trench; and

gate electrodes on either sides of the gate insulators in the trench.

17. The semiconductor device of claim 16 wherein each of the gate insulators include a primary gate insulator and a secondary gate insulator which comprise different materials.

18. The semiconductor device of claim 11 wherein the gate dielectric layer comprises the same thickness.