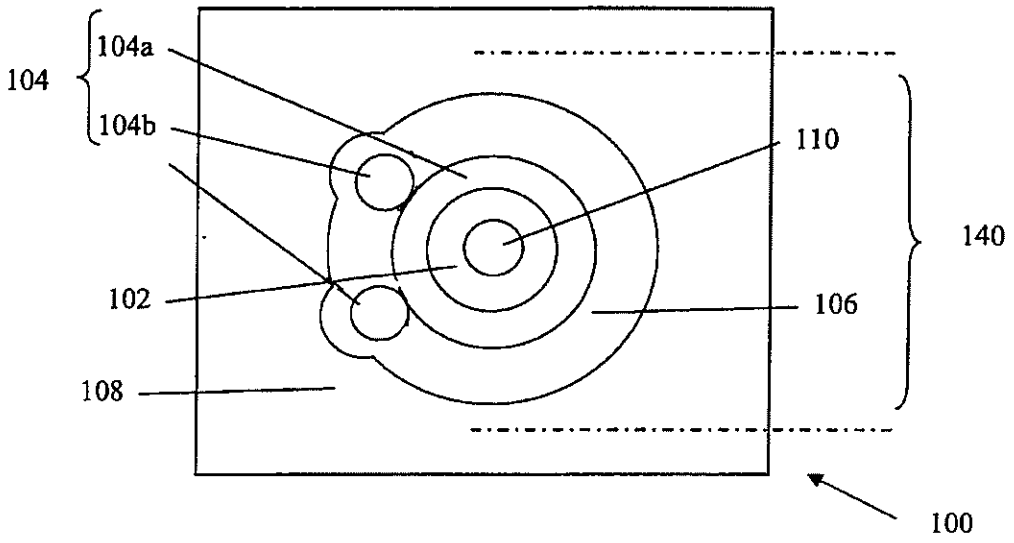


Figure 1A

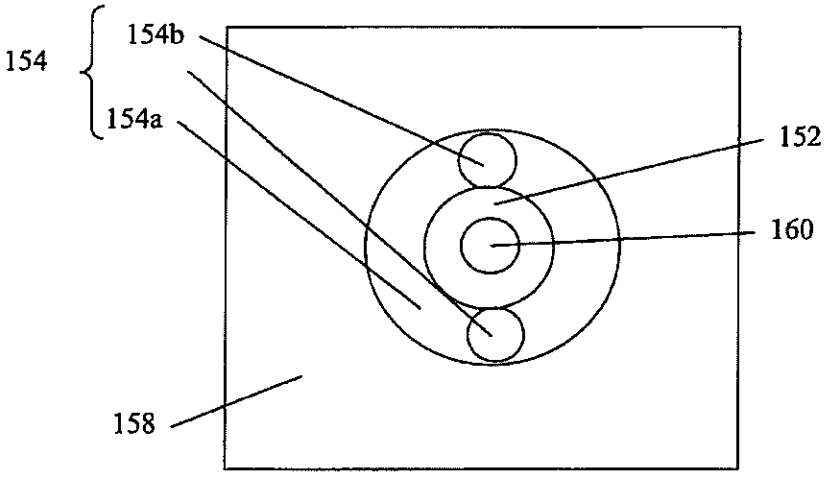


Figure 1B

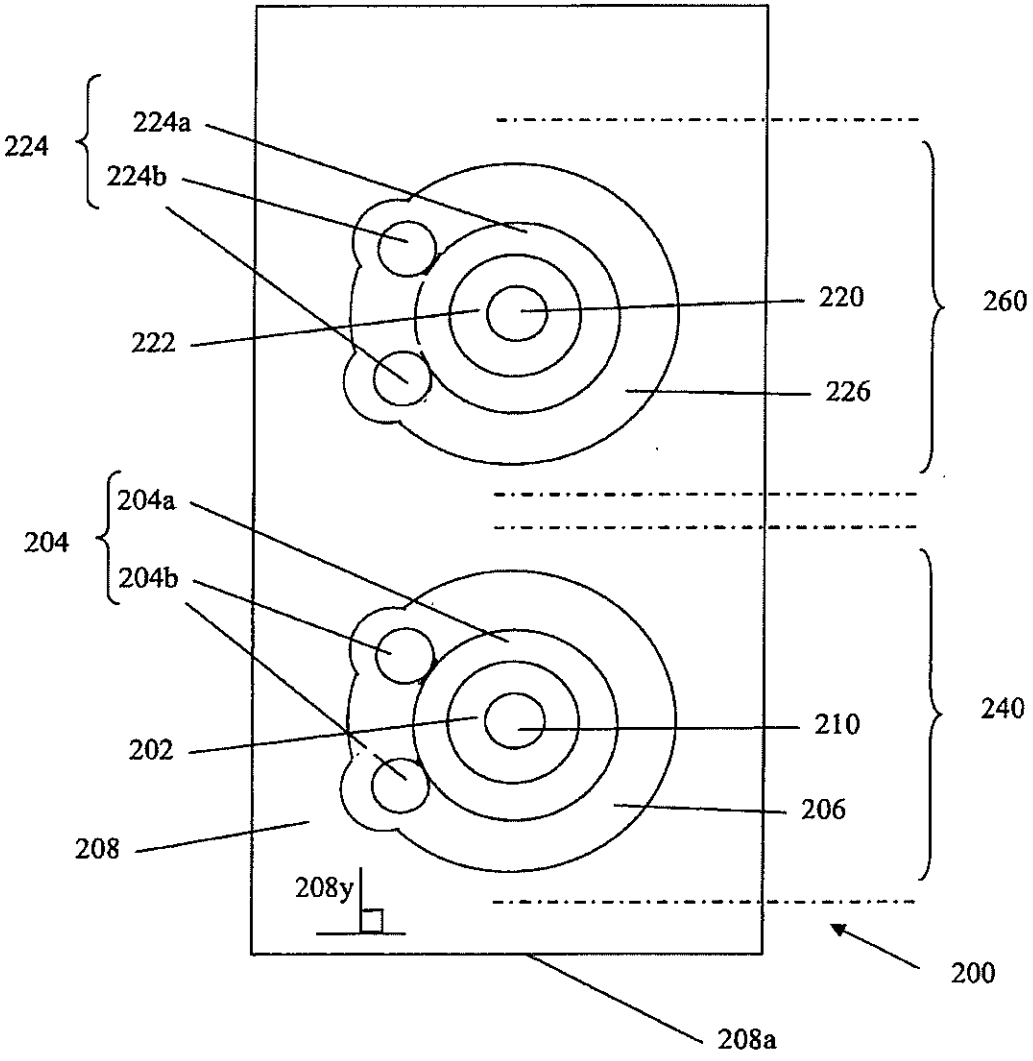

224
224a
224b
222
220
226
260
204
204a
204b
202
210
206
240
208
208y
200
208a

Figure 2A

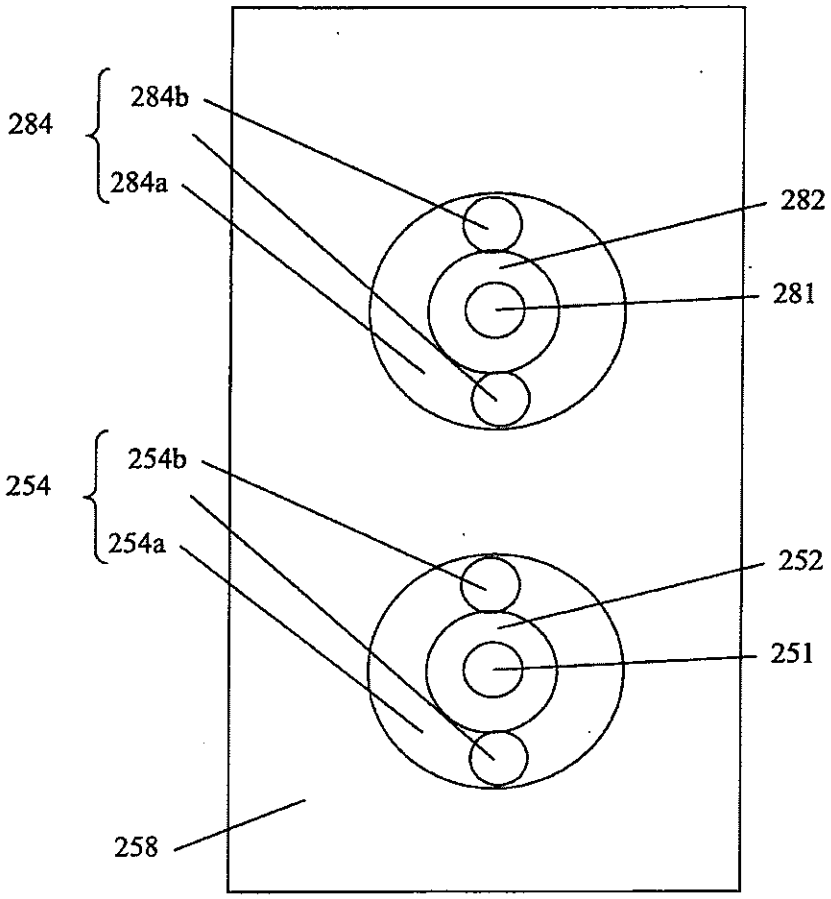


Figure 2B

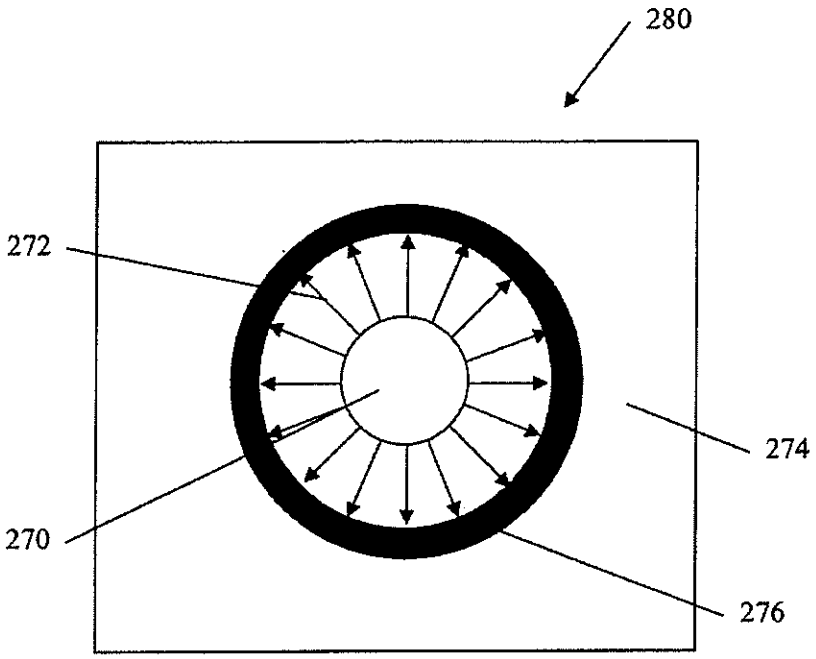


Figure 2 (I)

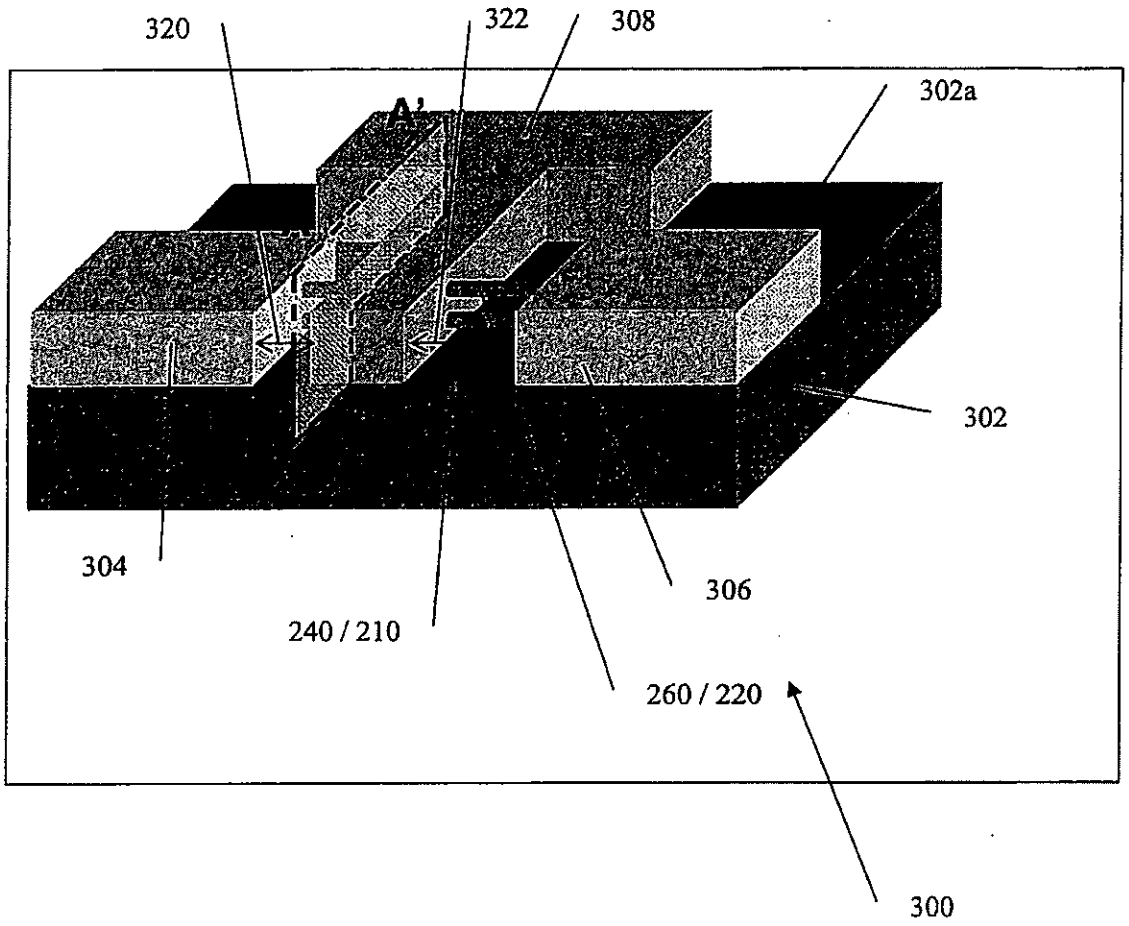


Figure 3

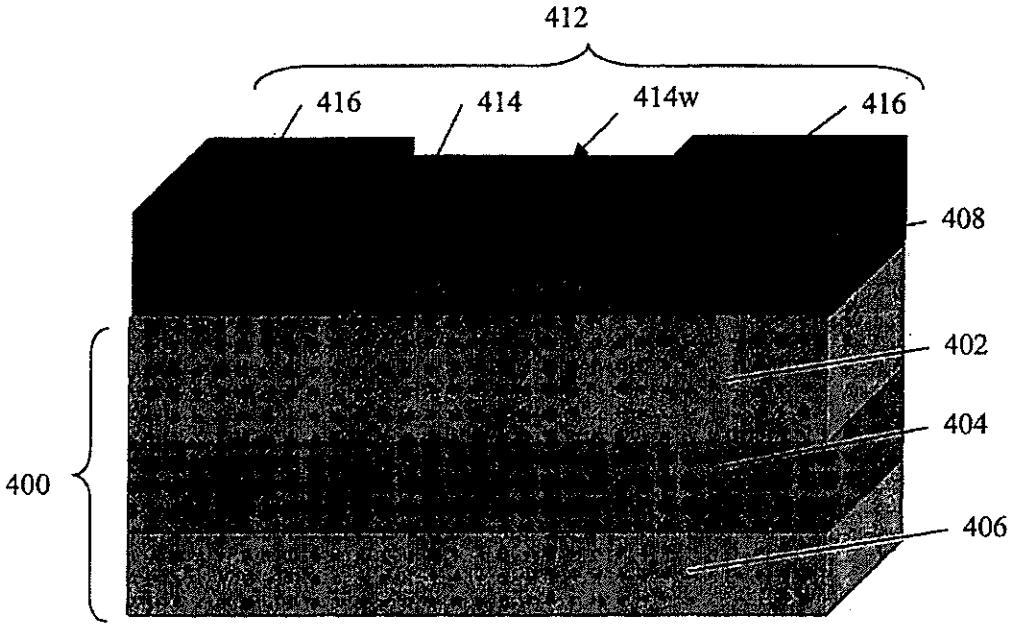


Figure 4A

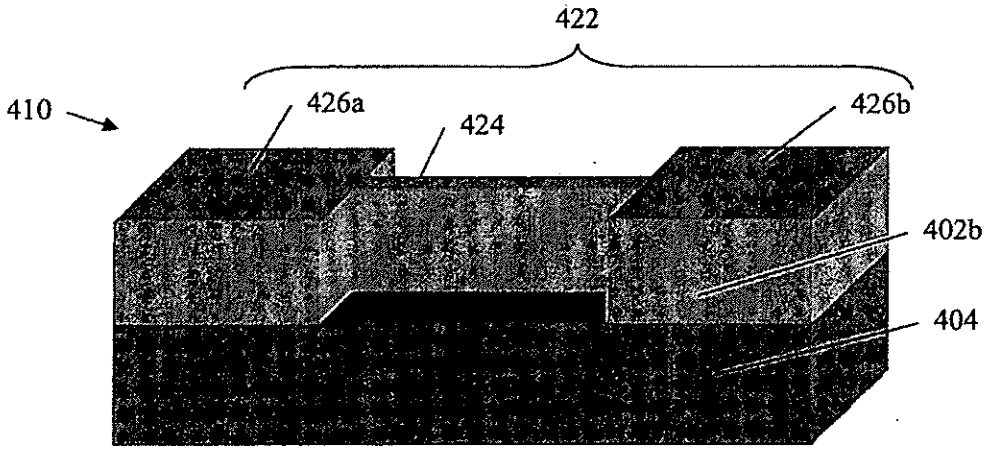


Figure 4B

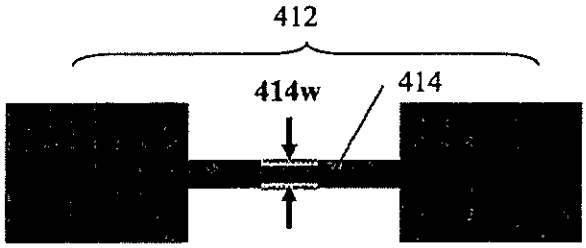


Figure 4B(I)

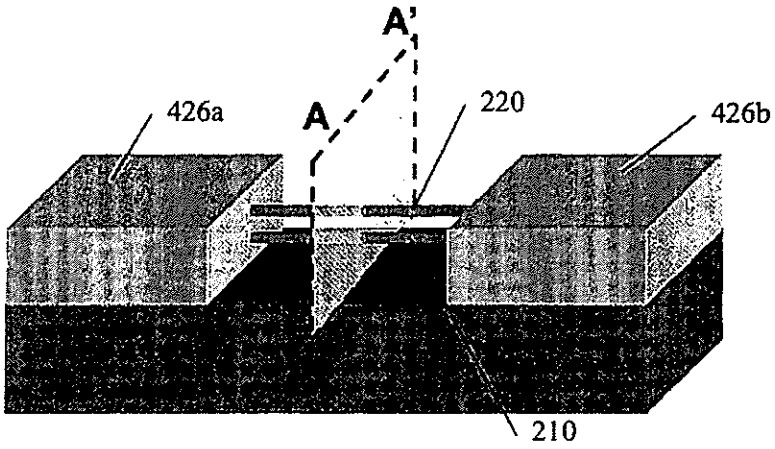


Figure 4C

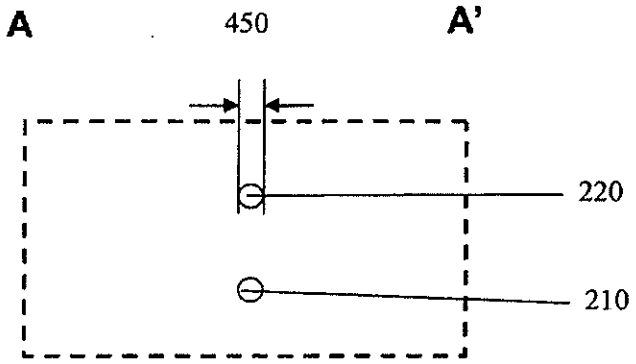


Figure 4C(I)

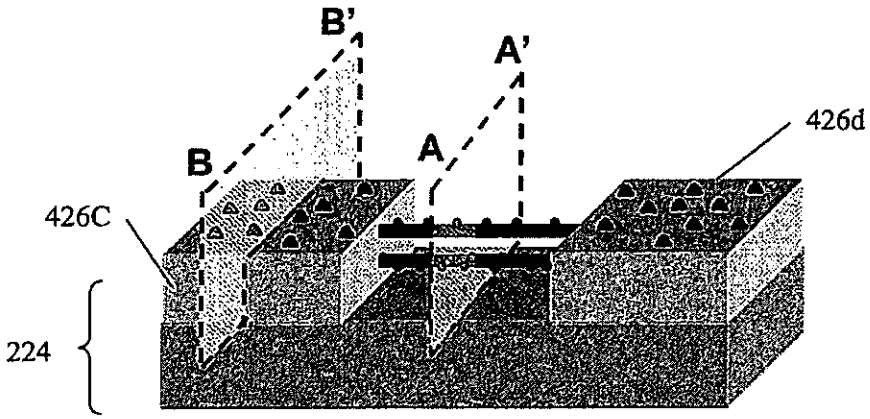


Figure 4D

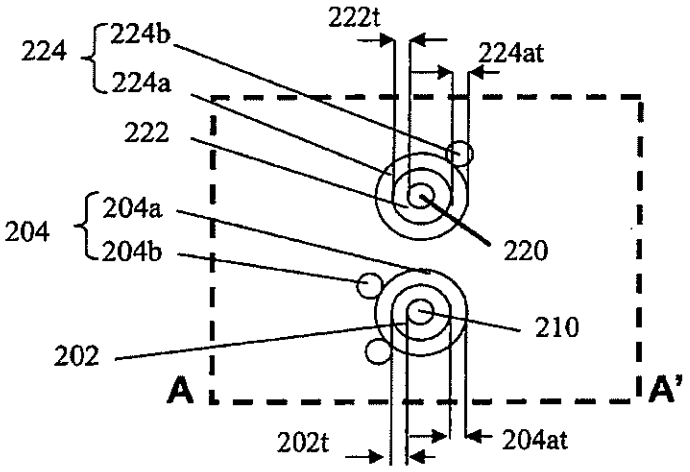


Figure 4D(I)

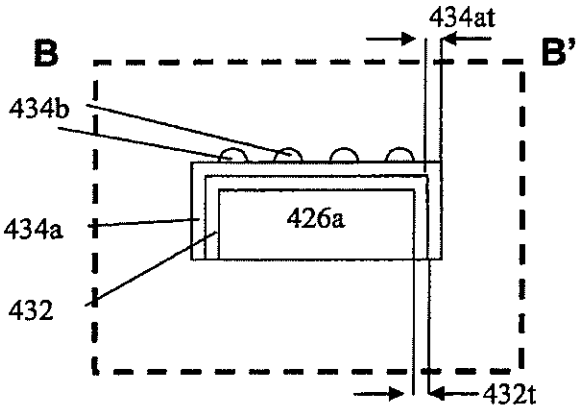


Figure 4D(II)

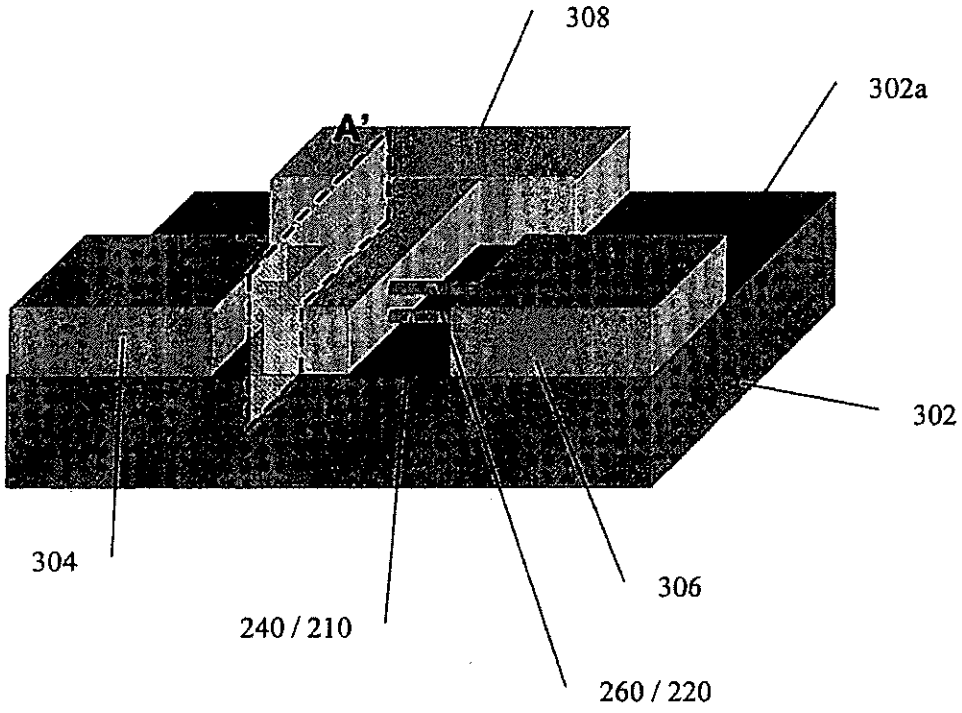


Figure 4E

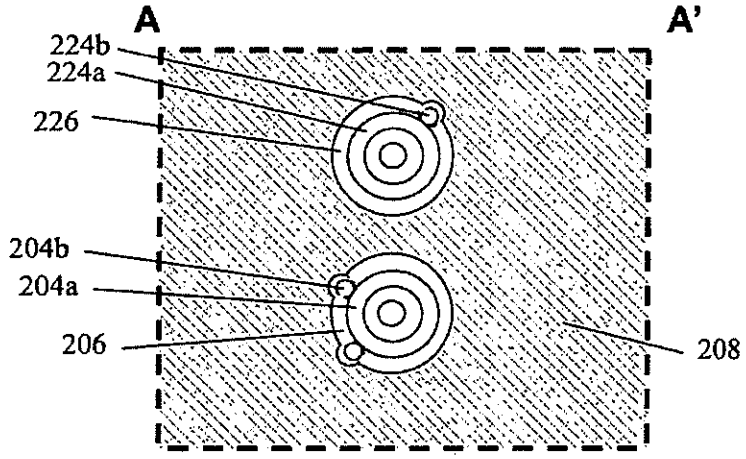


Figure 4E (I)

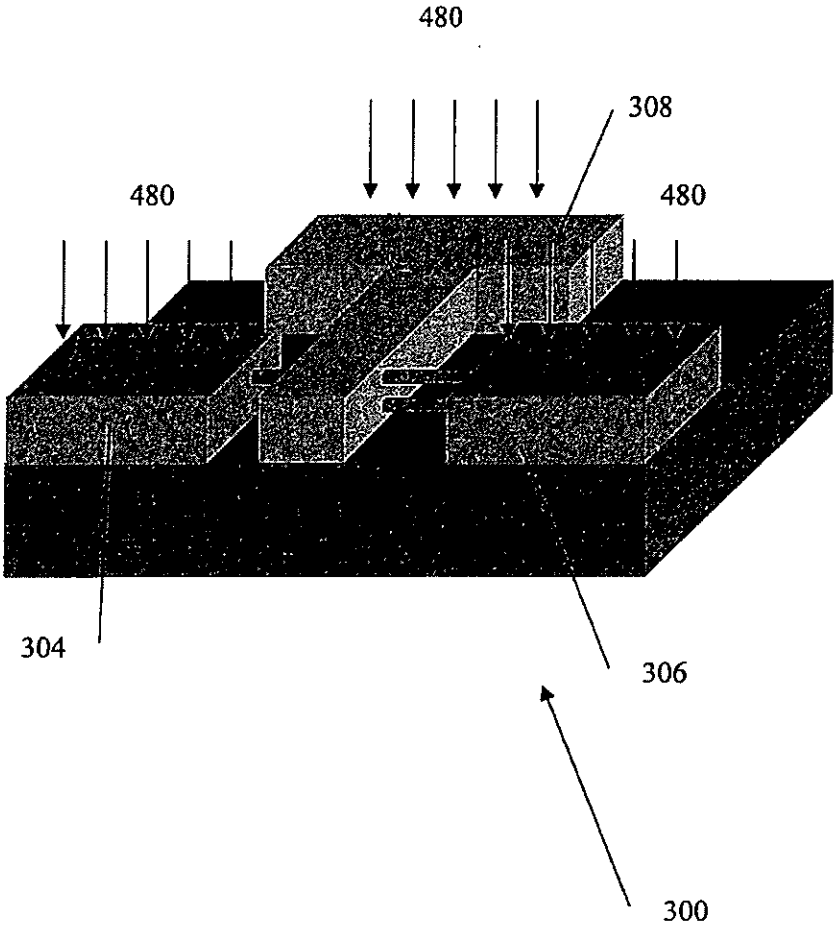


Figure 4F

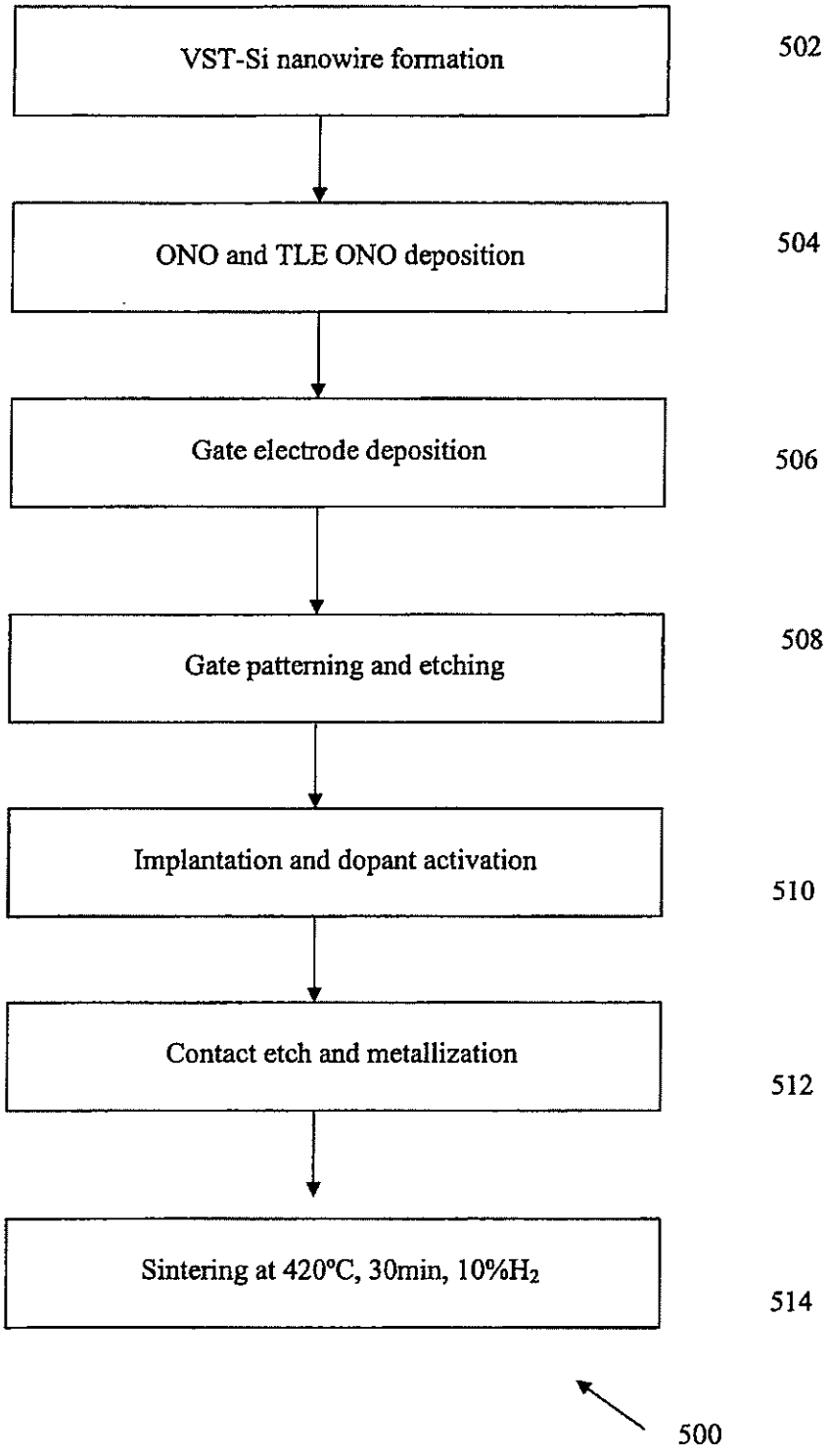

VST-Si nanowire formation
502
ONO and TLE ONO deposition
504
Gate electrode deposition
506
Gate patterning and etching
508
Implantation and dopant activation
510
Contact etch and metallization
512
Sintering at 420°C, 30min, 10%H_2
514
500

Figure 5A

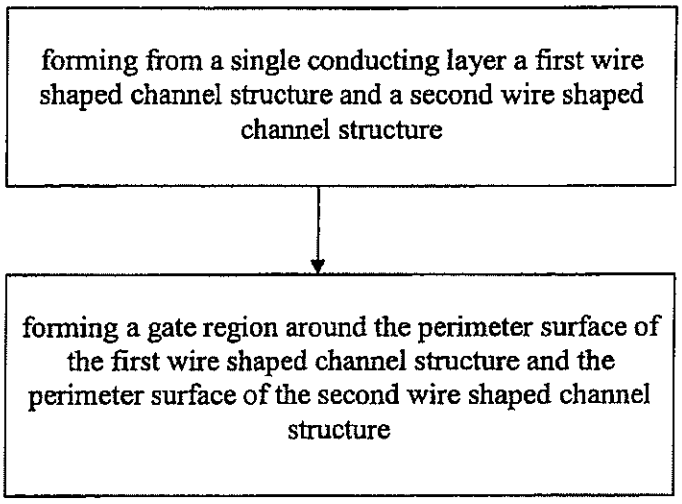


Figure 5B

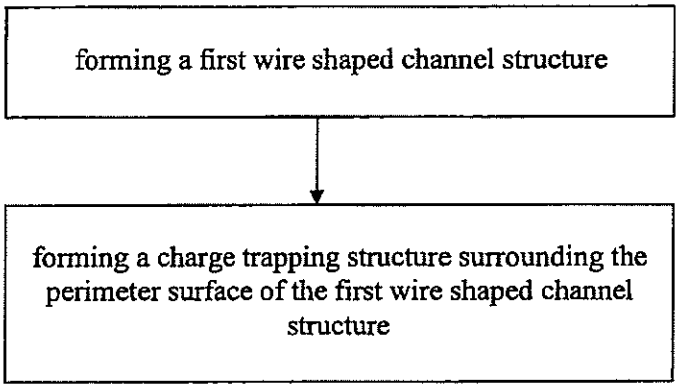


Figure 6

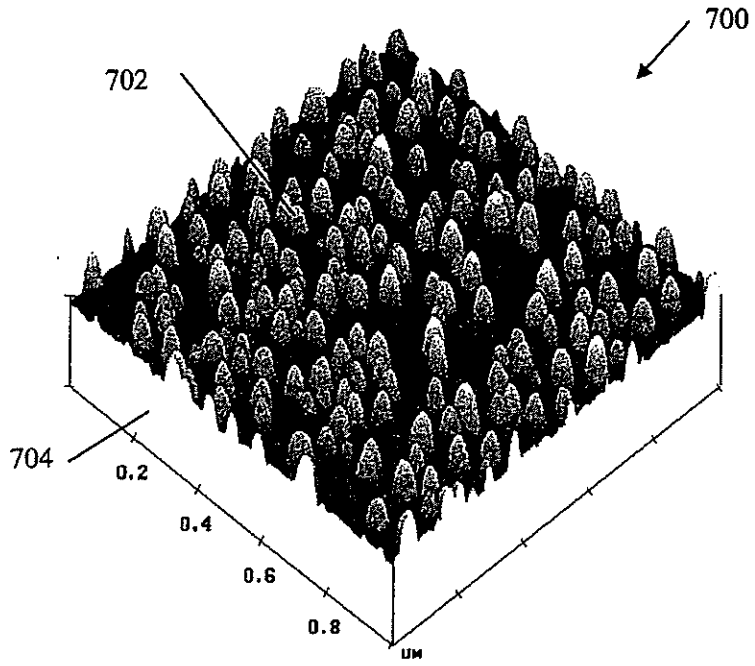


Figure 7

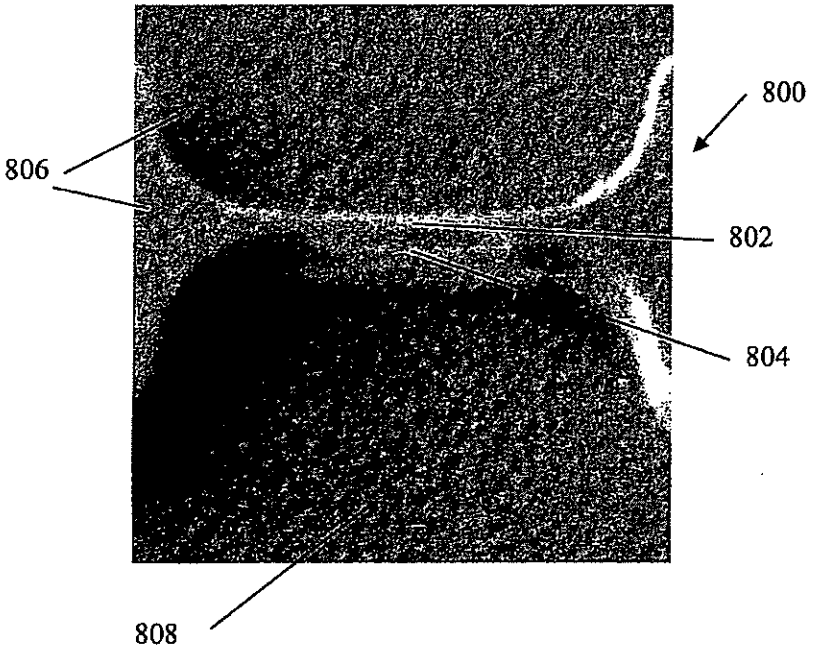


Figure 8

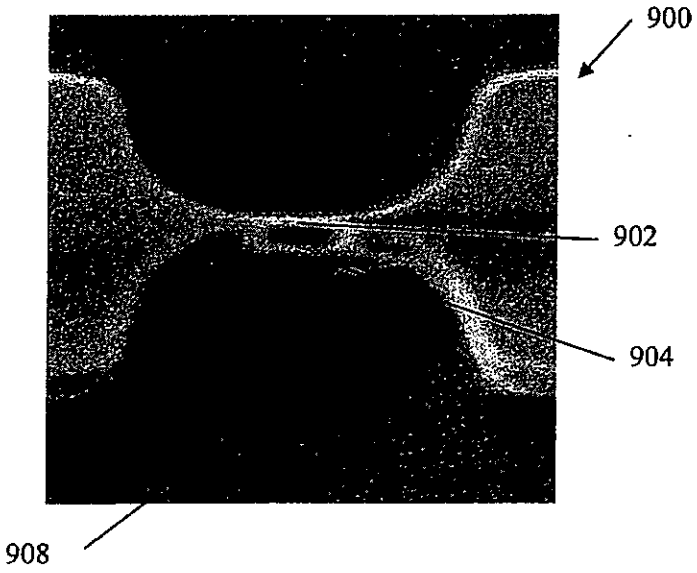


Figure 9

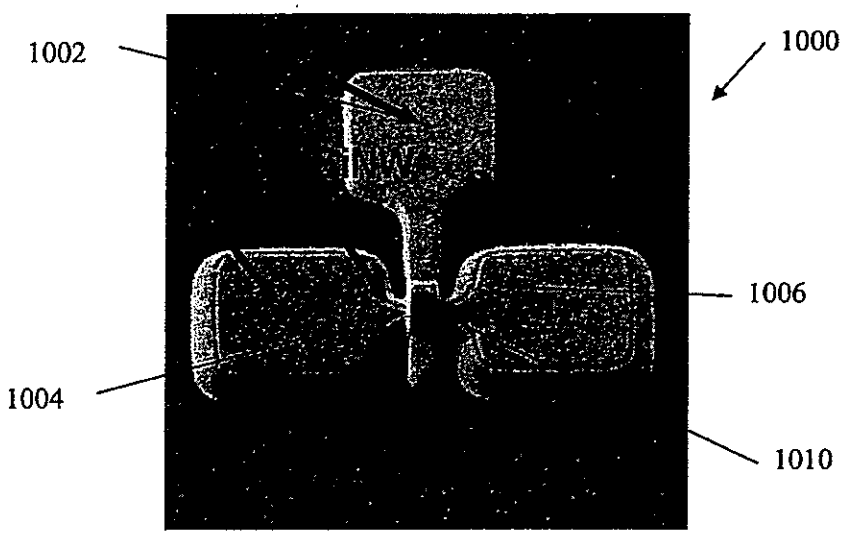


Figure 10

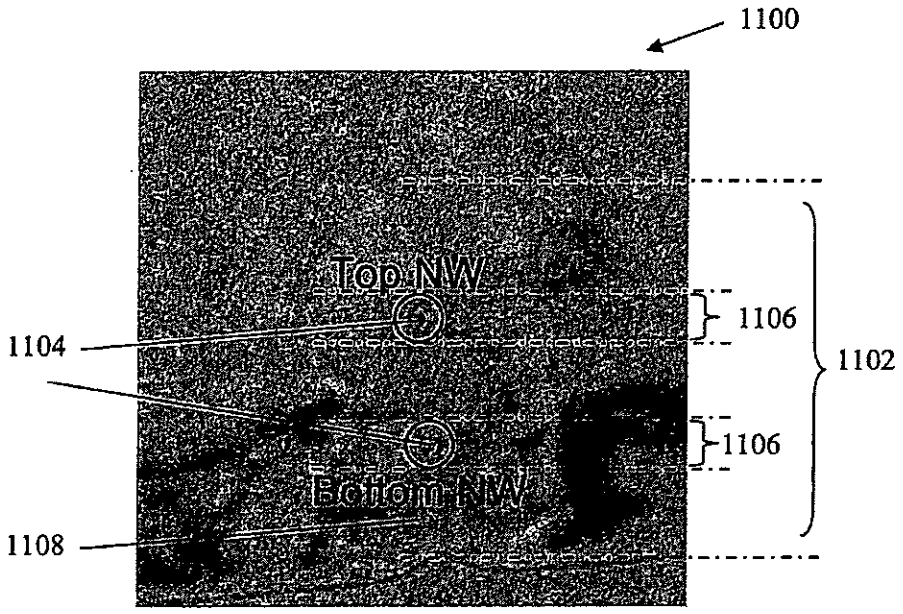


Figure 11

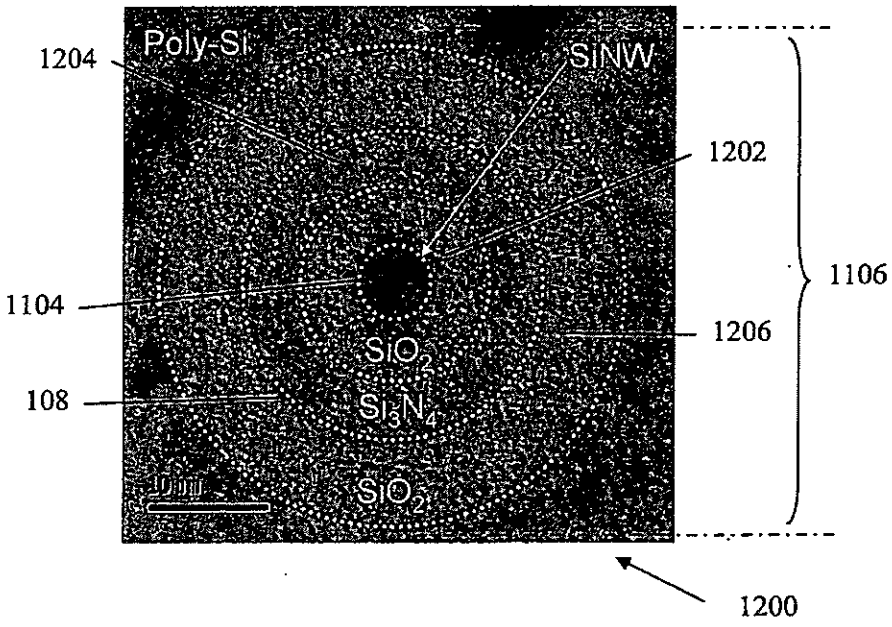


Figure 12

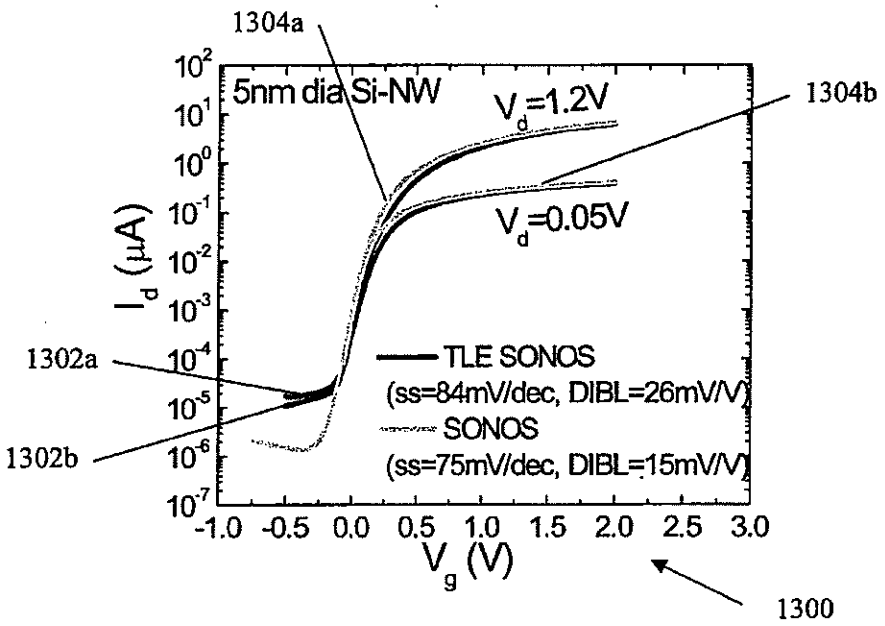


Figure 13

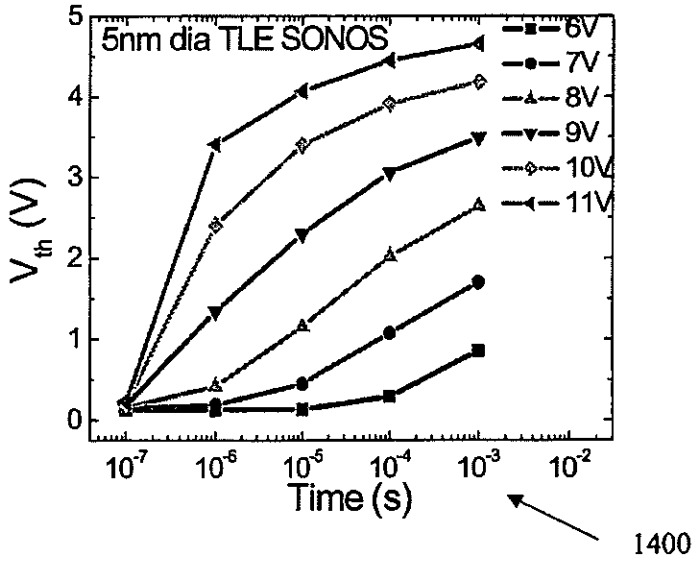


Figure 14A

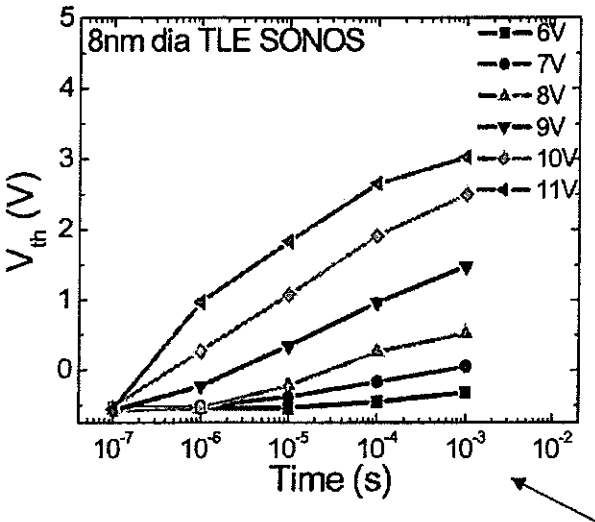


Figure 14B

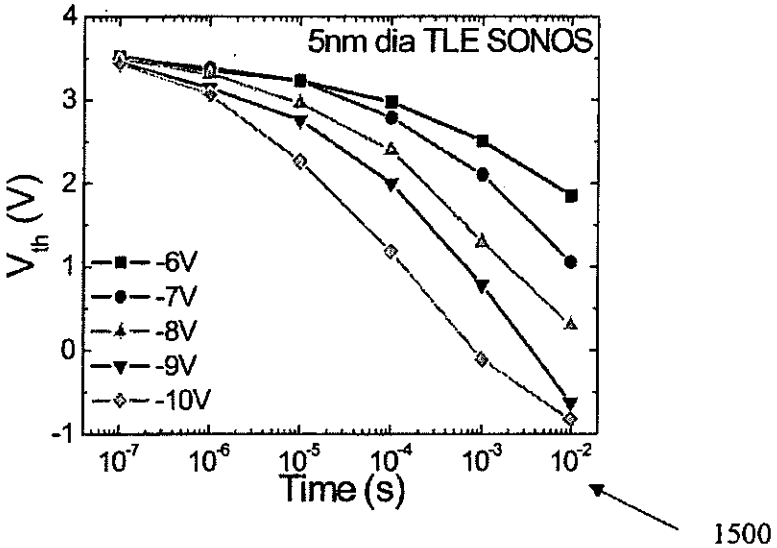


Figure 15A

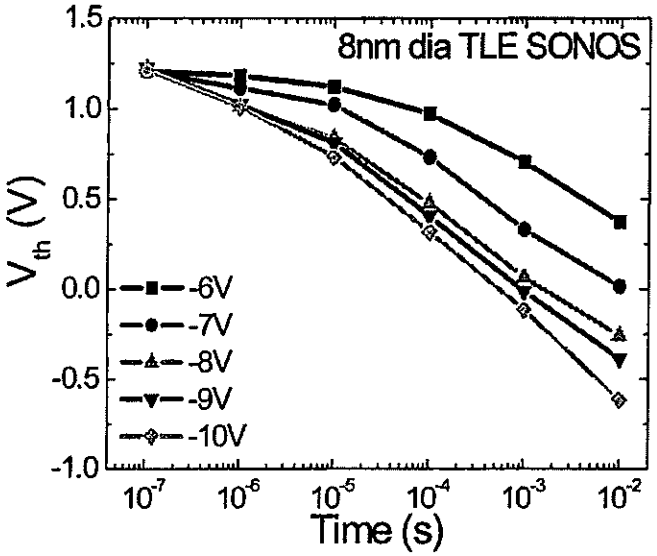


Figure 15B

1550

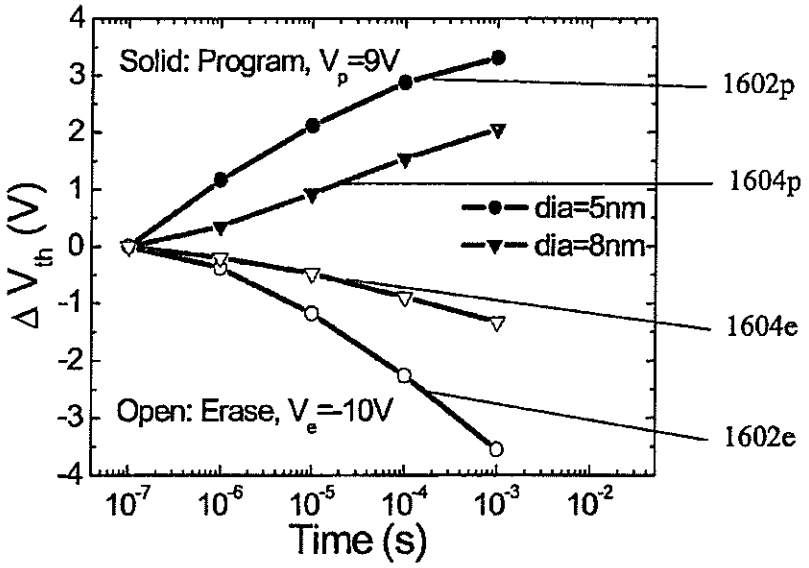


Figure 16

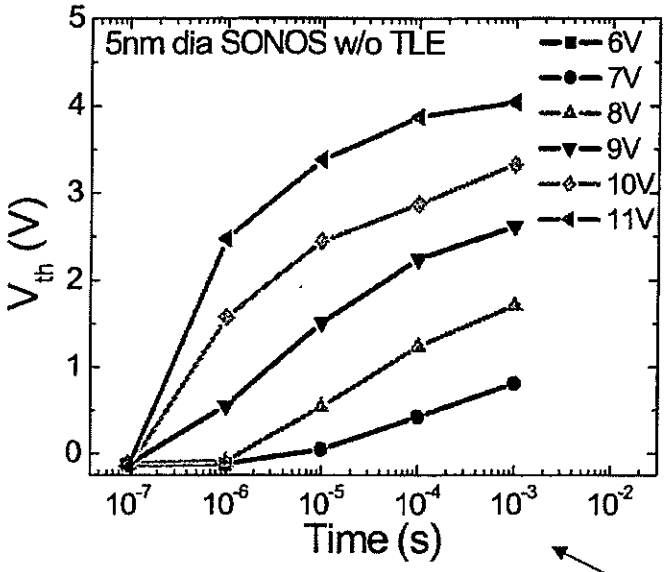


Figure 17A

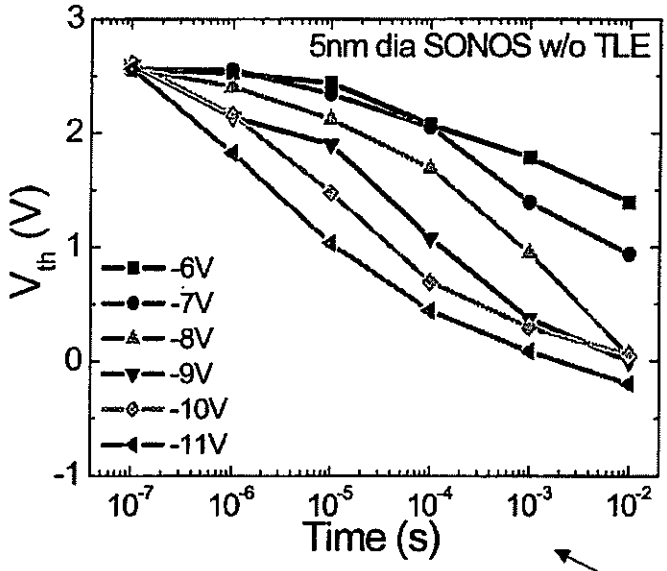


Figure 17B

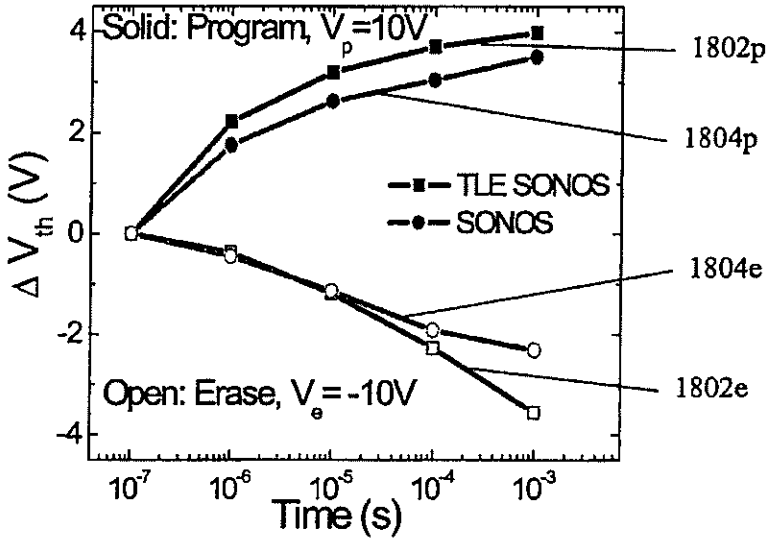


Figure 18

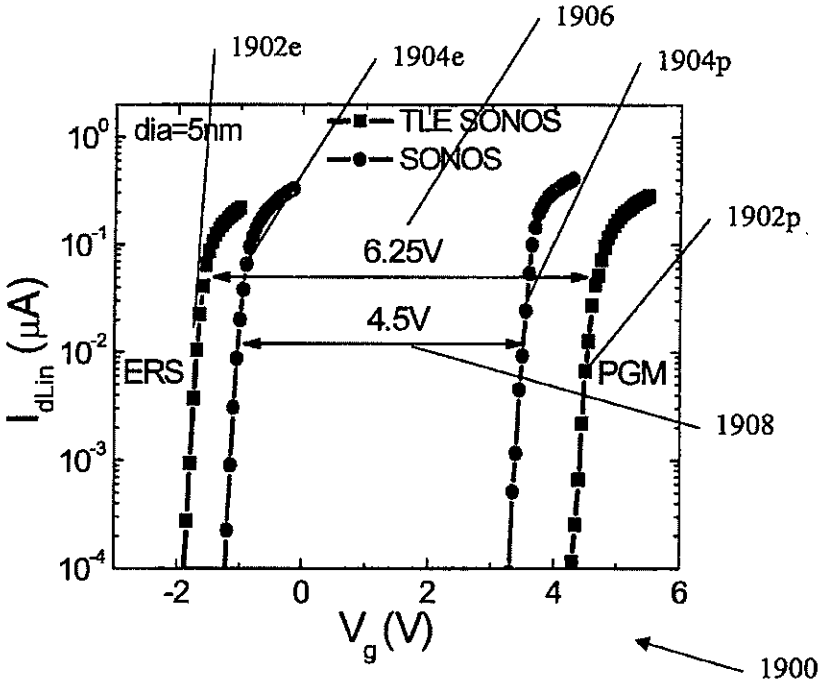


Figure 19

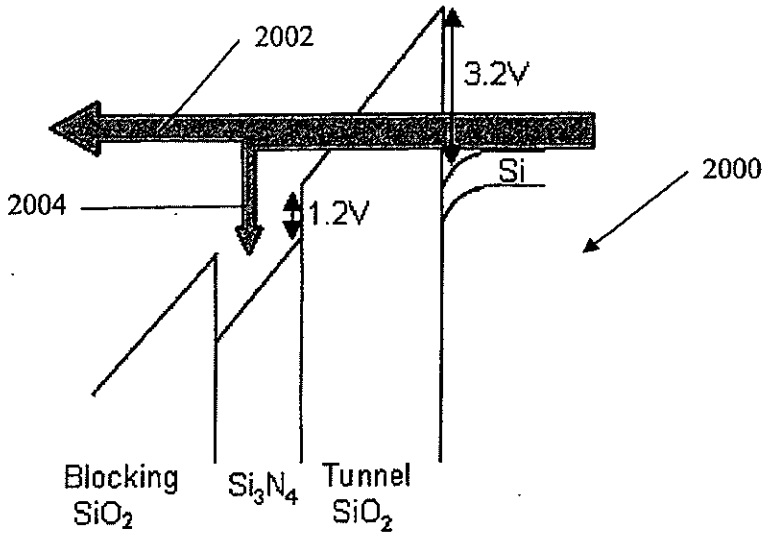


Figure 20A

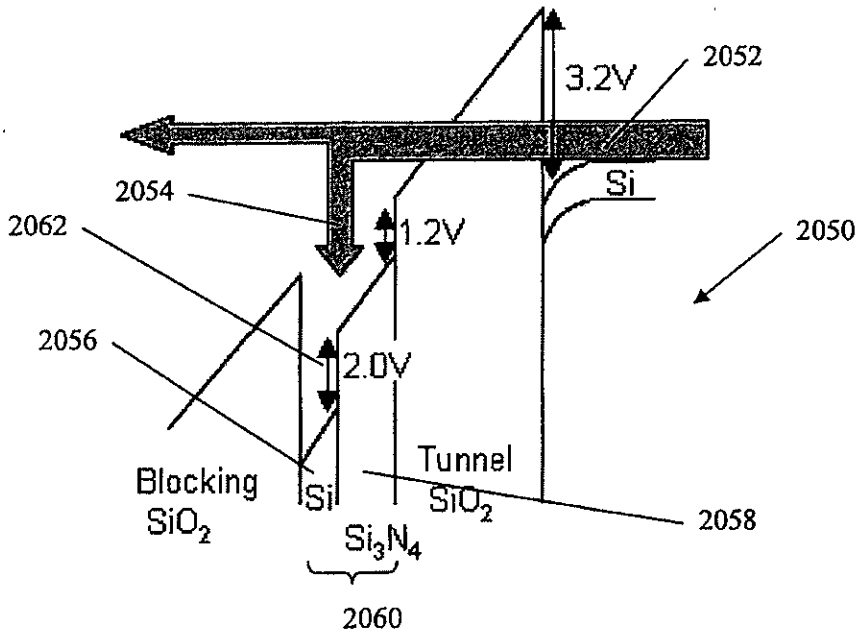


Figure 20B

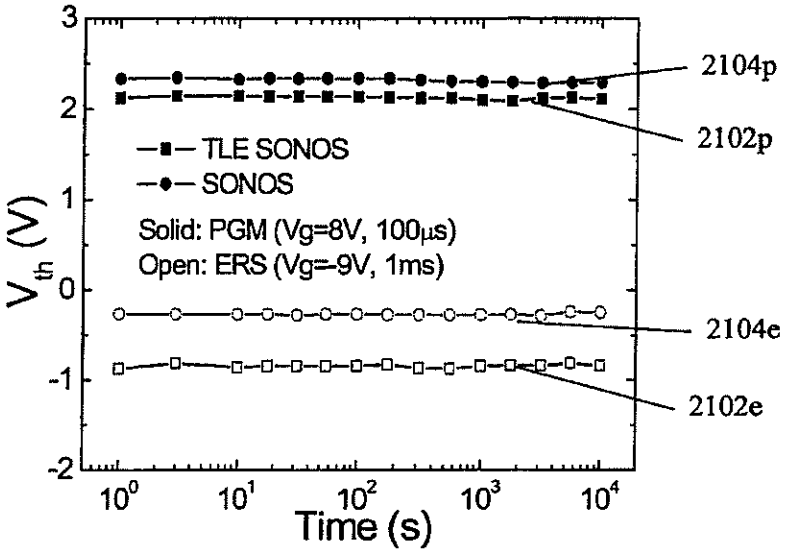


Figure 21

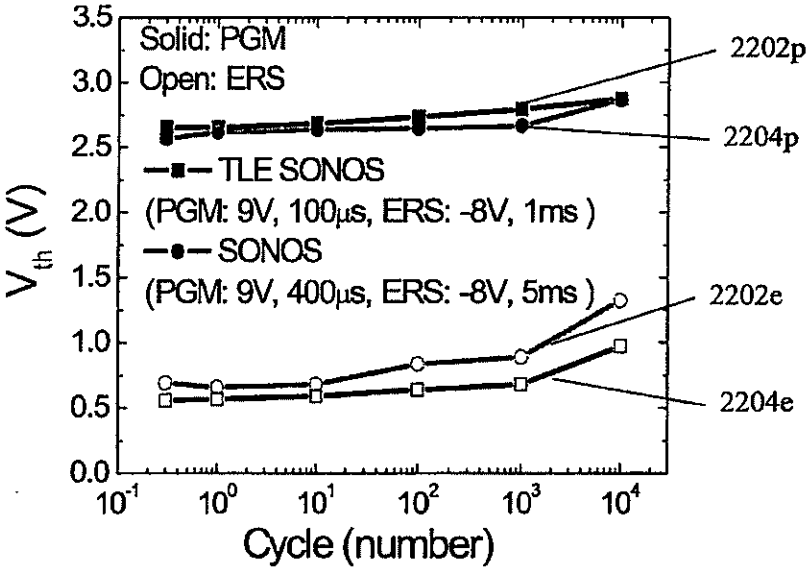


Figure 22

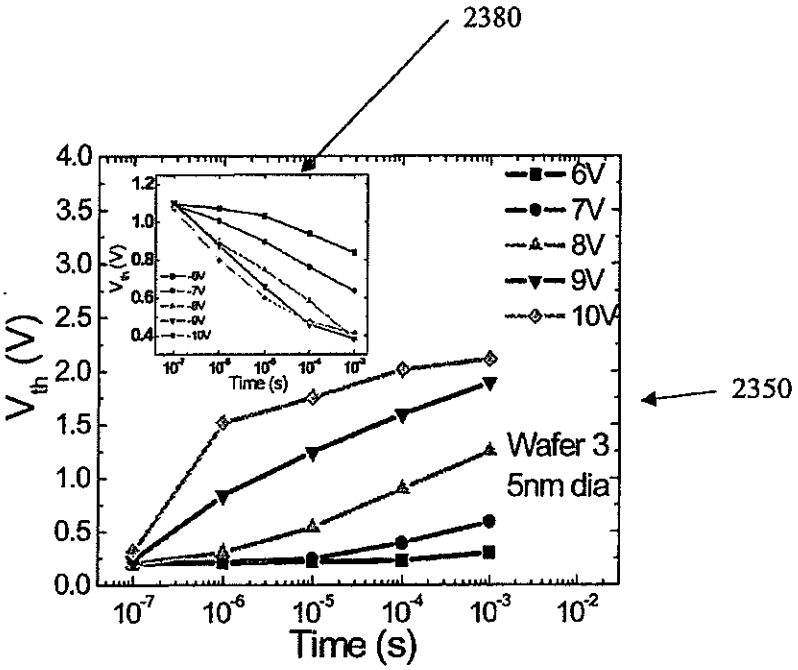

2380
2350
6V
7V
8V
9V
10V
Wafer 3
5nm dia
V_{th} (V)
Time (s)
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
10^{-7}
10^{-6}
10^{-5}
10^{-4}
10^{-3}
10^{-2}

Figure 23A