FIG. 1

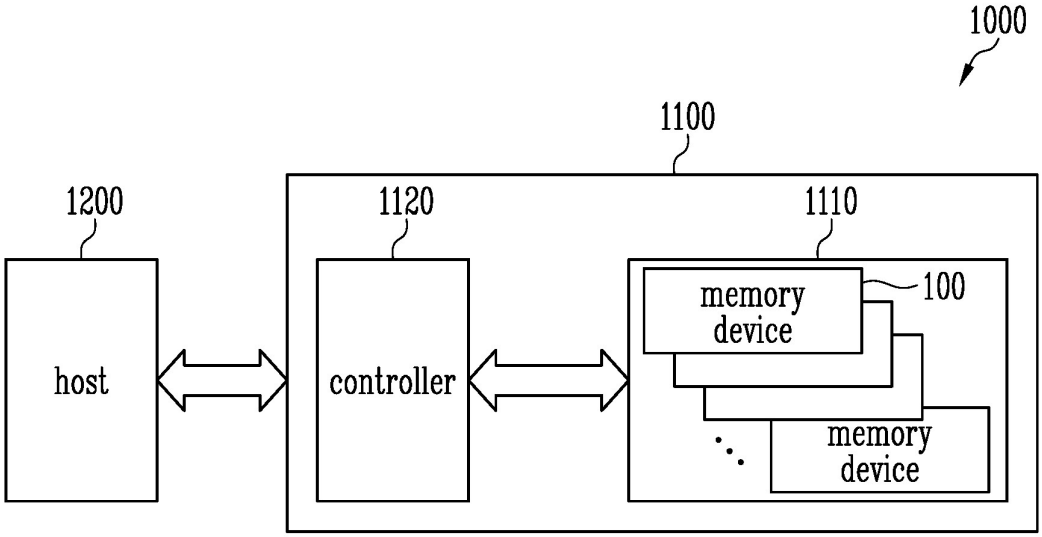

1000
1100
1200
1120
1110
host
controller
memory device
100
memory device

FIG. 2

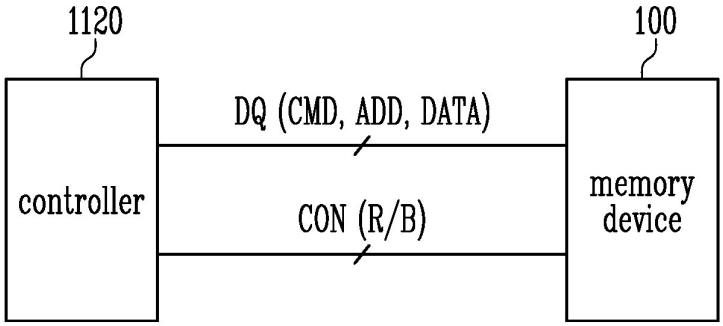

1120
100
controller
DQ (CMD, ADD, DATA)
CON (R/B)
memory device

FIG. 3

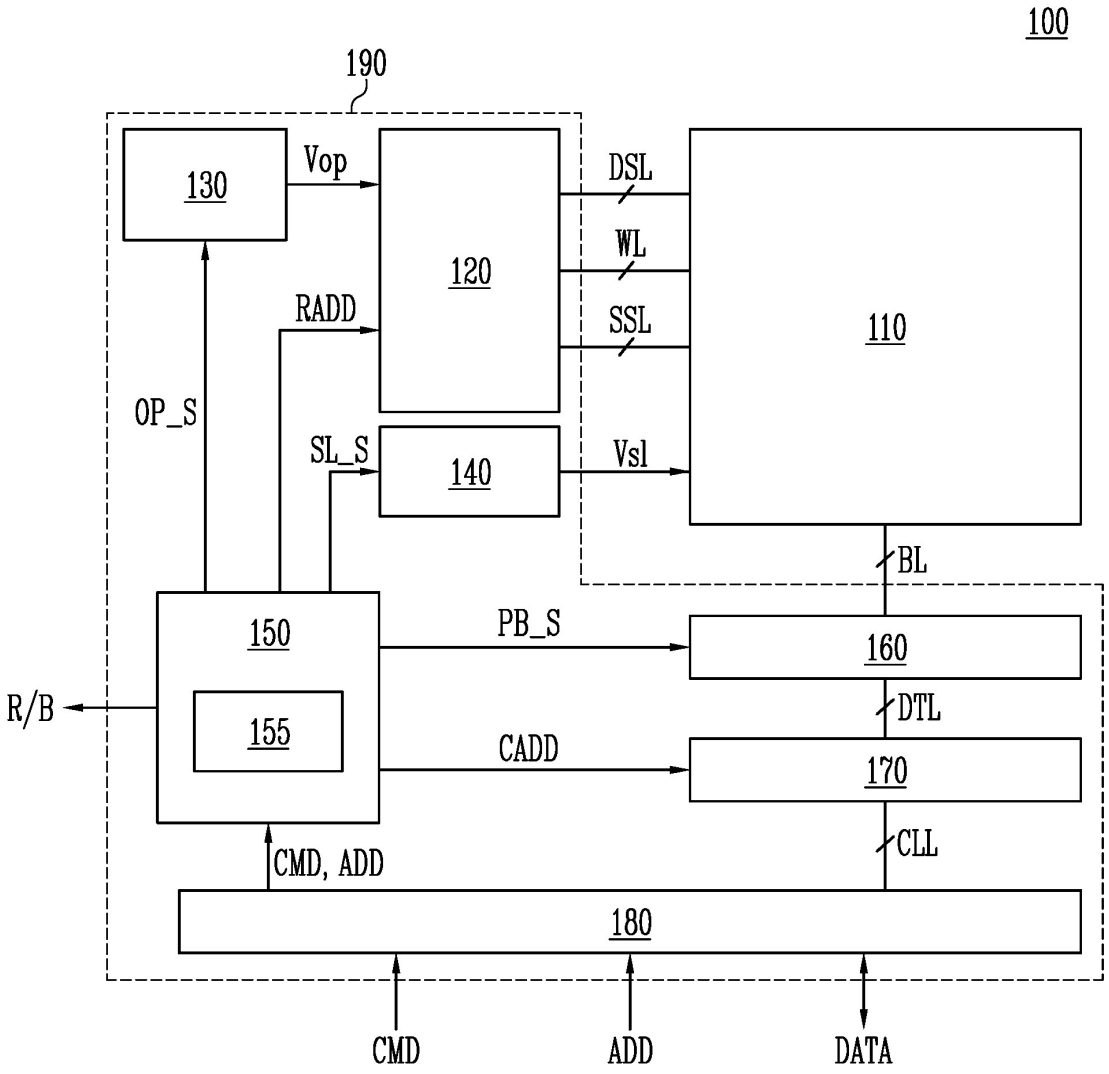

100
190
130
Vop
120
DSL
WL
SSL
110
RADD
OP_S
SL_S
140
Vsl
BL
150
PB_S
160
R/B
155
DTL
CADD
170
CLL
CMD, ADD
180
CMD
ADD
DATA

FIG. 4

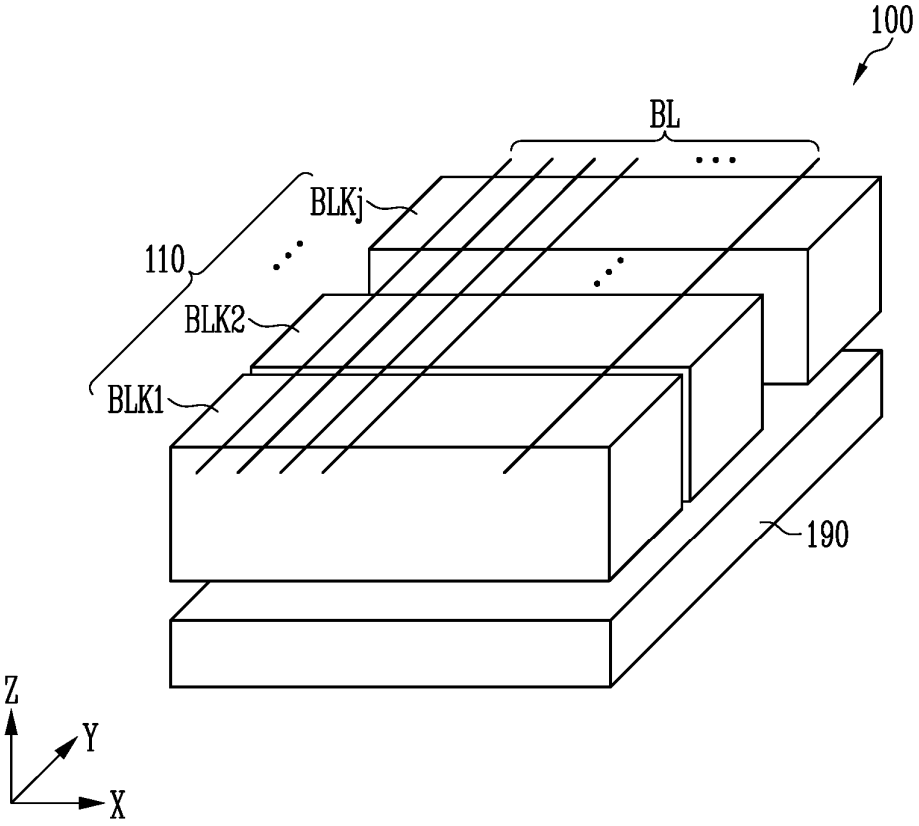


FIG. 5

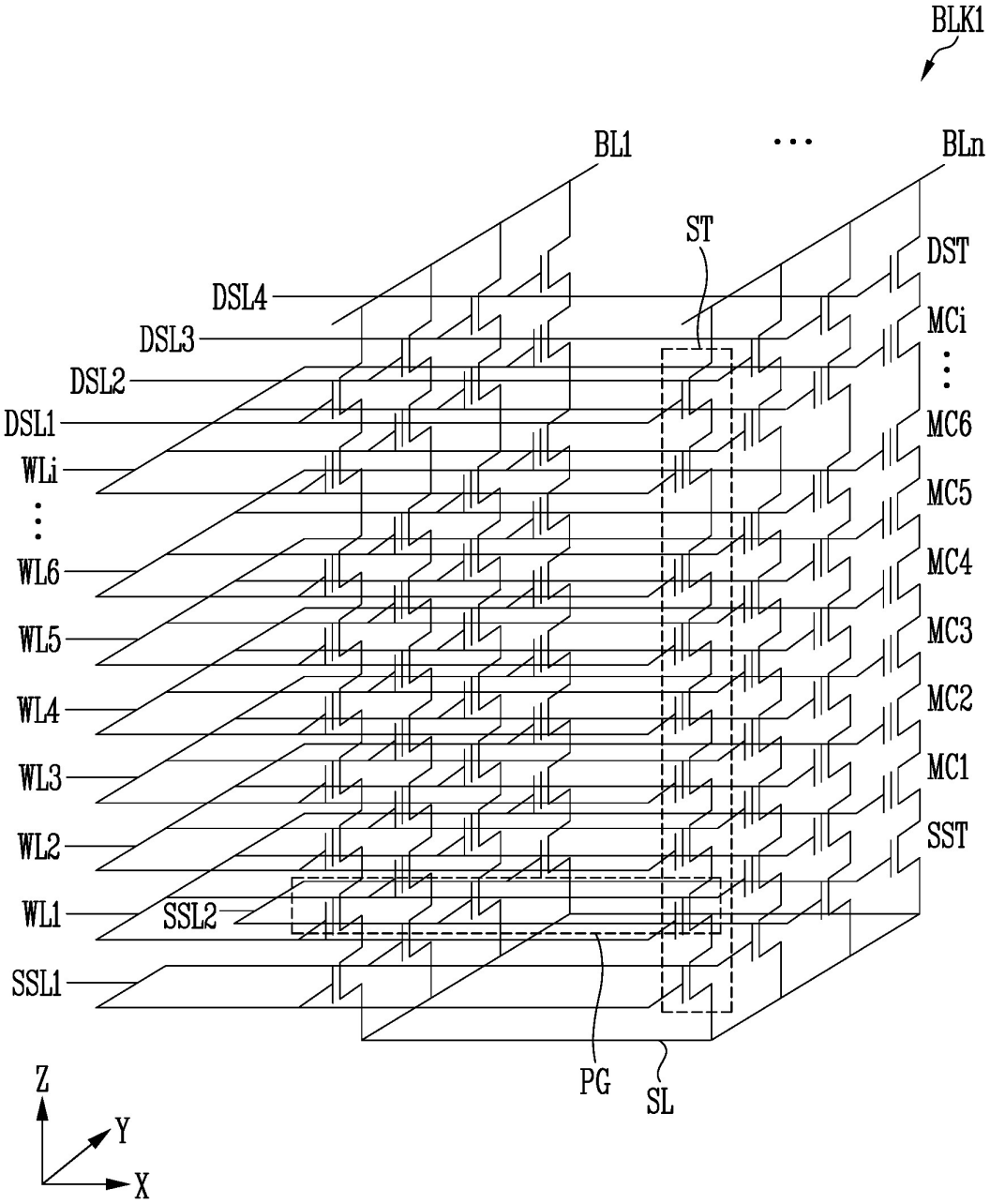

BLK1
BL1
BLn
ST
DST
DSL4
DSL3
DSL2
DSL1
WLi
WL6
WL5
WL4
WL3
WL2
WL1
SSL2
SSL1
MCi
MC6
MC5
MC4
MC3
MC2
MC1
SST
PG
SL
Z
Y
X

FIG. 6

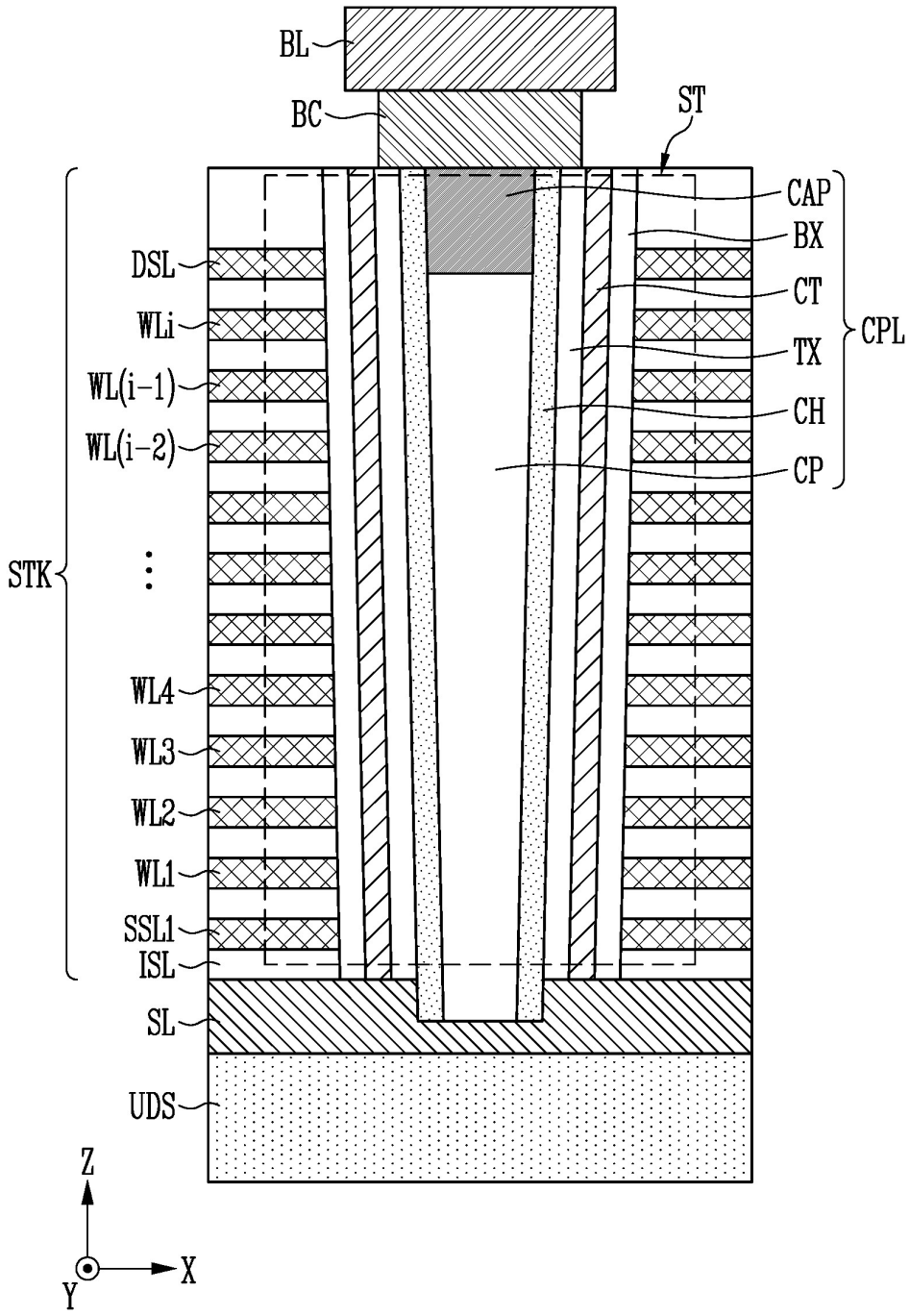

BL
BC
ST
CAP
BX
CT
TX
CH
CP
CPL
DSL
WLi
WL(i-1)
WL(i-2)
STK
WL4
WL3
WL2
WL1
SSL1
ISL
SL
UDS
Z
X
Y

FIG. 7A

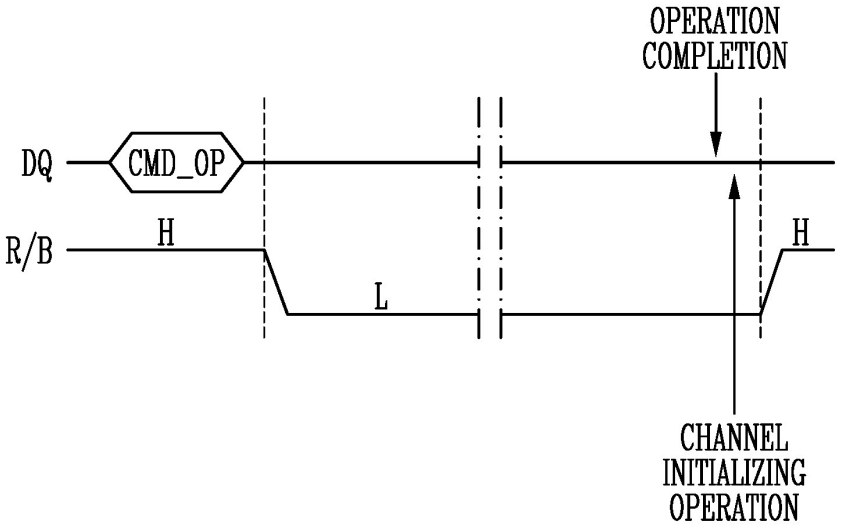

OPERATION
COMPLETION
DQ
CMD_OP
R/B
H
L
H
CHANNEL
INITIALIZING
OPERATION

FIG. 7B

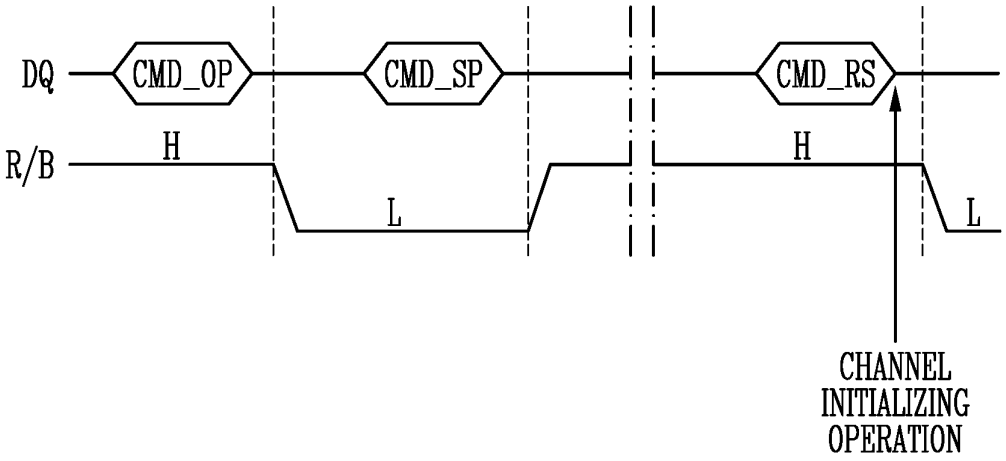

DQ
CMD_OP
CMD_SP
CMD_RS
R/B
H
L
H
L
CHANNEL
INITIALIZING
OPERATION

FIG. 8

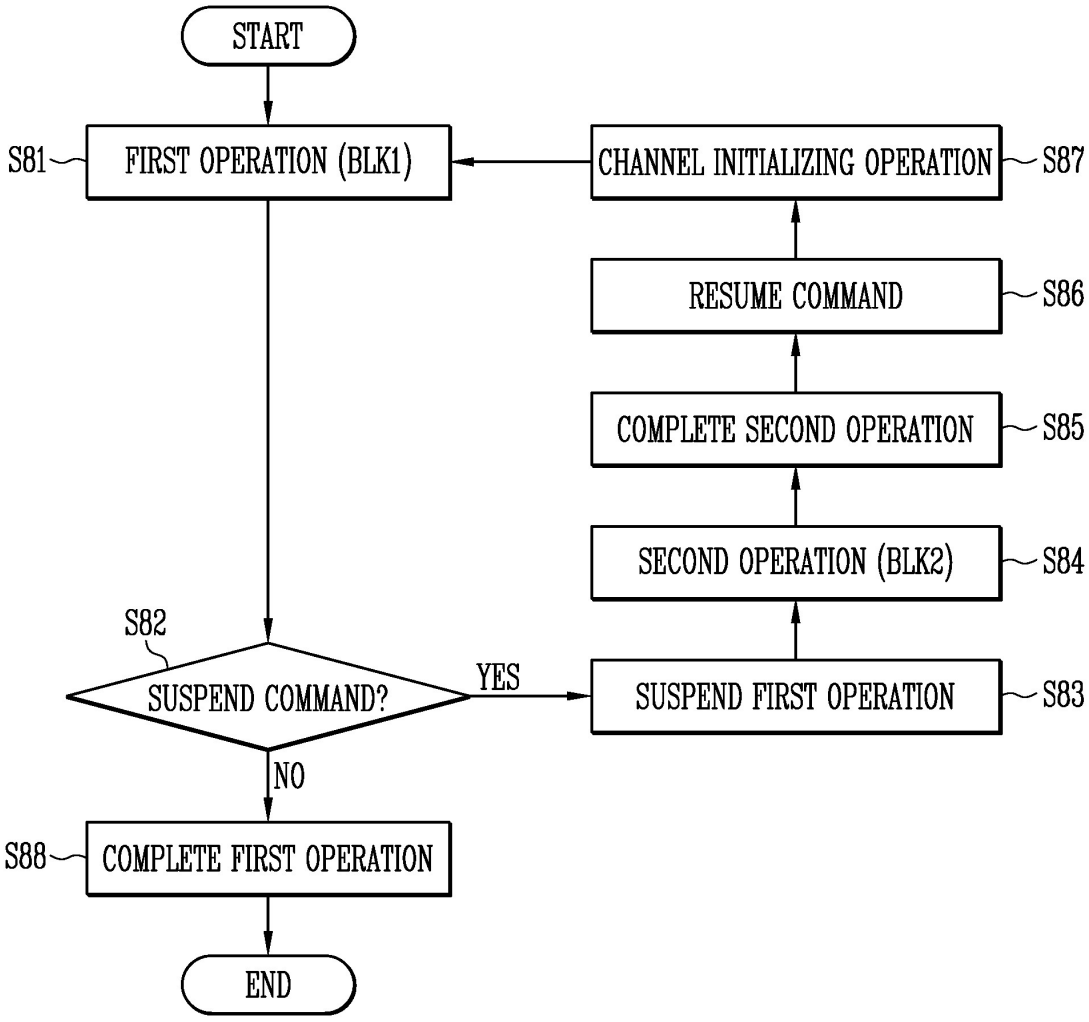

START
S81
FIRST OPERATION (BLK1)
S82
SUSPEND COMMAND?
YES
NO
S83
SUSPEND FIRST OPERATION
S84
SECOND OPERATION (BLK2)
S85
COMPLETE SECOND OPERATION
S86
RESUME COMMAND
S87
CHANNEL INITIALIZING OPERATION
S88
COMPLETE FIRST OPERATION
END

FIG. 9

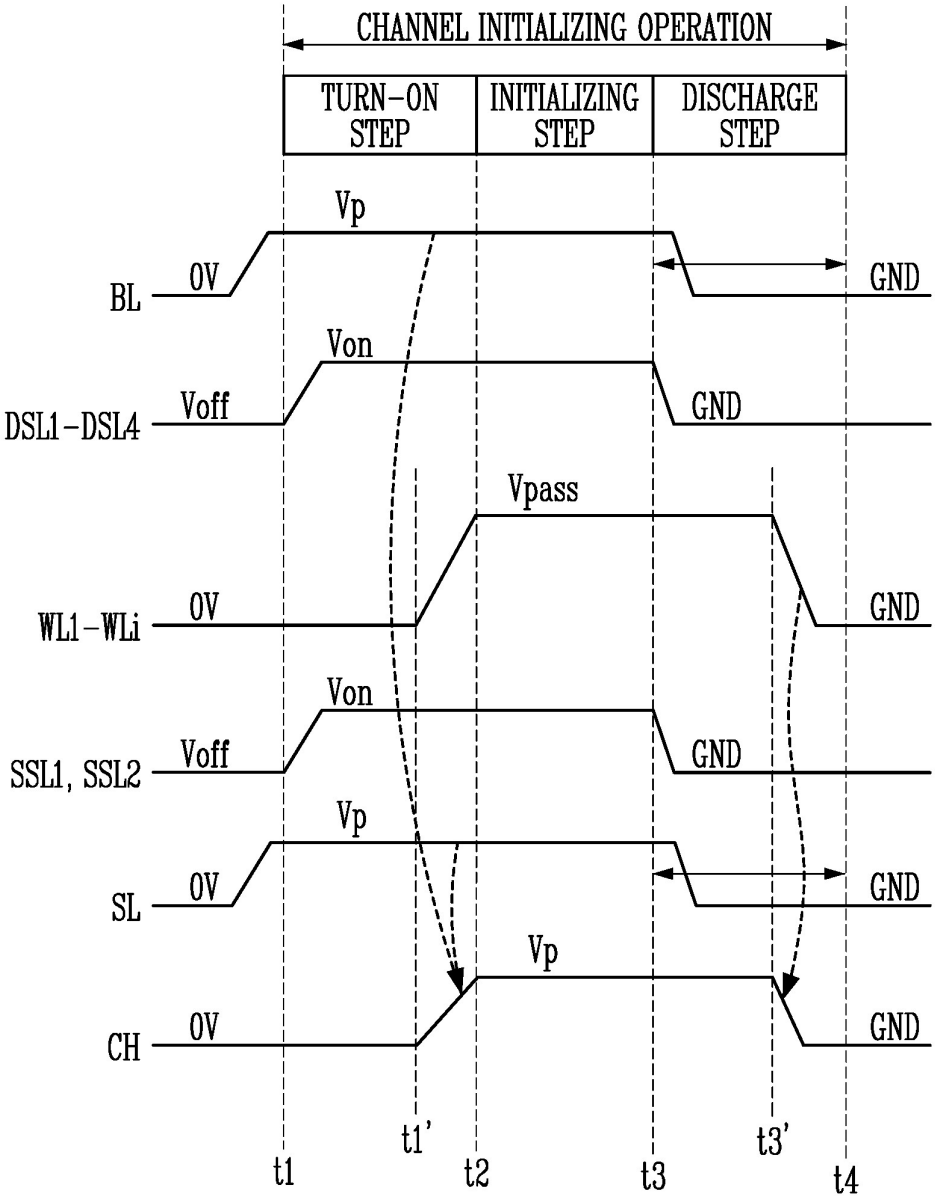

CHANNEL INITIALIZING OPERATION
TURN-ON STEP
INITIALIZING STEP
DISCHARGE STEP
BL
DSL1-DSL4
WL1-WLi
SSL1, SSL2
SL
CH
0V
Vp
Von
Voff
Vpass
GND
t1
t1'
t2
t3
t3'
t4

FIG. 10

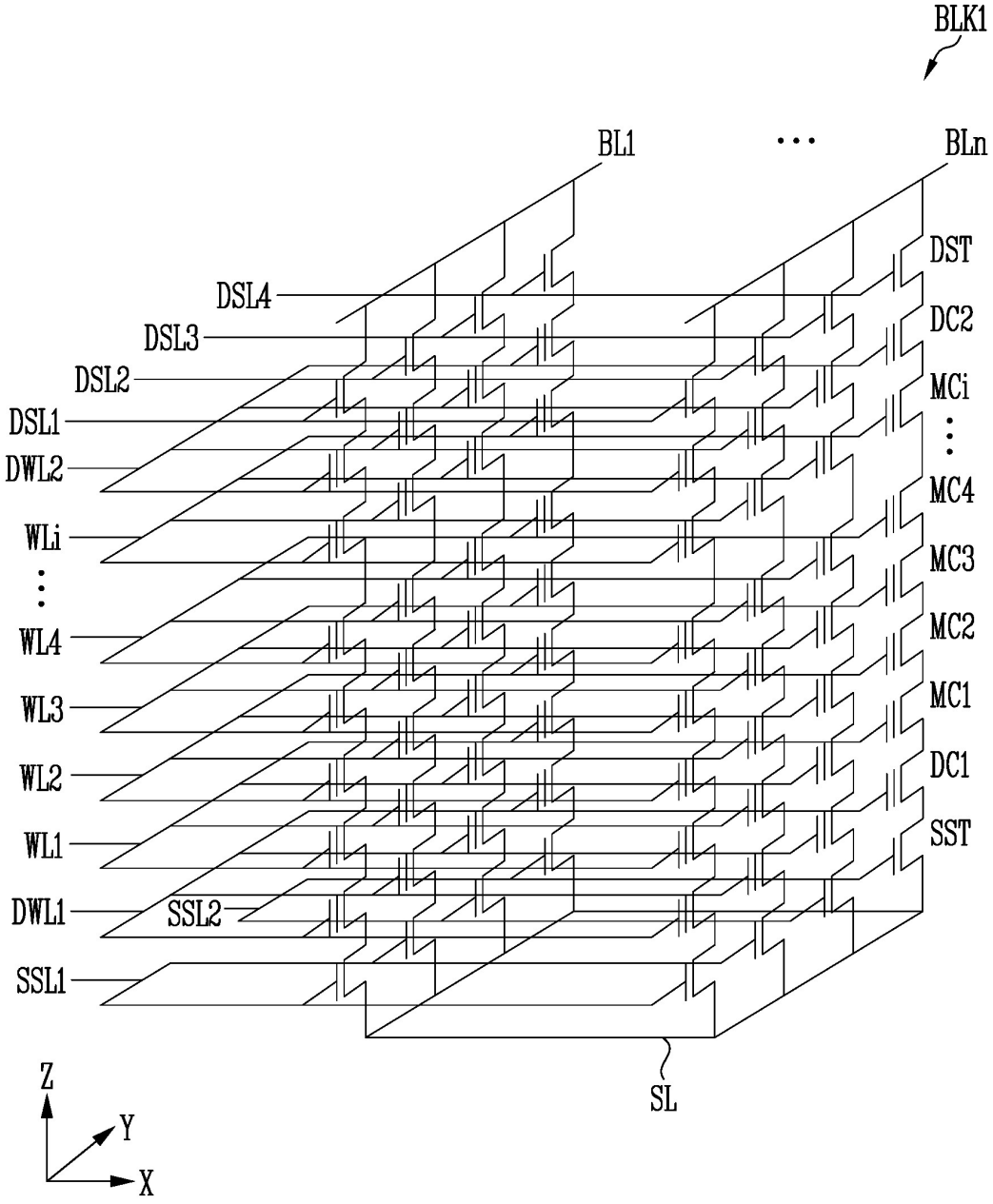

BLK1
BL1
BLn
DST
DSL4
DC2
DSL3
MCi
DSL2
DSL1
MC4
DWL2
WLi
MC3
WL4
MC2
WL3
MC1
WL2
DC1
WL1
SST
DWL1
SSL2
SSL1
SL
Z
Y
X

FIG. 11

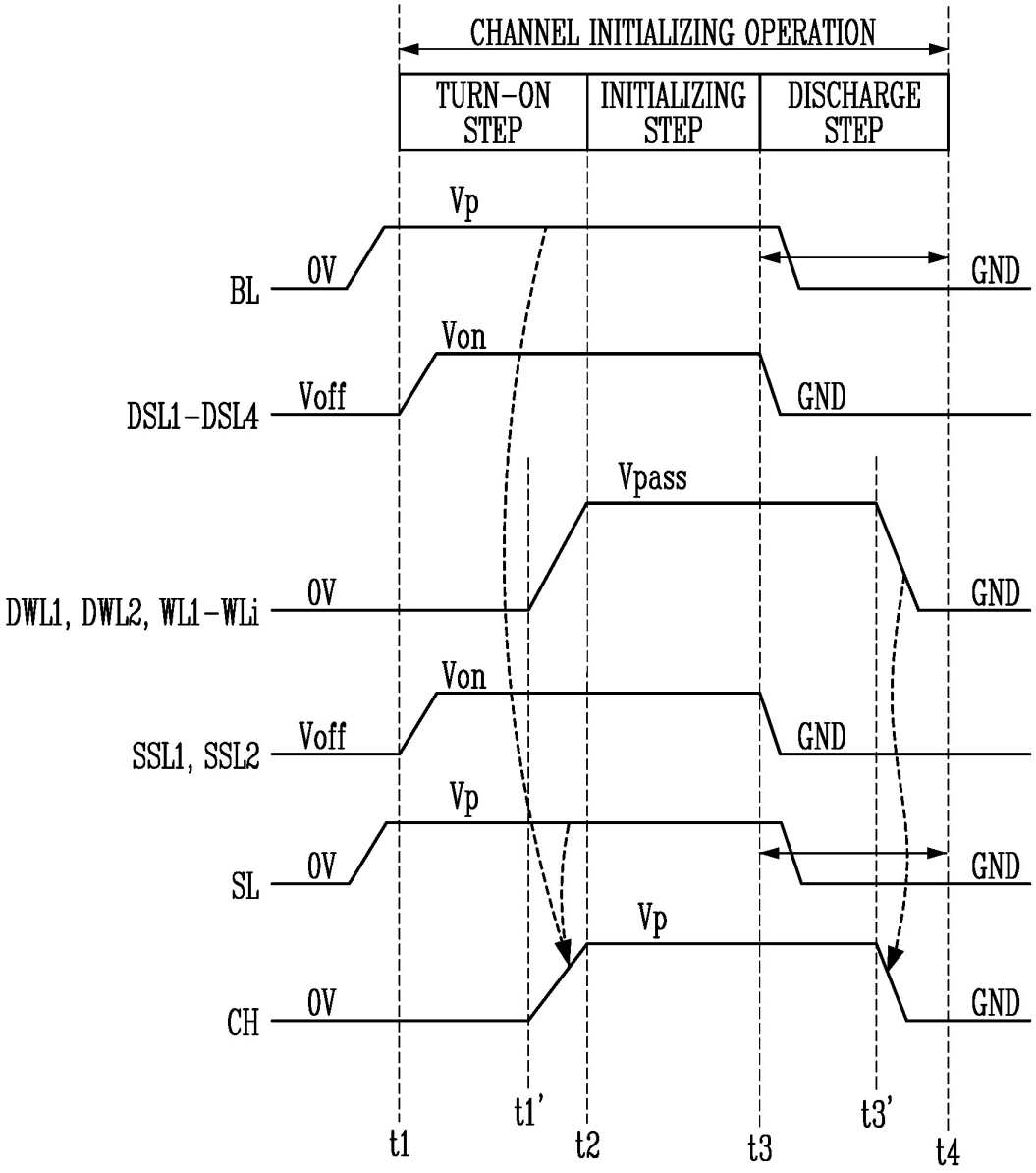

CHANNEL INITIALIZING OPERATION
TURN-ON STEP
INITIALIZING STEP
DISCHARGE STEP
BL
DSL1-DSL4
DWL1, DWL2, WL1-WLi
SSL1, SSL2
SL
CH
0V
Vp
Von
Voff
Vpass
GND
t1
t1'
t2
t3
t3'
t4

FIG. 12

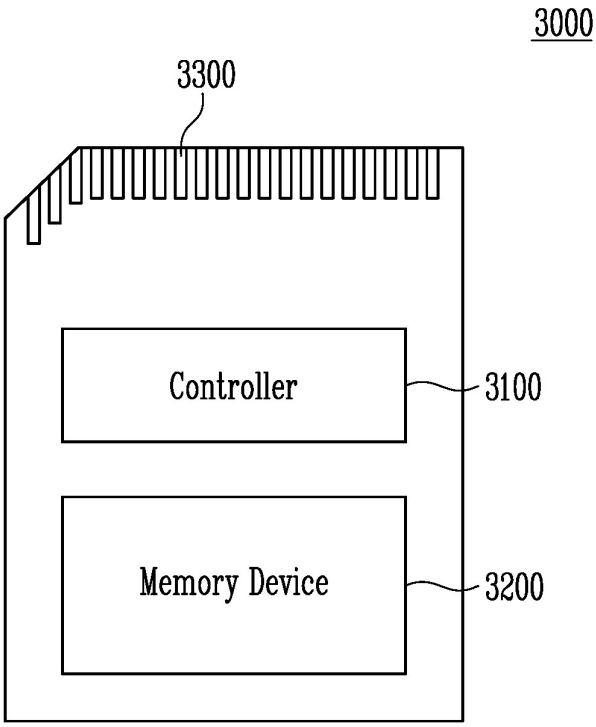
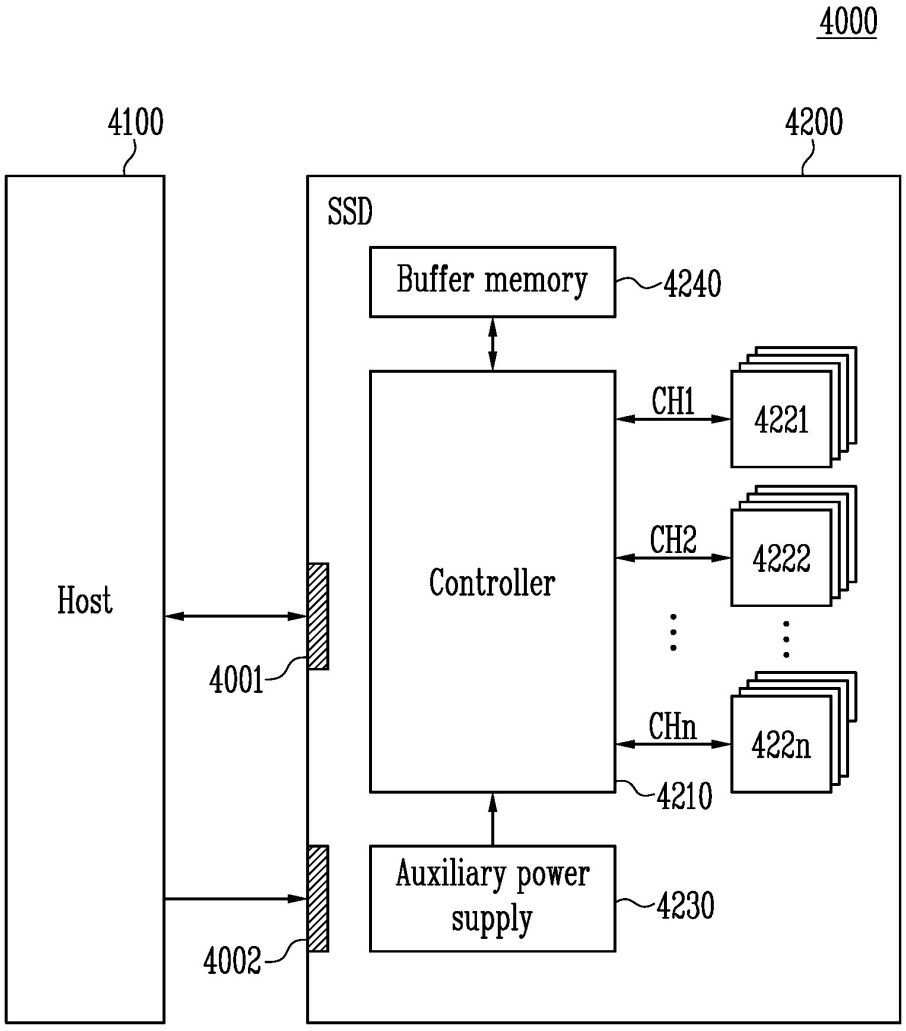


FIG. 13


4000
4100
4200
SSD
Buffer memory
4240
Controller
CH1
4221
CH2
4222
CHn
422n
4210
Host
4001
4002
Auxiliary power supply
4230