

CHALCOGENIDE MATERIAL AND SEMICONDUCTOR MEMORY DEVICE INCLUDING CHALCOGENIDE MATERIAL

5 CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority under 35 U.S.C. § 119(a) to Korean patent application number 10-2021-0138714, filed on October 18, 2021, which is incorporated herein by reference in its entirety.

10 BACKGROUND

Field of Invention

[0002] The present disclosure relates to a material of an electronic device and an electronic device, and more particularly, to a chalcogenide material and a semiconductor memory device
15 including the chalcogenide material.

Description of Related Art

[0003] An electronic device may include a semiconductor memory device for storing data. The semiconductor memory device may include memory cells each of which stores two or
20 more types of logic states. The above-described semiconductor memory device may include a separate device for selecting a memory cell so as to program data in the memory cell, or read data stored in the memory cell.

[0004] In line with miniaturization and high performance of an electronic device, various technologies for increasing a degree of integration of memory cells and an operating speed at low power may be developed.

5 **[0005]** As the semiconductor memory device with the improved degree of integration and operating speed at low power, the next generation memory devices such as a random access memory device (RAM) (e.g. a phase change RAM (PRAM), a magnetic RAM (MRAM), and a resistive RAM (RRAM)) have
10 been proposed. Recently, the development of the next generation memory devices using a chalcogenide material which is beneficial to improve the degree of integration is underway.

SUMMARY

15 **[0006]** According to an embodiment, a chalcogenide material may include germanium (Ge) with a first atomic percent, selenium (Se) with a second atomic percent that is at least twice the first atomic percent of the germanium, and indium (In) with a third atomic percent less than the first atomic percent of the
20 germanium.

[0007] According to an embodiment, a semiconductor memory device may include a first conductive pattern, a second conductive pattern crossing the first conductive pattern, and a chalcogenide material layer disposed between the first

conductive pattern and the second conductive pattern, the chalcogenide material layer including germanium (Ge) with a first atomic percent, selenium (Se) with a second atomic percent that is at least twice the first atomic percent of the germanium,
5 and indium (In) with a third atomic percent less than the first atomic percent of the germanium.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 is a diagram illustrating a semiconductor
10 memory device according to an embodiment of the present disclosure;

[0009] FIGs. 2A, 2B, and 2C are diagrams illustrating an example of a memory cell array of a semiconductor memory device according to embodiments of the present disclosure;

15 **[0010]** FIG. 3A is a graph illustrating a composition of a chalcogenide material; FIG. 3B is a graph illustrating leakage current characteristics according to a composition of a chalcogenide material;

[0011] FIG. 4 is a phase diagram of a binary compound
20 semiconductor including germanium (Ge) and selenium (Se);

[0012] FIGs. 5A and 5B are graphs illustrating a threshold voltage V_{th} of a chalcogenide material according to the content of indium;

[0013] FIGs. 6A and 6B are graphs illustrating a threshold

voltage V_{th} according to a thickness of a chalcogenide material layer;

[0014] FIG. 7 is a graph illustrating leakage current characteristics according to a thickness of a chalcogenide material layer;

[0015] FIGs. 8A and 8B are graphs illustrating a window margin of a chalcogenide material;

DETAILED DESCRIPTION

[0016] The specific structural or functional descriptions disclosed herein are merely illustrative for the purpose of describing embodiments according to the concepts of the present disclosure. Embodiments according to the concepts of the present disclosure can be implemented in various forms and should not be construed as limited to the specific embodiments set forth herein.

[0017] Hereinafter, the terms 'first' and 'second' are used to distinguish one component from another component. As such, the components should not be limited by these terms.

[0018] Various embodiments are directed to a chalcogenide material capable of improving electrical characteristics of a binary compound semiconductor, and a semiconductor memory device including the chalcogenide material.

[0019] FIG. 1 is a diagram illustrating a semiconductor

memory device according to an embodiment of the present disclosure.

[0020] Referring to FIG. 1, the semiconductor memory device may include a memory cell array 100, a column decoder
5 110, and a row decoder 120.

[0021] The memory cell array 100 may be coupled to a plurality of first signal lines and a plurality of second signal lines. The memory cell array 100 may include a plurality of memory cells MC11 to MC33 which are arranged at
10 intersections between the plurality of first signal lines and the plurality of second signal lines. An embodiment of the present disclosure is described below using an example in which the plurality of first signal lines are word lines WL1 to WL3 and the plurality of second signal lines are bit lines BL1 to BL3.
15 However, embodiments of the present disclosure are not limited thereto.

[0022] Each of the memory cells MC11 to MC33 may include a chalcogenide material with which a memory and a select device are embodied at the same time. According to an
20 embodiment of the present disclosure, the memory cells MC11 to MC33 are formed using a material with which a memory and a select device are manufactured at the same time, so that the structure of the semiconductor memory device may be simplified, manufacturing costs may be reduced, and a degree

of integration may be improved.

[0023] A distribution of ions within a chalcogenide material may vary depending on the polarity of a program pulse. Due to such characteristics, each of the memory cells MC11 to MC33
5 may have a threshold voltage which varies according to the polarity of the program pulse. For example, when the first memory cell MC11 is programmed by a first program pulse having a first polarity, the first memory cell MC11 may have a first threshold voltage. When the first memory cell MC11 is
10 programmed by a second program pulse having a second polarity opposite to the first polarity, the first memory cell MC11 may have a second threshold voltage having a different level from the first threshold voltage. An absolute value of the first program pulse may be the same as, or different from an
15 absolute value of the second program pulse. A width of the first program pulse may be the same as, or different from a width of the second program pulse.

[0024] A program state having the first threshold voltage and a program state having the second threshold voltage may
20 be referred to as a set state and a reset state, respectively. For example, the first threshold voltage may have a lower level than the second threshold voltage. The set state may refer to a program state having a first threshold voltage at a relatively low level. The reset state may refer to a program state having

a second threshold voltage at a relatively high level. The chalcogenide material may maintain an amorphous state even when the program pulse which is set to program a memory cell to the reset state and a program pulse which is set to program
5 a memory cell to the set state are applied.

[0025] A read operation of reading data stored in the memory cells MC11 to MC33 may be performed to identify data stored in the memory cells MC11 to MC33 by determining the polarity of the program pulse using a polarity of a read pulse.
10 According to an embodiment, during a read operation, a read pulse having a first polarity or a read pulse having a second polarity may be used. When the program pulse and the read pulse have the same polarity, a first resistance value may be detected. On the other hand, when the polarity of the program
15 pulse is opposite to the polarity of the read pulse, a second resistance value different from the first resistance value may be detected. Therefore, the polarity of the program pulse may be determined based on the resistance value which is detected when the read pulse is applied. The data stored in the memory
20 cells MC11 to MC33 may be identified using the determined polarity of the program pulse.

[0026] The polarity may be determined by a potential difference between a selected bit line and a selected word line. For example, the first polarity may be a positive polarity and

the second polarity may be a negative polarity. For example, the positive polarity may be defined as a polarity when a voltage applied to the selected bit line is greater than a voltage applied to the selected word line. The negative polarity may be defined as a polarity when the voltage applied to the selected bit line is less than the voltage applied to the selected word line.

[0027] The memory cell array 100 may be coupled to the column decoder 110 through the bit lines BL1 to BL3. The column decoder 110 may select at least one of the bit lines BL1 to BL3 in response to a column address C_ADD. The column decoder 110 may transfer operating voltages for a program operation and a read operation to the bit lines BL1 to BL3.

[0028] The memory cell array 100 may be coupled to the row decoder 120 through the word lines WL1 to WL3. The row decoder 120 may select at least one of the word lines WL1 to WL3 in response to a row address R_ADD. The row decoder 120 may transfer operating voltages for a program operation and a read operation to the word lines WL1 to WL3.

[0029] FIGs. 2A, 2B, and 2C are diagrams illustrating an example of the memory cell array 100 of the semiconductor memory device according to embodiments of the present disclosure. A first direction D1, a second direction D2, and a third direction D3 which are defined below may correspond to

directions in which axes crossing each other extend. According to an embodiment, the first direction D1, the second direction D2, and the third direction D3 may correspond to the x-axis, the y-axis, and the z-axis on the XYZ coordinate system, respectively.

[0030] Referring to FIG. 2A, the memory cell array may be configured as a single deck which includes a plurality of first conductive patterns 200, a plurality of second conductive patterns 240, and a plurality of memory cells MC.

10 **[0031]** The plurality of first conductive patterns 200 may extend in the first direction D1 and serve as the plurality of word lines WL1 to WL3. The plurality of second conductive patterns 240 may be arranged on the plurality of first conductive patterns 200 and extend in the second direction D2.

15 The plurality of second conductive patterns 240 may serve as the plurality of bit lines BL1 to BL3.

[0032] Each of the memory cells MC may be arranged at an intersection between the first conductive pattern 200 and the second conductive pattern 240 and may be disposed between

20 the first conductive pattern 200 and the second conductive pattern 240. The memory cell MC may include a chalcogenide material 220.

[0033] The memory cell array may further include a lower electrode 210 which is disposed between the chalcogenide

material (or chalcogenide material layer) 220 and the first
conductive pattern 200, and an upper electrode 230 which is
disposed between the chalcogenide material 220 and the
second conductive pattern 240. Two or more memory cells MC
5 which are arranged next to each other in the first direction D1
may be coupled in parallel with each other on each of the first
conductive patterns 200. A voltage which is applied to each of
the first conductive patterns 200 may be applied to the
chalcogenide material 220 through the lower electrode 210.
10 Two or more memory cells MC which are arranged next to each
other in the second direction D2 may be coupled in parallel with
each other on each of the second conductive patterns 240. A
voltage which is applied to each of the second conductive
patterns 240 may be applied to the chalcogenide material 220
15 through the upper electrode 230.

[0034] Referring to FIG. 2B, the memory cell array may be
configured as a multi-deck in which two or more decks are
stacked on top of each other. According to an embodiment, the
memory cell array may include a first deck DA and a second
20 deck DB over the first deck DA.

[0035] The first deck DA may include the plurality of first
conductive patterns 200, the plurality of second conductive
patterns 240, and a plurality of first memory cells MCA. The
first deck DA may further include a first lower electrode 210A

which is disposed between the first memory cell MCA and the first conductive pattern 200, and a first upper electrode 230A which is disposed between the first memory cell MCA and the second conductive pattern 240.

5 **[0036]** The plurality of first conductive patterns 200, the plurality of second conductive patterns 240, the first lower electrode 210A, and the first upper electrode 230A may have the same structures as the plurality of first conductive patterns 200, the plurality of second conductive patterns 240, the lower
10 electrode 210, and the upper electrode 230 as shown in FIG. 2A, respectively.

[0037] The second deck DB may include the plurality of second conductive patterns 240, a plurality of third conductive patterns 260, and a plurality of second memory cells MCB. The
15 plurality of second conductive patterns 240 may be shared between the first deck DA and the second deck DB.

[0038] The plurality of third conductive patterns 260 may be arranged above the plurality of second conductive patterns 240 and extend to cross the plurality of second conductive patterns
20 240. In an embodiment, the plurality of third conductive patterns 260 may extend in the first direction D1 to cross the plurality of second conductive patterns 240.

[0039] Each of the second memory cells MCB may be arranged at an intersection between the second conductive

pattern 240 and the third conductive pattern 260 and may be disposed between the second conductive pattern 240 and the third conductive pattern 260.

[0040] The second deck DB may further include a second lower electrode 230B which is disposed between the second memory cell MCB and the second conductive pattern 240, and a second upper electrode 210B which is disposed between the second memory cell MCB and the third conductive pattern 260.

[0041] Two or more second memory cells MCB which are arranged next to each other in the second direction D2 may be coupled in parallel with each other on each of the second conductive patterns 240. A voltage which is applied to each of the second conductive patterns 240 may be applied to the second memory cell MCB through the second lower electrode 230B. Two or more second memory cells MCB which are arranged next to each other in the first direction D1 may be coupled in parallel with each other on each of the third conductive patterns 260. A voltage which is applied to each of the third conductive patterns 260 may be applied to the second memory cell MCB through the second upper electrode 210B.

[0042] The plurality of first conductive patterns 200 and the plurality of third conductive patterns 260 may serve as a plurality of word lines (WL11 to WL13 and WL21 to WL23). The plurality of second conductive patterns 240 may serve as the

plurality of bit lines BL1 to BL3.

[0043] The first memory cell MCA may include a first chalcogenide material (or first chalcogenide material layer) 220A and the second memory cell MCB may include a second
5 chalcogenide material (or second chalcogenide material layer) 220B.

[0044] Referring to FIG. 2C, the memory cell array may be realized as a three-dimensional memory cell array. The three-dimensional memory cell array may include a plurality of first
10 conductive patterns 200C, a plurality of second conductive patterns 240C crossing the plurality of first conductive patterns 200C, and a plurality of chalcogenide materials (or a plurality of chalcogenide material layers) 220C formed at interconnections between the plurality of first conductive
15 patterns 200C and the plurality of second conductive patterns 240C.

[0045] Each of the first conductive patterns 200C may be in the form of a flat panel which extends in the first direction D1 and the second direction D2. The plurality of first conductive
20 patterns 200C may be stacked on top of each other so as to be separated from each other in the third direction D3. The plurality of first conductive patterns 200C may serve as the plurality of word lines WL1 to WL3.

[0046] The plurality of second conductive patterns 240C may

extend in the third direction D3 to pass through the plurality of first conductive patterns 200C. Though not shown in FIG. 2C, a plurality of bit lines which are coupled to the plurality of second conductive patterns 240C may be arranged over the plurality of second conductive patterns 240C. Each of the chalcogenide material 220C may surround a sidewall of each of the second conductive patterns 240C corresponding thereto. Some areas of the chalcogenide materials 220C arranged at the intersections between the plurality of first conductive patterns 200C and the plurality of second conductive patterns 240C may serve as memory cells. Though not shown in FIG. 2C, a dielectric layer may be arranged between each of the first conductive patterns 200C and each of the chalcogenide materials 220C.

15 **[0047]** A memory and a select device may be embodied at the same time using each of the chalcogenide materials 220, 220A, 220B, and 220C as shown in FIGs. 2A, 2B, and 2C. Each of the chalcogenide materials 220, 220A, 220B, and 220C may mainly include a binary compound semiconductor of germanium (Ge) and selenium (Se), and may further include indium (In). A composition ratio between Ge, Se, and In in which form each of the chalcogenide materials 220, 220A, 220B, and 220C may be controlled so as to ensure desirable electrical characteristics. According to an embodiment, each of the chalcogenide

materials 220, 220A, 220B, and 220C may have a composition which includes germanium (Ge), selenium (Se) having an atomic percent twice or more than twice as great as an atomic percent of germanium, and indium (In) having an atomic
5 percent smaller than each of those of germanium and selenium. In an embodiment, the sum of the atomic percent of germanium, the atomic percent of selenium, and the atomic percent of indium may be substantially 100 % (e.g., at least 99%). In an embodiment, the sum of the atomic percent of
10 germanium, the atomic percent of selenium, and the atomic percent of indium may be equal to or greater than 99.5 %, 99.7 %, or 99.9 %. In other words, according to an embodiment of the present disclosure, the composition of each of the chalcogenide materials 220, 220A, 220B, and 220C may
15 exclude arsenic (As) which is an element in a high risk group. For example, if a chalcogenide material includes arsenic, disposal costs and environmental pollution associated with a memory device including the chalcogenide material may be increased and safety concerns may arise in processing the
20 chalcogenide material. When arsenic is excluded, waste disposal costs and environmental pollution may be reduced and the safety of a workplace for processing the chalcogenide material may be improved. In an embodiment, a chalcogenide material according to an embodiment of the present disclosure

may contain substantially no arsenic.

[0048] According to an embodiment of the present disclosure, a composition ratio of germanium, selenium, and indium may be controlled so as to be in a range which stably enables an operation of a memory cell. According to an embodiment, germanium may be included within a range from 25 at% to 32 at% in the chalcogenide material 220, 220A, 220B, or 220C, selenium may be included within a range from 50 at% to 66 at% in the chalcogenide material 220, 220A, 220B, or 220C, and indium may be included within a range from 1 at% to 12 at% in the chalcogenide material 220, 220A, 220B, or 220C. The chalcogenide material 220, 220A, 220B, or 220C may maintain an amorphous state at a temperature of 600 °C or less. Hereinafter, electrical characteristics which may be ensured by controlling the above-described composition ratio in various experimental groups will be described.

[0049] FIG. 3A is a graph illustrating a composition of a chalcogenide material. FIG. 3B is a graph illustrating leakage current characteristics according to the composition of the chalcogenide material. In FIG. 3B, the x-axis represents a voltage ratio normalized by a threshold voltage V_{th} and the y-axis represents a current.

[0050] Referring to FIG. 3A and [Table 1] below, a split A may correspond to a control group, and splits B, C, D, E, F, G,

and H may correspond to experimental groups. A percentage as shown in FIG. 3A and [Table 1] may indicate an atomic percent (at%).

[Table 1]

Split	A	B	C	D	E	F	G	H
Material	Ge/As/ Se/In	Ge/Se			Ge/Se/In			
Ge	See FIG. 3A	73.4%	40.0%	33.2%	31.8%	30.4%	27.6%	25.6%
As		–	–	–	–	–	–	–
Se		26.6%	60.0%	66.8%	65.5%	65.1%	64.4%	63.4%
In		–	–	–	2.7%	4.6%	8.0%	11.0%

5 **[0051]** The split A may correspond to a chalcogenide material with electrical characteristics which may stably enable an operation of a memory cell. The split A may provide a reference value for identifying the electrical characteristics of the experimental groups. The split A may include germanium,
 10 selenium, indium, and arsenic. Each of the splits B, C, and D may be a chalcogenide material which excludes arsenic.

[0052] Referring to [Table 1] and FIGs. 3A and 3B, even if arsenic is excluded, when the atomic percent of selenium is increased to be at least twice that of germanium, good leakage
 15 current characteristics as in the splits D, E, F, G, and H, may be obtained. For example, although it is known that excluding arsenic may deteriorate leakage current characteristics, the leakage current characteristics may be improved, rather than being deteriorated, when the atomic percent of selenium is
 20 increased to be at least twice that of germanium. Therefore,

leakage current characteristics of a binary compound semiconductor which includes arsenic and selenium may be ensured by increasing the atomic percent of selenium twice or more than twice as much as that of germanium.

5 **[0053]** In an embodiment, leakage current characteristics may be ensured by controlling the content of germanium in the chalcogenide material to be in the range from about 25 at% (e.g., from 24.5 to 25.4 at%) to about 32 at% (e.g., from 31.5 to 32.4 at%) and controlling the content of selenium to be in
10 the range from about 50 at% to about 66 at%(for example, in the range from about 56 at% to about 66 at%). For example, as shown in splits E, F, G, and H of Table 1 and FIGs. 3A and 3B, leakage current characteristics may be sufficiently ensured when the atomic percent of germanium is in the range from 25
15 at% to 32 at% and the atomic percent of selenium is in the range from 63 at% to 66 at%.

[0054] FIG. 4 is a phase diagram of a binary compound semiconductor including germanium (Ge) and selenium (Se).

[0055] Referring to FIG. 4, in a composition where
20 germanium and selenium are dominant, α -GeSe and GeSe₂ may have phase stability. Therefore, the phase stability of the binary compound semiconductor based on germanium and selenium may be ensured by controlling the atomic percent of selenium to be twice or more than twice as much as that of the

atomic percent of germanium.

[0056] Referring to FIGs. 3A and 3B, [Table 1], and FIG. 4, by controlling the atomic percent of selenium to be twice or more than twice as much as the atomic percent of germanium
5 by about 1 at% to about 12 at%, both phase stability and leakage current characteristics may be ensured. For example, when germanium is included at a ratio of about [N] at% in the chalcogenide material, about [2N] at% selenium may be included in the chalcogenide material, or selenium may be
10 included in a range from about [2N+1] to about [2N+12] at%, N being an integer.

[0057] As a result of performing an annealing process up to a temperature of 600 °C with the contents of germanium and selenium limited to the above ratios, the chalcogenide material
15 having the above-described composition and including germanium and selenium may maintain an amorphous state at a temperature of up to 600 °C. As described above, according to an embodiment of the present disclosure, because a chalcogenide material maintains an amorphous state at a
20 temperature of 600 °C or less, crystallization of the chalcogenide material caused by heat generated during the manufacturing processes of a semiconductor memory device may be substantially prevented. Therefore, according to an embodiment of the present disclosure, stability and reliability

of the manufacturing processes may be improved.

[0058] The split D which includes only the binary compound semiconductor of germanium and selenium may have a threshold voltage higher than a target range. Indium may have a lower bandgap than GeSe_2 . Thus, by adding indium to a binary compound semiconductor including germanium and selenium, a threshold voltage of the Ge and Se-based binary compound semiconductor may be reduced. Indium may be doped into the chalcogenide material by a sputtering process.

A composition ratio of indium may be controlled by adjusting a ratio of power which is applied to sputtering equipment. Hereinafter, electrical characteristics of a chalcogenide material depending on the indium content will be described with reference to FIGs. 5A and 5B.

[0059] FIGs. 5A and 5B are graphs illustrating the threshold voltage V_{th} of a chalcogenide material depending on the content of indium. FIG. 5A is a graph illustrating the threshold voltage V_{th} of the splits D, E, F, G, and H when an initial pulse is applied after the manufacturing processes are completed.

FIG. 5B is a graph illustrating the threshold voltage V_{th} of the splits D, E, F, G, and H when the same pulse as the initial pulse is repeatedly applied.

[0060] Referring to FIGs. 5A and 5B, the threshold voltage distribution width of each of the splits E, F, G, and H may be

reduced compared to a threshold voltage distribution width of the split D. By including indium in a range from about 1 at% (e.g., from 0.5 to 1.4 at%) to about 12 at% (e.g., from 11.5 to 12.4 at%) in the chalcogenide material including germanium, selenium and indium, such as the splits E, F, G, and H, the threshold voltage may be controlled to be in a target range (e.g., from 3 V to 7 V). For example, the chalcogenide material including indium in a range from 2 at% to 11 at%.

[0061] FIGs. 6A and 6B are graphs illustrating the threshold voltage V_{th} according to a thickness of a chalcogenide material layer. FIGs. 6A and 6B show the threshold voltage V_{th} obtained by changing the thickness of the chalcogenide material layer which has the same composition as the split F among the splits E, F, G, and H which have effective electrical characteristics. FIG. 6A is a graph illustrating the threshold voltage V_{th} of the splits A, F, F1 and F2 when the initial pulse is applied after the completion of the manufacturing processes. FIG. 6B is a graph illustrating the threshold voltage V_{th} of the splits A, F, F1, and F2 when the same pulse as the initial pulse is repeatedly applied. The splits F1 and F2 in the experimental group may have substantially the same composition as the split F and have a different thickness from the split F. For example, in the embodiment of FIGs. 6A and 6B, the splits F, F1 and F2 may correspond to chalcogenide material layers having

thicknesses of 200 Å, 175 Å, and 150 Å, respectively.

[0062] Referring to FIGs. 6A and 6B, by controlling a deposition thickness of the chalcogenide material layer having the same composition ratio so as to be in a range from 150 Å to 5 200 Å, the chalcogenide material layer having a threshold voltage in a target range (e.g., from 3 V to 7 V) may be provided.

[0063] FIG. 7 is a graph illustrating leakage current characteristics according to a thickness of a chalcogenide 10 material layer. FIG. 7 illustrates leakage current characteristics with respect to the splits A, F, F1, and F2 as shown in FIGs. 6A and 6B.

[0064] Referring to FIG. 7, when the deposition thickness of the chalcogenide material layer having the same composition 15 ratio is controlled to be in the range from 150 Å to 200 Å, better leakage current characteristics than the split A may be provided.

[0065] FIGs. 8A and 8B are graphs illustrating a window margin of a chalcogenide material. FIGs. 8A and 8B are graphs 20 illustrating window margins of the splits F and A among the splits E, F, G, and H which have effective electrical characteristics.

[0066] Referring to FIGs. 8A and 8B, on the basis of a program voltage of 4.5 V, the threshold voltage V_{th} of the split

A in a set state may be 3.98 V and the threshold voltage V_{th} of the split A in a reset state may be 5.3 V. Therefore, the split A may have a window margin of 1.32 V. On the basis of the program voltage of 6 V, the threshold voltage V_{th} of the split F in the set state may be 5.1 V and the threshold voltage V_{th} of the split F in the reset state may be 6.78 V. Therefore, the split F may have a window margin of 1.68 V which is higher than that (i.e., 1.32V) of the split A.

[0067] As described above, a chalcogenide material including germanium, selenium which has an atomic percent twice or more than twice as much an atomic percent of germanium, and indium which has a smaller atomic percent than each of the atomic percent of germanium and the atomic percent of selenium according to an embodiment of the present disclosure may be used as materials for forming a memory and a select device.

[0068] A chalcogenide material according to an embodiment of the present disclosure may have desirable threshold voltage switching characteristics as described above (e.g., as shown in FIGs. 3B, 5A, 5B, 6A, 6B, and 7). Therefore, the chalcogenide material according to an embodiment of the present disclosure may be used to form a select device of various electronic devices. According to an embodiment of the present disclosure, a chalcogenide material may be applied as a material of a

select device which is connected to a variable resistance memory cell which includes a phase-change material layer.

[0069] According to the present disclosure, electrical characteristics of a chalcogenide material may be improved by
5 forming the chalcogenide material in which a binary compound including germanium (Ge) and selenium (Se) is combined with indium (In).

WHAT IS CLAIMED IS:

1. A chalcogenide material comprising:

germanium with a first atomic percent, selenium with a second atomic percent that is at least twice the first atomic percent of the germanium, and indium with a third atomic percent less than the first atomic percent of the germanium.

2. The chalcogenide material of claim 1, wherein a total sum of the first atomic percent of the germanium, the second atomic percent of the selenium, and the third atomic percent of the indium is substantially 100 %.

3. The chalcogenide material of claim 1, wherein the first atomic percent of the germanium is in a range from 25 at% to 32 at%.

4. The chalcogenide material of claim 1, wherein the second atomic percent of the selenium is in a range from 50 at% to 66 at%.

5. The chalcogenide material of claim 1, wherein the third atomic percent of the indium is in a range from 1 at% to 12 at%.

6. The chalcogenide material of claim 1, wherein the first

atomic percent of the germanium is $[N]$ at%, N being an integer,
and

wherein the second atomic percent of the selenium is in a
range from $[2N+1]$ at% to $[2N+12]$ at%.

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7. The chalcogenide material of claim 1, wherein the
second atomic percent of the selenium is in a range from 56 at%
to 66 at%.

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8. The chalcogenide material of claim 1, wherein the
material maintains an amorphous state at a temperature of
600 °C or less.

9. The chalcogenide material of claim 1, wherein the first
15 atomic percent of the germanium is in a range from 25 at% to
32 at%,

wherein the second atomic percent of the selenium is in
the range from 63 at% to 66 at%, and

wherein the third atomic percent of the indium is in the
20 range from 2 at% to 11 at%.

10. A semiconductor memory device, comprising:
a first conductive pattern;
a second conductive pattern crossing the first conductive

pattern; and

a chalcogenide material layer disposed between the first
conductive pattern and the second conductive pattern, the
chalcogenide material layer including germanium with a first
5 atomic percent, selenium with a second atomic percent, and
indium with a third atomic percent,

wherein the second atomic percent is at least twice that of
the first atomic percent, and the third atomic percent is less
than the first atomic percent .

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11. The semiconductor memory device of claim 10,
wherein a total sum of the first atomic percent of the germanium,
the second atomic percent of the selenium, and the third atomic
percent of the indium is substantially 100 %.

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12. The semiconductor memory device of claim 10,
wherein the first atomic percent of the germanium is in a range
from 25 at% to 32 at%.

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13. The semiconductor memory device of claim 10,
wherein the second atomic percent of the selenium is in a range
from 50 at% to 66 at%.

14. The semiconductor memory device of claim 10,

wherein the third atomic percent of the indium is in a range from 1 at% to 12 at%.

15. The semiconductor memory device of claim 10,
5 wherein the first atomic percent of the germanium is [N] at%, N being an integer, and

wherein the second atomic percent of the selenium is in a range from $[2N+1]$ at% to $[2N+12]$ at%.

10 16. The semiconductor memory device of claim 10, wherein the second atomic percent of the selenium is in a range from 56 at% to 66 at%.

17. The semiconductor memory device of claim 10,
15 wherein the chalcogenide material layer maintains an amorphous state at a temperature of 600 °C.

18. The semiconductor memory device of claim 10,
wherein the first atomic percent of the germanium is in a range
20 from 25 at% to 32 at%,

wherein the second atomic percent of the selenium is in the range from 63 at% to 66 at%, and

wherein the third atomic percent of the indium is in the range from 2 at% to 11 at%.

19. The semiconductor memory device of claim 10, wherein the chalcogenide material layer has a thickness in a range from 150 Å to 200 Å.

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20. The semiconductor memory device of claim 10, wherein the chalcogenide material layer surrounds a sidewall of the second conductive pattern.

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