

**MICROELECTROMECHANICAL SYSTEM (MEMS) BOND
RELEASE STRUCTURE AND METHOD OF WAFER TRANSFER
FOR THREE-DIMENSIONAL INTEGRATED CIRCUIT (3D IC)
INTEGRATION**

Field of Disclosure

[0001] Various embodiments described herein relate to three-dimensional integrated circuit (3D IC) devices, and more particularly, to 3D IC stacking using a microelectromechanical mechanical system (MEMS) bond release structure.

Background

[0002] Three-dimensional circuit integration by stacking integrated circuits in multiple tiers allows circuit designers to achieve benefits of improved power, performance, area and cost (PPAC) beyond the Moore's law scaling limit. Various schemes of three-dimensional integrated circuit (3D IC) stacking, including silicon-in-package (SiP) 3D IC stacking schemes such as wire-bond, flip-chip bond, through-silicon via (TSV) and silicon interposer technologies have been developed in order to achieve higher densities in circuitry, inter-tier links and vias. 3D ICs with multi-tier stacking are desirable in devices in which form factor requirements are stringent, such as smartphones and other mobile devices. In addition to conventional SiP 3D IC stacking schemes, sequential monolithic 3D IC (sM3DIC) technology has been developed. In sM3DIC, a single crystal semiconductor layer is sequentially integrated and bonded onto a finished lower-tier complementary metal oxide semiconductor (CMOS) wafer, and an upper-tier CMOS is then built upon it.

[0003] The sM3DIC technology is currently considered to have the potential of achieving huge PPAC benefits with high inter-tier link/via densities, on the order of more than 1,000,000 links per square millimeter. However, the sM3DIC technology currently faces several significant process integration challenges that need to be overcome before it can become commercially feasible. Such challenges may include, for example, low thermal budget/process requirements for upper-tier source/drain (S/D) ohmic contact, channel/well dopant activation, S/D recrystallization, and potential contamination problems related to copper interconnect processes when the lower-tier wafer completed by a back end-of-line (BEOL) process is brought to the front end-of-line (FEOL).

[0004] Another 3D IC stacking scheme, called parallel monolithic 3D IC (pM3DIC), may be capable of achieving inter-tier link/via densities on the order of about 100,000 to 1,000,000 links per square millimeter. In pM3DIC, a wafer-to-wafer (W2W) hybrid bonding (metal-to-metal and oxide-to-oxide fusion bonding) technique is used which includes a high-precision W2W alignment process having a tolerance of less than 0.5 μ m in combination with a very thin upper-tier wafer having a thickness of less than 5 μ m after removal of the bulk silicon. The high-precision W2W alignment process allows the landing pad size to be reduced while the very thin upper-tier wafer allows the size of through-silicon and through-oxide inter-tier vias to be reduced, thereby achieving an increase the inter-tier link/via density.

[0005] Even though the pM3DIC approach is currently considered to be capable of offer an intermediate level of inter-tier link/via density within a shorter development period, significant process challenges may still exist. For example, while it is possible to thin the upper-tier wafer down to 5 μ m or less by using existing wafer thinning techniques, such as mechanical wafer backgrinding including a coarse grinding and a fine polish followed by chemical-mechanical polish (CMP), CMOS device characteristics are found to drift when the wafer is thinned down to 25 μ m or less due to particle-induced stress impact onto the CMOS device during the mechanical grinding process in the bumping line. Moreover, with existing mechanical wafer grinding and CMP technologies, it may still be difficult to achieve a reasonable total thickness variation (TTV) of 1 μ m or less.

[0006] Another approach for wafer thinning for a CMOS imager utilizes selective wet etch on a P+ etch stop layer. However, such an approach may present challenges for obtaining a reasonable process window to control precise and uniform layer thickness, to control defect density, and to manage boron doping diffusion during the remaining CMOS process. Alternatively, a silicon-on-insulator (SOI) wafer may provide an acceptable solution for precise wafer thinning down to the "buried oxide" (BOX) layer, that is, a layer including a silicon (Si) layer and a silicon dioxide (SiO₂) layer processed by coarse and fine grinding, followed by CMP, and then followed by selective wet etch of Si and SiO₂. The SOI wafer may be used as the starting wafer for the upper-tier. However, once the wafer is processed by mechanical grinding through the bumping line, the wafer may often be contaminated with heavy metals such as gold, silver, tin, or other metals in practice. With heavy metal contamination, the wafer can no longer be

practically processed in the BEOL to add additional backside metals with fine pitch metal layers, thus losing 3D integration flexibility in terms of interconnect configurations. Moreover, other factors such as wafer cost, material utilization, and throughput considerations, for example, may not be favorable for pM3DIC integration.

SUMMARY

[0007] Exemplary embodiments are directed to a microelectromechanical system (MEMS) bond release structure for wafer transfer and a method of making the same, and a three-dimensional integrated circuit device and a method of making the same by using the MEMS bond release structure for wafer transfer.

[0008] In an embodiment, a microelectromechanical system (MEMS) bond release structure is provided, the structure comprising: a carrier wafer; a MEMS sacrificial release layer on the carrier wafer; a semiconductor oxide layer on the MEMS sacrificial release layer; and an active semiconductor layer on the semiconductor oxide layer.

[0009] In another embodiment, a method of making a microelectromechanical system (MEMS) bond release structure is provided, the method comprising: providing a carrier wafer; providing a MEMS sacrificial release layer on the carrier wafer; providing a semiconductor oxide layer on the MEMS sacrificial release layer; and providing an active semiconductor layer on the semiconductor oxide layer.

[0010] In another embodiment, a three-dimensional integrated circuit device is provided, the device comprising: a substrate; a first tier of one or more integrated circuits comprising one or more metal layers and one or more inter-layer dielectric (ILD) layers; a second tier of one or more integrated circuits comprising one or more metal layers and one or more ILD layers; and a first BOX layer in contact with at least one of the ILD layers in the second tier of one or more integrated circuits, wherein one or more portions of the first BOX layer and one or more portions of said at least one of the ILD layers in the second tier of one or more integrated circuits are removed to form one or more vias through the first BOX layer and said at least one of the ILD layers in the second tier.

[0011] In yet another embodiment, a method of making a three-dimensional integrated circuit device is provided, the method comprising: providing a substrate; forming a first tier of one or more integrated circuits comprising one or more metal layers and one or more inter-layer dielectric (ILD) layers; forming a second tier of one or more integrated circuits comprising one or more metal layers and one or more ILD layers; forming a

first BOX layer in contact with at least one of the ILD layers in the second tier of one or more integrated circuits; and forming one or more vias through the first BOX layer and said at least one of the ILD layers in the second tier.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The accompanying drawings are presented to aid in the description of embodiments and are provided solely for illustration of the embodiments and not limitations thereof.

[0013] FIG. 1 is a cross-sectional view of a carrier wafer and a microelectromechanical system (MEMS) sacrificial release layer, illustrating an embodiment of a structure in the initial step of fabricating a MEMS bond release structure.

[0014] FIG. 2 is a cross-sectional view of a carrier wafer, a MEMS sacrificial release layer, and an oxide layer, illustrating an embodiment of a structure in the second step of fabricating a MEMS bond release structure.

[0015] FIG. 3 is a cross-sectional view of a plurality of MEMS posts or pillars on a carrier wafer, illustrating an embodiment of a structure in the third step of fabricating a MEMS bond release structure.

[0016] FIG. 4A is a cross-sectional view of an embodiment of a transfer substrate, which is initially provided separately from the carrier wafer as shown in FIGs. 1-3, for fabricating a MEMS bond release structure.

[0017] FIG. 4B is a cross-sectional view of an embodiment of a carrier substrate comprising the structure of FIG. 3 before the transfer substrate is bonded to the carrier substrate.

[0018] FIG. 5A is a cross-sectional view of the embodiment of the transfer substrate of FIG. 4A flipped upside down before it is bonded to the carrier substrate.

[0019] FIG. 5B is a cross-sectional view of the carrier substrate of FIG. 4B ready for accepting bonding of the flipped-over transfer substrate of FIG. 5A.

[0020] FIG. 6 is a cross-sectional view of an embodiment of a bonded structure after the flipped-over transfer substrate is bonded to the carrier substrate.

[0021] FIG. 7 is a cross-sectional view of an embodiment showing separation of a portion of the transfer substrate from the carrier substrate while leaving another portion of the transfer substrate intact with the carrier substrate.

[0022] FIG. 8 is a cross-sectional view of a MEMS pillar/post bond release structure after separation of a portion of the transfer substrate.

- [0023] FIG. 9 is a cross-sectional view of an embodiment of a finished MEMS pillar/post bond release structure.
- [0024] FIGs. 10A and 10B are cross-sectional and top views, respectively, of an embodiment of a MEMS post/pillar bond release structure in which outer and inner MEMS posts or pillars have different widths.
- [0025] FIG. 11 is a cross-sectional view of an alternate embodiment of a MEMS bond release structure with a continuous MEMS sacrificial release layer.
- [0026] FIG. 12 is a cross-sectional view of a first tier (Tier 1) of integrated circuits prepared before one or more additional tiers of integrated circuits are stacked on Tier 1.
- [0027] FIG. 13 is a cross-sectional view of a second tier (Tier 2) of integrated circuits prepared on a MEMS bond release structure, embodiments of which are described above with references to FIGs. 1-11, before Tier 2 is stacked on Tier 1 of integrated circuits as shown in FIG. 12.
- [0028] FIG. 14 is a cross-sectional view illustrating the alignment of Tier 1 and Tier 2 of integrated circuits as shown in FIGs. 12 and 13 before they are bonded together.
- [0029] FIG. 15 is a cross-sectional view illustrating wafer-to-wafer (W2W) bonding of Tier 1 and Tier 2 of integrated circuits as shown in FIG. 14.
- [0030] FIG. 16 is a cross-sectional view illustrating an embodiment of a two-tier 3D IC after the MEMS sacrificial release layer of the MEMS bond release structure is removed.
- [0031] FIG. 17 is a cross-sectional view of the 3D IC of FIG. 16 after removing the remaining thin oxide layer on the BOX layer to form a smooth top surface.
- [0032] FIG. 18 is a cross-sectional view of the 3D IC of FIG. 17 after vias are formed in the BOX layer and the inter-layer dielectric (ILD) layer directly beneath the BOX layer in Tier 2.
- [0033] FIG. 19 is a cross-sectional view of the 3D IC of FIG. 18 after metal interconnects are formed as part of an additional metal layer over the vias in Tier 2.
- [0034] FIG. 20 is a cross-sectional view of the 3D IC of FIG. 19 after additional ILD layers are formed on the additional metal layer over the vias.
- [0035] FIG. 21 is a cross-sectional view of an embodiment of a three-tier 3D IC, in which Tier 2 and Tier 1 of integrated circuits are formed and combined together by using the MEMS bond release structure.

DETAILED DESCRIPTION

[0036] Aspects of the disclosure are described in the following description and related drawings directed to specific embodiments. Alternate embodiments may be devised without departing from the scope of the disclosure. Additionally, well known elements will not be described in detail or will be omitted so as not to obscure the relevant details of the disclosure.

[0037] The word “exemplary” is used herein to mean “serving as an example, instance, or illustration.” Any embodiment described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other embodiments. Likewise, the term “embodiments” does not require that all embodiments include the discussed feature, advantage or mode of operation.

[0038] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the embodiments. As used herein, the singular forms “a,” “an,” and “the,” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises,” “comprising,” “includes,” or “including,” when used herein, specify the presence of stated features, integers, steps, operations, elements, or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, or groups thereof. Moreover, it is understood that the word “or” has the same meaning as the Boolean operator “OR,” that is, it encompasses the possibilities of “either” and “both” and is not limited to “exclusive or” (“XOR”), unless expressly stated otherwise.

[0039] FIG. 1 is a cross-sectional view of a carrier wafer 102 and a microelectromechanical system (MEMS) sacrificial release layer 104 on top of the carrier wafer 102, illustrating an embodiment of a structure in the initial step of fabricating a MEMS bond release structure. In an embodiment, the carrier wafer 102 comprises a silicon wafer. The MEMS sacrificial release layer 104 may comprise a material such as molybdenum (Mo), germanium (Ge), germanium oxide (GeOx), silicon oxide (SiOx) including silicon dioxide (SiO₂), or other types of sacrificial material. In an embodiment, the MEMS sacrificial release layer 104 may be provided on the carrier wafer 102 by using a conventional deposition process, such as a chemical vapor

deposition (CVD), a plasma-enhanced chemical vapor deposition (PECVD), a physical vapor deposition (PVD) process, for example.

[0040] FIG. 2 is a cross-sectional view of the carrier wafer 102, the MEMS sacrificial release layer 104 on top of the carrier wafer 102, and an oxide layer 106 for oxide-to-oxide fusion bonding on top of the MEMS sacrificial release layer 104, illustrating an embodiment of a structure in the second step of fabricating the MEMS bond release structure. In an embodiment, the oxide layer 106 comprises a thin oxide material such as silicon dioxide (SiO_2) for oxide-to-oxide bonding. In an embodiment, the oxide layer 106 may be provided on the MEMS sacrificial release layer 104 by using a conventional deposition process such as a CVD process, for example. In a further embodiment, the oxide layer 106 may be provided on the MEMS sacrificial release layer 104 by a plasma-enhanced chemical vapor deposition (PECVD) process, for example.

[0041] FIG. 3 is a cross-sectional view of a MEMS post/pillar bond release structure having a plurality of MEMS posts or pillars 108a, 108b, 108c, ... on the carrier wafer 102, illustrating an embodiment of a structure in the third step of fabricating the MEMS bond release structure. In an embodiment, each of the MEMS posts or pillars 108a, 108b, 108c, ... comprises a MEMS sacrificial release layer 104 on top of the carrier wafer 102 and an oxide layer 106 on top of the MEMS sacrificial release layer 104. In an embodiment, the MEMS posts or pillars 108a, 108b, 108c, ... as shown in FIG. 3 may be formed by patterning and etching the continuous MEMS sacrificial release layer 104 and the oxide layer 106 as shown in FIG. 2, for example.

[0042] Although the cross-sectional view of FIG. 3 shows a plurality of MEMS posts or pillars 108a, 108b, 108c, ... as being substantially identical to one another with substantially equal spacing, the MEMS posts or pillars on a given carrier wafer need not have the same width, and spacings between adjacent MEMS posts or pillars need not be identical, as will be described below with reference to an embodiment as shown in FIGs. 10A and 10B. Moreover, in an alternate embodiment, MEMS posts or pillars need not be fabricated, and the MEMS sacrificial release layer 104 may be formed instead as a continuous layer, which will be described below with reference to an embodiment as shown in FIG. 11.

[0043] FIG. 4A is a cross-sectional view of an embodiment of a transfer substrate 200, which is initially provided separately from the carrier wafer 102 as shown in FIGs. 1-3. In the embodiment shown in FIG. 4A, the transfer substrate 200 comprises a bulk wafer

202 having opposite surfaces 204 and 206, and two semiconductor oxide layers 208 and 210 disposed on the surfaces 204 and 206 of the bulk wafer 202, respectively. In this embodiment, two semiconductor oxide layers 208 and 210 are thermally-oxidized and positioned to sandwich the bulk wafer 202. Alternatively, only one semiconductor oxide layer 208 is provided for illustration on the surface 204 of the bulk wafer 202. In an embodiment, the bulk wafer 202 of the transfer substrate 200 comprises a silicon wafer, whereas each of the semiconductor oxide layers 208 and 210 comprises SiO₂. In an embodiment, the SiO₂ layers 208 and 210 may be formed on the bulk silicon wafer 202 by thermally-oxidizing the surfaces of the bulk silicon wafer 202, for example.

[0044] In an embodiment, a dopant is implanted to a portion 212 near the surface 204 of the bulk wafer 202 in contact with the semiconductor oxide layer 208. In an embodiment in which the bulk wafer 202 is sandwiched by two semiconductor oxide layers 208 and 210 as shown in FIG. 4A, dopant implantation may be applied to only a portion near one of the surfaces of the bulk wafer in contact with one of the semiconductor layers, for example, the portion 212 near the surface 204 of the bulk wafer 202 in contact with the semiconductor oxide layer 208. In an embodiment, an ion implantation process such as H⁺ delta implantation may be applied to the portion 212 near the surface 204 of the bulk wafer 202, for example. FIG. 4B is a cross-sectional view of a carrier substrate 300, which includes the carrier wafer 102 and the plurality of MEMS posts or pillars 108a, 108b, 108c, ... each having a MEMS sacrificial release layer 104 and an oxide layer 106 as shown in FIG. 3, before the transfer substrate 200 of FIG. 4A is flipped over and bonded to the carrier substrate 300 of FIG. 4B.

[0045] In practice, it is usually easier to implant a dopant from the top surface 204 rather than the bottom surface 206 of the bulk wafer 202 of the transfer substrate 200, the initial orientation of which is shown in FIG. 4A, consistent with the initial orientation of the MEMS post/pillar bond release structure as shown in FIG. 4B. In an embodiment, the transfer substrate 200 is flipped upside down, as shown in the cross-sectional view of FIG. 5A, before it is bonded to the carrier substrate 300, the cross-sectional view of which is shown in FIG. 5B.

[0046] FIG. 6 is a cross-sectional view of an embodiment of a bonded structure which is a combination of the carrier substrate 300 and the transfer substrate 200 after the flipped-over transfer substrate 200 is bonded to the carrier substrate 300. In the embodiment shown in FIG. 6, the semiconductor oxide layer 208, which is in contact

with the surface 204 of the bulk wafer 202 to which H⁺ delta implantation was applied, is directly bonded to the oxide layer 106 of each of the MEMS posts or pillars 108a, 108b, 108c,

[0047] FIG. 7 is a cross-sectional view of an embodiment showing separation of a portion of the transfer substrate 200 from the carrier substrate 300, while leaving the H⁺ delta implanted portion 212 of the bulk wafer 202 and the semiconductor oxide layer 208 on the surface 204 of the H⁺ delta implanted portion 212 of the bulk wafer 202 intact with the carrier substrate 300. In an embodiment, an undoped portion 220 of the bulk wafer 202 and the semiconductor oxide layer 210 on the surface 206 opposite the H⁺ delta implanted portion 212 of the bulk wafer 202 are separated from the H⁺ delta implanted portion 212 of the bulk wafer 212. Separation of the undoped portion 220 of the bulk wafer 202 from the H⁺ delta implanted portion 212 of the bulk wafer 202 may be achieved by cleavage, for example.

[0048] FIG. 8 is a cross-sectional view of a MEMS pillar/post bond release structure after the undoped portion of the bulk wafer of the transfer substrate is separated or cleaved from the H⁺ delta implanted portion 212 of the bulk wafer 202. As shown in FIG. 8, the H⁺ delta implanted portion 212 of the bulk wafer 202 and the semiconductor oxide layer 208 on the surface 204 of the H⁺ delta implanted portion 212 of the bulk wafer 202 are now integrated parts of the MEMS post/pillar bond release structure, which also includes the carrier wafer 102 and the plurality of MEMS posts or pillars 108a, 108b, 108c, ... each having a MEMS sacrificial release layer 104 and a thin oxide layer 106.

[0049] In an embodiment, the semiconductor oxide layer 208, which may comprise an SiO₂ layer, is directly positioned on the thin oxide layer 106 of each of the MEMS posts or pillars 108a, 108b, 108c, In an embodiment in which the bulk wafer 202 of the transfer substrate 200 comprises silicon and the semiconductor oxide layer 208 of the transfer substrate 200 comprises SiO₂, the H⁺ delta implanted portion 212 of the bulk wafer 202 and the semiconductor oxide layer 208 together form a silicon-on-insulator (SOI) substrate 400. Such a SOI substrate 400 may also be regarded as a SiO₂ BOX layer in the fabrication of 3D ICs, which will be described below with reference to FIGs. 13-21.

[0050] FIG. 9 is a cross-sectional view of an embodiment of a finished MEMS pillar/post bond release structure, after the SOI substrate 400 is subjected to wafer

surface finishing processes. In an embodiment, the finishing processes may include, for example, a post-bonding chemical mechanical polish (CMP) process to smooth the top surface 230 of the H⁺ delta implanted portion 212 bulk wafer 202 resulting from the separation or cleavage of the undoped portion of the bulk wafer from the MEMS pillar/post bond release structure as described above with reference to FIG. 7. In a further embodiment, the finishing processes may also include ozone oxidation treatment for the SOI substrate 400, for example.

[0051] FIGs. 10A and 10B are side/cross-sectional and top views, respectively, of an embodiment of a MEMS post/pillar bond release structure across a semiconductor wafer, in which some of the MEMS posts or pillars may have different widths. In FIGs. 10A and 10B, a plurality of inner MEMS posts or pillars 108a, 108b, 108c, ... are provided as part of the MEMS post/pillar bond release structure similar to the structure described above with reference to FIG. 9. In addition to the inner MEMS posts or pillars 108a, 108b, 108c, ... , FIGs. 10A and 10B also shows a plurality of outer MEMS posts or pillars 150a, 150b, ... surrounding the inner MEMS posts or pillars 108a, 108b, 108c, In an embodiment, each of the outer MEMS posts or pillars 150a, 150b, ... has a width greater than the width of each of the inner MEMS posts or pillars 108a, 108b, 108c, ... on the carrier wafer 102 to provide sufficient structural support of the entire bonded-wafers during the sacrificial layer release process. Other than having different widths, the outer MEMS posts or pillars 150a, 150b, ... have the same two-layer structure as that of the inner MEMS posts or pillars 108a, 108b, 108c, ... , including a MEMS sacrificial release layer 104 and a thin oxide layer 106. In a further embodiment, a sealing ring 160 is also provided along the outer perimeter of the carrier wafer 102. In an embodiment, the sealing ring 160 also has the same two-layer structure as that of the inner and outer MEMS posts or pillars, including a MEMS sacrificial release layer 104 and a thin oxide layer 106.

[0052] FIG. 11 is a cross-sectional view of an alternate embodiment of a MEMS bond release structure. Instead of the MEMS posts or pillars described above, the MEMS bond release structure in the embodiment shown in FIG. 11 includes a continuous MEMS sacrificial release layer 504 on the carrier wafer 102 to form a carrier substrate 500. In an embodiment, the SOI substrate 400, which comprises a semiconductor oxide layer 208 and a layer of bulk wafer 202, which may be doped by an H⁺ delta implantation process, for example, is bonded to the carrier substrate 500. In an

embodiment, the carrier wafer 102 comprises silicon whereas the bulk wafer 202 comprises H⁺ delta doped silicon, for example. In an embodiment, the MEMS sacrificial release layer 504, which is continuously disposed across the carrier wafer 102, may comprise a sacrificial material such as Mo, Ge, GeO_x or SiO_x including SiO₂, for example. In an embodiment, the semiconductor oxide layer 208 of the SOI substrate 400 comprises SiO₂.

[0053] FIGS. 12-21 are cross-sectional views illustrating embodiments of processes for making a 3D IC by stacking multiple tiers of integrated circuits using one or more MEMS bond release structures, embodiments of which are described above with respect to FIGS. 1-11. FIG. 12 is a cross-sectional view of a first tier (Tier 1) of integrated circuits. A wafer 1202 for Tier 1, which may comprise a silicon bulk handler or a silicon-on-insulator (SOI) substrate, may be prepared in a conventional manner. In the embodiment shown in FIG. 12, the integrated circuits in Tier 1 may include one or more metal layers (M1, M2, M3, M4 layers) 1204, 1206, 1208 and 1210, and one or more inter-layer dielectric (ILD) layers (ILD-0, ILD-1, ILD-2, ILD-3 layers) 1212, 1214, 1216 and 1218.

[0054] A plurality of vias may also be provided for electrical interconnects between some or all of the metal layers through one or more of the ILD layers, including, for example, vias (V1, V2, V3) 1220, 1222 and 1224 as shown in FIG. 12. In an embodiment, an additional ILD layer (ILD-4 layer) 1230 is provided on the top metal layer (M4 layer) 1210 for oxide bonding with a second tier (Tier 2) of integrated circuits, which will be described below with reference to FIG. 13. Referring to FIG. 12, a plurality of bonding pads such as bonding pads 1240 and 1242 are provided on top of at least some of the metal contacts in the top metal layer (M4 layer) 1210 in the top ILD layer 1230 for bonding with corresponding bonding pads in the second tier of integrated circuits.

[0055] FIG. 13 is a cross-sectional view of a second tier (Tier 2) of integrated circuits prepared on a MEMS bond release structure, embodiments of which are described above with references to FIGS. 1-11. In FIG. 13, a MEMS post/pillar bond release structure as shown in FIG. 10A is provided, which comprises a carrier wafer 102, a plurality of inner MEMS posts or pillars 108a, 108b, 108c, ... , a plurality of outer MEMS posts or pillars 150a, 150b, ... and a sealing ring 160 each having a MEMS sacrificial release layer 104 and a thin oxide layer 106, and a SOI substrate 400, also

called a BOX layer, which may comprise a silicon dioxide (SiO_2) layer and an active silicon layer. Referring to FIG. 13, a plurality of metal layers (M1, M2, M3, M4 layers) 1302, 1304, 1306 and 1308 and a plurality of ILD layers (ILD-0, ILD-1, ILD-2, ILD-3 layers) 1310, 1312, 1314 and 1316 are provided on top of the SOI substrate or BOX layer 400.

[0056] Similar to Tier 1, Tier 2 of integrated circuits may also include a plurality of vias (V1, V2, V3) 1320, 1322 and 1324 provided for electrical interconnects between some or all of the metal layers through one or more of the ILD layers. Again, similar to Tier 1, Tier 2 of integrated circuits may also include a top ILD layer (ILD-4 layer) 1330 on the top metal layer (M4 layer) 1308 for oxide bonding. Furthermore, a plurality of bonding pads such as bonding pads 1340 and 1342 are provided on top of at least some of the metal contacts in the top metal layer (M4 layer) 1308 in the top ILD layer 1330 for bonding with corresponding bonding pads in the first tier (Tier 1) of integrated circuits.

[0057] FIG. 14 is a cross-sectional view illustrating the alignment of Tier 1 and Tier 2 of integrated circuits before they are bonded together. In FIG. 14, Tier 2 of integrated circuits is flipped upside down from the orientation in the cross-sectional view of FIG. 13. In FIG. 14, after Tier 2 of integrated circuits attached to the BOX layer 400 of the MEMS post/pillar bond release structure is flipped upside down, the bonding pads 1342 and 1340 of Tier 2 are aligned with the bonding pads 1240 and 1242 of Tier 1, respectively. As shown in FIG. 14, the width of each bonding pad of a given tier need not be the identical to the width of the corresponding bonding pad of the other tier, as long as the corresponding pads are aligned with one another such that sufficiently good electrical connections, i.e., sufficient contact areas are established once the pads are bonded to one another.

[0058] FIG. 15 is a cross-sectional view illustrating the wafer-to-wafer (W2W) bonding of Tier 2 and Tier 1 of integrated circuits. In FIG. 15, upon bonding of Tier 2 to Tier 1, the bonding pads 1342 and 1340 of Tier 2 are in direct contact with the bonding pads 1240 and 1242 of Tier 1, respectively, thereby establishing electrical connections between the corresponding bonding pads. Moreover, the top ILD layer (ILD-4 layer) 1230 of Tier 1 is also in direct contact with the top ILD layer (ILD-4 layer) 1330 of Tier 2, thereby forming a two-tier 3D IC.

[0059] FIG. 16 is a cross-sectional view illustrating an embodiment of the two-tier 3D IC after the MEMS sacrificial release layer 104 in each of the inner MEMS posts or pillars 108a, 108b, 108c, ... , the outer MEMS posts or pillars 150a, 150b, ... and the sealing ring 160 is removed, thus leaving the thin oxide layer 106 in each of the inner and outer MEMS posts or pillars and the sealing ring intact with the BOX layer 400. In an embodiment in which the MEMS bond release structure includes a plurality of MEMS posts or pillars as shown in FIG. 2 and described above, the thin oxide layer 106 after removal of the MEMS sacrificial release layer 104 would be in the form of small protrusions on the BOX layer 400 as shown in FIG. 16. The MEMS sacrificial release layer 104 may be removed easily by release-etching process, either in wet or dry etch chemistry. For example, XeF_2 is widely used as a dry-etch release chemistry for Mo or Si sacrificial layer. With the removal of the MEMS sacrificial release layer, the carrier wafer 102 is completely released or detached from Tier 2 of integrated circuits.

[0060] FIG. 17 is a cross-sectional view of the 3D IC of FIG. 16 after removing the remaining thin oxide layer 106 on the BOX layer 400 to form a smooth top surface 1702 of the BOX layer 400. The top surface 1702 of the BOX layer 400 may be smoothed by a conventional polishing process, such as a chemical mechanical polish (CMP) process in back end-of-line (BEOL) in an embodiment. FIG. 18 is a cross-sectional view of the 3D IC of FIG. 17 after a plurality of vias 1802a, 1802b, 1802c, ... are provided through the BOX layer 400 and the ILD layer (ILD-0 layer) 1310 of Tier 2 directly beneath the BOX layer 400. The vias 1802a, 1802b, 1802c may be formed by removing designated portions of the BOX layer 400 and corresponding portions of the ILD layer (ILD-0 layer) 1310 directly beneath the BOX layer 400 in a conventional manner. After the via formation, these vias are filled with metal (e.g., Cu), then followed by the CMP process typically used in the BEOL.

[0061] FIG. 19 is a cross-sectional view of the 3D IC of FIG. 18 after one or more metal interconnects 1902a, 1902b, 1902c, ... are formed as part of an additional metal layer (M5 layer) over the vias 1802a, 1802b, 1802c, FIG. 20 is a cross-sectional view of the 3D IC of FIG. 19 after one or more additional ILD layers (ILD-5, ILD-6 layers) 2002 and 2004 are formed on the M5 layer in an embodiment. In a further embodiment, another additional metal layer (M6 layer) having metal interconnects 2006a, 2006b, 2006c, ... are provided on top of the ILD-5 layer 2002 and within the ILD-6 layer 2004. In yet a further embodiment, a plurality of vias 2008a, 2008b, 2008c,

... are provided in the ILD-5 layer 2002 to allow for electrical connections between metal interconnects of M5 and M6 layers. In an embodiment, one or more bonding pads such as bonding pads 2010a and 2010b are formed on top of one or more metal interconnects of the M6 layer.

[0062] FIG. 21 is a cross-sectional view of an embodiment of a three-tier 3D IC, in which Tier 2 and Tier 1 of integrated circuits are formed and combined together by the bonding processes described above with references to FIGs. 12-20. In the embodiment shown in FIG. 21, an additional tier, Tier 3, of integrated circuits is formed on top of Tier 2 in the same manner as the formation and bonding of Tier 2 to Tier 1 described above. In FIG. 21, bonding pads 2110a and 2110b are provided in Tier 3 and aligned with bonding pads 2010a and 2010b of Tier 2, respectively, in a wafer-to-wafer (W2W) hybrid-bonding process, for example.

[0063] In FIG. 21, an additional BOX layer 2120, which is formed by a silicon dioxide (SiO_2) layer and an active silicon layer in an embodiment of a MEMS bond release structure described above, is provided for Tier 3. Furthermore, one or more metal layers (M5, M6 layers) and one or more ILD layers (ILD-5, ILD-6 layers) may be provided on top of the BOX layer 2120, and one or more bonding pads 2130a and 2130b may be provided on top of the M6 layer in an embodiment to allow an additional tier of integrated circuits (not shown) to be bonded to Tier 3 in a W2W hybrid-bonding process. Multiple tiers of integrated circuits may be stacked in a similar manner to produce a multi-tier 3D IC.

[0064] Although some of the embodiments described above relate to the processing of silicon integrated circuits, the principles of the disclosure are also applicable to integrated circuits based on other materials. In other embodiments, the semiconductor materials of upper-tier wafers may be other than silicon, such as silicon germanium (SiGe), gallium arsenide (GaAs), indium phosphide (InP), gallium nitride (GaN), or other semiconductor. Moreover, the lower-tier wafer can be non-semiconductors such as insulative substrate materials. For example glass, quartz substrate, or even glass panel used in flat panel displays or sensors may be used as insulative substrate materials for the lower-tier wafer. Moreover, the MEMS bond release structure according to embodiments of the disclosure allows precise upper-tier wafer thinning and thickness control by controlling the thickness of the BOX layer for each tier, rather than by

conventional mechanical grinding processes such as coarse and fine grinding, thus achieving a very small wafer total thickness variation (TTV).

[0065] Moreover, by avoiding the need for a conventional mechanical wafer grinding process, adverse effects on electrical properties of circuit elements in the upper tiers due to mechanical stress introduced during mechanical wafer grinding may be avoided. Furthermore, with the MEMS sacrificial layer release process, higher throughput in manufacturing of multi-tier 3D IC devices may be achieved because MEMS sacrificial layer release by etching may be faster than time-consuming mechanical grinding processes. By using the MEMS bond release structure according to embodiments of the disclosure in the manufacturing of 3D IC devices, lower material cost, higher yield and better material utilization may be achieved by avoiding waste of semiconductor materials and mechanical stress on the circuit elements resulting from conventional mechanical grinding processes.

[0066] While the foregoing disclosure describes illustrative embodiments, it should be noted that various changes and modifications could be made herein without departing from the scope of the appended claims. The functions, steps or actions in the method and apparatus claims in accordance with the embodiments described herein need not be performed in any particular order unless explicitly stated otherwise. Furthermore, although elements may be described or claimed in the singular, the plural is contemplated unless limitation to the singular is explicitly stated.

CLAIMS**WHAT IS CLAIMED IS:**

1. A microelectromechanical system (MEMS) bond release structure, comprising:

a carrier wafer;

a MEMS sacrificial release layer on the carrier wafer;

a semiconductor oxide layer on the MEMS sacrificial release layer; and

an active semiconductor layer on the semiconductor oxide layer.

2. The structure of claim 1, wherein the semiconductor oxide layer comprises a silicon dioxide (SiO₂) layer.

3. The structure of claim 2, wherein the active semiconductor layer comprises an active silicon layer on the SiO₂ layer.

4. The structure of claim 1, wherein the MEMS sacrificial release layer comprises a plurality of MEMS posts spaced apart from one another.

5. The structure of claim 4, wherein each of the MEMS posts comprises a sacrificial release material.

6. The structure of claim 5, wherein the sacrificial release material comprises a material selected from the group consisting of molybdenum (Mo), germanium (Ge), germanium oxide (GeO_x) and silicon oxide (SiO_x).

7. The structure of claim 5, wherein each of the MEMS posts further comprises an oxide material on the sacrificial release material for bonding the sacrificial release material with the semiconductor oxide layer.

8. The structure of claim 4, wherein the MEMS posts comprise one or more inner MEMS posts and one or more outer MEMS posts at least partially surrounding said one or more inner MEMS posts on the carrier wafer.

9. The structure of claim 1, wherein the MEMS sacrificial release layer comprises a continuous sacrificial release layer on the carrier wafer.

10. The structure of claim 1, wherein the semiconductor oxide layer and the active semiconductor layer together form a buried oxide (BOX) layer.

11. A method of making a microelectromechanical system (MEMS) bond release structure, comprising:

providing a carrier wafer;

providing a MEMS sacrificial release layer on the carrier wafer;

providing a semiconductor oxide layer on the MEMS sacrificial release layer;

and

providing an active semiconductor layer on the semiconductor oxide layer.

12. The method of claim 11, wherein the step of providing the MEMS sacrificial release layer comprises:

depositing a sacrificial release material on the carrier wafer; and

depositing an oxide material on the sacrificial release material.

13. The method of claim 12, wherein the step of depositing the sacrificial release material comprises the step of depositing a material selected from the group consisting of molybdenum (Mo), germanium (Ge), germanium oxide (GeO_x) and silicon oxide (SiO_x).

14. The method of claim 12, wherein the step of depositing the sacrificial release material comprises the step of depositing the sacrificial release material by chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), or physical vapor deposition (PVD).

15. The method of claim 12, wherein the step of depositing the oxide material comprises the step of depositing the oxide material by chemical vapor

deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), or physical vapor deposition (PVD).

16. The method of claim 11, further comprising the steps of:
providing a transfer substrate comprising a bulk wafer and at least one semiconductor oxide layer on a surface of the bulk wafer; and
applying H⁺ delta implantation to a first portion of the bulk wafer near the surface of the bulk wafer in contact with the semiconductor oxide layer.

17. The method of claim 16, further comprising bonding the transfer substrate to a carrier substrate comprising the carrier wafer, the MEMS sacrificial release layer, the semiconductor oxide layer and the active semiconductor layer.

18. The method of claim 17, wherein the step of bonding the transfer substrate to the carrier substrate comprises the step of bonding the semiconductor oxide layer of the transfer substrate to the MEMS sacrificial release layer.

19. The method of claim 18, further comprising:
separating a second portion of the bulk wafer of the transfer substrate from the carrier substrate; and
leaving the first portion of the bulk wafer with H⁺ delta implantation in contact with the semiconductor oxide layer.

20. The method of claim 19, wherein the semiconductor oxide layer of the transfer substrate comprises silicon dioxide (SiO₂), and wherein the bulk wafer of the transfer substrate comprises silicon (Si).

21. A three-dimensional integrated circuit device, comprising:
a substrate;
a first tier of one or more integrated circuits comprising one or more metal layers and one or more inter-layer dielectric (ILD) layers;
a second tier of one or more integrated circuits comprising one or more metal layers and one or more ILD layers; and

a first buried oxide (BOX) layer in contact with at least one of the ILD layers in the second tier of one or more integrated circuits, wherein one or more portions of the first BOX layer and one or more portions of said at least one of the ILD layers in the second tier of one or more integrated circuits are removed to form one or more vias through the first BOX layer and said at least one of the ILD layers in the second tier.

22. The device of claim 21, further comprising one or more metal interconnects over said one or more vias.

23. The device of claim 22, further comprising one or more metal layers and one or more ILD layers on the metal interconnects.

24. The device of claim 23, further comprising a plurality of bonding pads on said one or more metal layers.

25. The device of claim 21, wherein the first BOX layer comprises a silicon (Si) layer and a silicon dioxide (SiO₂) layer.

26. The device of claim 21, wherein the first tier of one or more integrated circuits further comprises a first set of one or more bonding pads, wherein the second tier of one or more integrated circuits further comprises a second set of one or more bonding pads, and wherein at least one of the bonding pads in the first set is connected to at least one of the bonding pads in the second set.

27. The device of claim 21, further comprising:

a third tier of one or more integrated circuits comprising one or more metal layers and one or more ILD layers;

a second BOX layer in contact with at least one of the ILD layers in the third tier of one or more integrated circuits, wherein one or more portions of the second BOX layer and one or more portions of said at least one of the ILD layers in the third tier of one or more integrated circuits are removed to form one or more vias through the second BOX layer and said at least one of the ILD layers in the third tier.

28. The device of claim 27, wherein the second tier of one or more integrated circuits further comprises a second set of one or more bonding pads, wherein the third tier of one or more integrated circuits further comprises a third set of one or more bonding pads, and wherein at least one of the bonding pads in the second set is connected to at least one of the bonding pads in the third set.

29. The device of claim 21, wherein the substrate comprises a silicon-on-insulator (SOI) substrate.

30. The device of claim 21, wherein the substrate comprises a silicon (Si) bulk handler.

31. A method of making a three-dimensional integrated circuit device, comprising:

providing a substrate;

forming a first tier of one or more integrated circuits comprising one or more metal layers and one or more inter-layer dielectric (ILD) layers;

forming a second tier of one or more integrated circuits comprising one or more metal layers and one or more ILD layers;

forming a first buried oxide (BOX) layer in contact with at least one of the ILD layers in the second tier of one or more integrated circuits; and

forming one or more vias through the first BOX layer and said at least one of the ILD layers in the second tier.

32. The method of claim 31, wherein the step of forming the second tier of one or more integrated circuits comprises aligning one or more bonding pads in the second tier of one or more integrated circuits with one or more bonding pads in the first tier of one or more integrated circuits.

33. The method of claim 32, wherein the step of forming the second tier of one or more integrated circuits further comprises bonding said one or more bonding pads in the second tier of one or more integrated circuits with said one or more bonding pads in the first tier of one or more integrated circuits.

34. The method of claim 31, wherein the step of forming the second tier of one or more integrated circuits comprises forming the second tier of one or more integrated circuits on a microelectromechanical system (MEMS) bond release structure comprising a carrier wafer, a MEMS sacrificial release layer on the carrier wafer, and the first BOX layer on the MEMS sacrificial release layer.

35. The method of claim 34, further comprising separating the carrier wafer from the second tier of one or more integrated circuits by releasing the MEMS sacrificial release layer.

36. The method of claim 35, further comprising:
forming a one or more metal interconnects over said one or more vias;
forming one or more metal layers and one or more ILD layers on the metal interconnects; and
forming a plurality of bonding pads on said one or more metal layers.

37. The method of claim 31, further comprising:
forming a third tier of one or more integrated circuits comprising one or more metal layers and one or more ILD layers; and
forming a second BOX layer in contact with at least one of the ILD layers in the third tier of one or more integrated circuits.

38. The method of claim 37, further comprising forming one or more vias through the second BOX layer and said at least one of the ILD layers in the third tier.

39. The method of claim 37, wherein the step of forming the third tier of one or more integrated circuits comprises forming the third tier of one or more integrated circuits on a microelectromechanical system (MEMS) bond release structure comprising a carrier wafer, a MEMS sacrificial release layer on the carrier wafer, and the second BOX layer on the MEMS sacrificial release layer.

40. The method of claim 39, further comprising separating the carrier wafer from the third tier of one or more integrated circuits by releasing the MEMS sacrificial release layer.