ABSTRACT

LAYOUT METHOD FOR SCALABLE DESIGN OF THE AGGRESSIVE RAM CELLS USING A POLY-CAP MASK

A method for integrating salicide and self-aligned contact processes in the fabrication of integrated circuits by using a poly cap mask and a special layout technique is described. A pair of gate electrodes and associated source and drain regions are formed overlying a semiconductor substrate wherein nitride spacers are formed on sidewalls of the gate electrodes. A poly-cap layer is deposited overlying the gate electrodes and source and drain regions. The poly-cap layer is selectively removed overlying one of the source and drain regions between the gate electrode pair where a self-aligned contact is to be formed and removed over one of the gate electrode pair. An insulating layer is deposited over the surface of the semiconductor substrate. The planned self-aligned contact opening is made through the insulating layer to the source/drain region to be contacted wherein the contact opening partially overlies the poly-cap layer over the adjacent gate electrode of the pair. The self-aligned contact opening is filled with a conducting layer to complete fabrication of the integrated circuit device.

(FIGURE 1A IS SUGGESTED FOR PUBLICATION)