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(54) A METHOD AND AN APPARATUS FOR FORMING A CHARACTER FROM A PATTERN OF SEPARATE DISPLAY PICTURE ELEMENTS

(71) We, KABUSHIKI KAISHA SEIKOSHA, a Japanese company of 2—5 Kyobashi, Chuo-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to methods and apparatus for forming a character, such as, for example, a letter, numeral or symbol from separate display picture elements.

In general when forming a letter, numeral, symbol or the like by means of a matrix of dots, the character formed is relatively legible within a given range of sizes. However, outside this given range of sizes there is a tendency for some letters to become illegible. For example, the letters "E" and "F" which are constructed solely from horizontal and vertical lines offer no serious problem irrespective of their size. In contrast, letters including oblique lines, such as "R" and "X", become very difficult to read as their size is increased. Figure 2 shows the letter "R" formed of a dot matrix of 7 rows and 5 columns and Figure 3 shows the same letter but increased in size by a factor of 2. As will be apparent, the magnified letter is relatively illegible. Moreover, as the size of the letter is increased so it becomes more difficult to read.

There has heretofore been a technique in which subsidiary dots are printed between adjacent dots of a main dot matrix of the character, thus to enhance the clearness of oblique lines and the legibility of the character. With this technique, however, the sizes of the character are subject to a prescribed normalization, and upper and lower or right and left straight lines of the character are not adjusted at all. Moreover to increase the size of the character complicated circuitry is required.

According to one aspect of the present invention there is provided an apparatus for clarifying a character formed by a matrix of display picture elements and non-display picture elements, the apparatus comprising: first means for storing a bit pattern in which the display picture elements and the non-display picture elements forming the character are converted into bits of a first logical value and a second logical value respectively; second means for detecting whether an array of both an arbitrary bit of the second logical value in the aforementioned bit pattern and the surrounding bits thereof coincides with a predetermined rule; third means for converting the arbitrary bit into a bit of the first logical value if the array coincides with the predetermined rule, said second means comprising means for detecting whether or not there is satisfied the condition that in the aforementioned bit pattern two bits of the first logical value are adjoined in an oblique direction and that each of two bits of the second logical value adjoins each of the aforementioned two bits of the first logical value; and said third means comprises means for converting one of the said two bits of the second logical value into one bit of the first logical value if the detected condition is satisfied.

According to a further aspect of the present invention, there is provided an apparatus for clarifying a character formed by a matrix of display picture elements and non-display picture elements, the apparatus comprising: first means for storing a bit pattern in which the display picture elements and the non-display picture elements forming the character are converted into bits of a first logical value and a second logical value respectively; second means for detecting whether an array of both an arbitrary bit of the second logical value in the aforementioned

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bit pattern and the surrounding bits thereof coincides with a predetermined rule; third means for converting the arbitrary bit into a bit of the first logical value if the array coincides with the predetermined rule, said second means comprising means for detecting whether or not there is satisfied the condition that an arbitrary three bits of the first logical value, the first, second and third bits are formed in an oblique direction, and that two other bits of the first logical value are formed in a row or column direction such that one bit thereof adjoins the first bit and the other bit thereof adjoins the said one bit, and that the angle between the aforementioned oblique and row or column directions is within 90° ; and said third means comprises means for converting the one bit of the second logical value which adjoins the aforementioned first and second bits into a bit of the first logical value if the detected condition is satisfied.

According to another aspect of the present invention there is provided an apparatus for increasing and clarifying a character formed by a matrix of display picture elements and non-display picture elements, the apparatus comprises; first means for storing a bit pattern in which the display picture elements and the non-display picture elements forming the character are converted into bits of a first logical value and a second logical value respectively; second means for storing a row magnification of the character; third means for storing a column magnification which equals the row magnification; fourth means for storing in a register a logical value of a bit selected from the aforementioned bit pattern in accordance with a predetermined order; fifth means for detecting whether or not an array of both an arbitrary bit of the second logical value in the aforementioned bit pattern and the surrounding bits thereof coincides with a predetermined rule and, if it coincides, converting the arbitrary bit of the second logical value into a bit of the first logical value; sixth means for storing the converted bit into the aforementioned register; and dot forming means for forming dots in accordance with bits derived from the aforementioned register.

According to a still further aspect of the present invention there is provided a method for clarifying a character formed by a matrix of display picture elements which are contained in display picture element domains and non-display picture elements which are contained in non-display picture element domains, the method comprising the steps: selecting an arbitrary minor matrix of two rows and two columns of two display picture elements and two non display picture elements from a matrix representative of the character; detecting whether or not there is satisfied the condition that said two display picture elements are adjacently formed in an oblique direction and that each of said two non-display picture elements adjoins each of the said two display picture elements; and displaying, if the aforementioned condition is satisfied, a part of the non-display picture element domain containing one of the said two non-display picture elements.

According to yet another aspect of the present invention there is provided a method for clarifying a character formed by a matrix of display picture elements which are contained in display picture element domains and non-display picture elements which are contained in non-display picture element domains, the method comprising the steps: selecting an arbitrary minor matrix of three rows and three columns of five display picture elements and four non-display picture elements, from a matrix representative of the character; detecting whether or not there is satisfied the condition that three of said five display picture elements the first, second and third display picture elements are formed in an oblique direction and that the other remaining two display picture elements are formed in a row or column direction such that one display picture element adjoins the aforementioned first display picture element and the other display picture element adjoins the aforementioned one display picture element, and that the angle between the aforementioned oblique and row or column direction is within 90° ; and displaying, if the aforementioned condition is satisfied, a part of the non-display picture element domain containing one of the aforementioned two non-display picture elements.

According to yet another aspect of the present invention there is provided a method for increasing the size of and clarifying a character formed by a matrix of display picture elements and non-display picture elements, the method comprising the steps: storing a bit pattern in which the display picture elements and the non-display picture elements forming the character are converted into bits of a first logical value and a second logical value respectively; presetting a row magnification and a column magnification which equals the row magnification; reading out by the number of the row or column magnification a logical value of a bit selected from the aforementioned bit pattern in accordance with a predetermined

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order; detecting whether or not the array of both an arbitrary bit of the second logical value in the aforementioned bit pattern and the surrounding bits thereof coincides with a predetermined rule and, if it coincides, converting the arbitrary bit of the second logical value into a bit of the first logical value; reading out the converted bit; and forming dots in accordance with the aforementioned bits read out.

The invention is illustrated, merely by way of example, in the accompanying drawings in which:—

Figure 1, shows on an enlarged scale, the letter "R" produced by a prior art display device;

Figure 2 shows the original dot character pattern of the letter "R" of Figure 1;

Figure 3 shows the dot character pattern of the letter "R" as produced by an embodiment of an apparatus according to the present invention for forming a character out of a pattern of separate display picture elements;

Figures 4 and 5 are dot arrangement diagrams illustrating interpolation rules of an apparatus according to the present invention;

Figures 6A to 6H show logical circuits illustrating an embodiment of an apparatus according to the present invention for forming a character out of a pattern of separate display picture elements;

Figure 7 is a diagram in which the dot character pattern of Figure 2 is represented by a bit pattern;

Figures 8 and 9 are diagrams illustrating the first and second interpolation rules as bit patterns;

Figures 10 and 11 are bit content diagrams each showing a memory state of a shift register of the apparatus of Figure 6;

Figure 12 is a bit content diagram for explaining the logic function of a supplement detecting circuit of the apparatus of Figure 6;

Figure 13 is a diagram explaining the operation of the supplement detecting circuit and a gate controlling an output thereof; and

Figure 14 is an enlarged dot character pattern of the letter "R" formed by an apparatus according to the present invention for forming a character out of a pattern of separate display picture elements.

In the following description the interpolation rules employed by an apparatus according to an embodiment of the present invention for forming a character out of a pattern of separate display picture elements will first be described in detail and then apparatus according to an embodiment of the present invention will subsequently be described.

Figure 2 shows an original dot character pattern of the letter "R" constructed from a dot matrix of 7 rows and 5 columns, and the original dot character pattern is enlarged twice and is illustrated by black circular dots in Figure 3. A first interpolation rule relates to those parts which become unclear due to the enlargement. Dot forming parts and non-dot forming parts (null dot forming parts) which constitute the original dot character pattern of the letter "R" of Figure 2 are divided into domain patterns of 7 rows and 5 columns. Notice is taken of any one domain $\{n,m\}$ (n and m denote row and column numbers respectively), and a minor matrix of 3 rows and 3 columns including the domain $\{n,m\}$ is constructed. The minor matrix is not arbitrary, but is chosen so that, assuming the domain $\{n,m\}$ to be at a position $\{p,q\}$ in the minor matrix, the sum $(p+q)$ is an odd number. Where, in the minor matrix thus chosen, the dot domain has any of the constructions shown in Figures 4A—4H, the interpolation is performed in such a way that a dot is formed at a part d of the non-dot domain $a_{n,m}$ between dot domains b_1 and b_2 . When this interpolation rule is applied to Figure 2, the corresponding domain is $\{5,2\}$. Therefore, in Figure 3 in which the original dot character pattern is magnified twice, a dot d_0 is formed in the enlarged domain $a_{5,2}$ of the domain $\{5,2\}$.

In this manner, the minor matrix of 3 rows and 3 columns is constructed by taking note of any one dot domain, and whether or not the interpolation is necessary is determined.

By this first interpolation rule, the clearness of the character is somewhat enhanced. By applying the second interpolation rule to be explained hereafter, the character can be reproduced well to conform to the intended shape.

In Figure 2 notice is taken of any one non-dot domain $\{p,q\}$, and a minor matrix of 2 rows and 2 columns including the non-dot domain $\{p,q\}$ is constructed. The non-dot domain is denoted by $a_{n,m}$ (n and m indicate the row and column numbers respectively), while the matrices of 2 rows and 2 columns are denoted by:

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$$\left\{ \begin{array}{cc} a_{n-1,m} & a_{n-1,m+1} \\ a_{n,m} & a_{n,m+1} \end{array} \right\} ; \left\{ \begin{array}{cc} a_{n,m} & a_{n,m+1} \\ a_{n+1,m} & a_{n+1,m+1} \end{array} \right\}$$

$$\left\{ \begin{array}{cc} a_{n,m-1} & a_{n,m} \\ a_{n+1,m-1} & a_{n+1,m} \end{array} \right\} ; \left\{ \begin{array}{cc} a_{n-1,m-1} & a_{n-1,m} \\ a_{n,m-1} & a_{n,m} \end{array} \right\}$$

Where, in matrices, each of the domain $a_{n-1,m+1}$, $a_{n+1,m+1}$, $a_{n+1,m-1}$, and $a_{n-1,m-1}$ is a non-dot-domain and each of the domains $a_{n-1,m}$, $a_{n,m+1}$, $a_{n,m+1}$, $a_{n+1,m}$, $a_{n,m-1}$, $a_{n+1,m}$, $a_{n-1,m}$ and $a_{n,m-1}$ is a dot domain, the interpolation is performed at a part of the non-dot domain $a_{n,m}$. In cases other than the above, no interpolation is carried out.

Figures 5A to 5D indicate all the positional relations between non-dot domains C_1 to C_4 and dot domains b_1 , b_2 , and the corresponding interpolation is carried out. When the second interpolation rule is applied to Figure 2, interpolation is performed at domains $\{1,5\}$, $\{2,4\}$, $\{3,4\}$, $\{4,5\}$, $\{5,4\}$, $\{6,3\}$, $\{7,4\}$ and $\{6,5\}$.

Referring now to Figure 6, an embodiment of an apparatus according to the present invention forming a character out of a pattern of separate picture elements using the interpolation rules discussed above, will be described. In Figure 6A a keyboard K is made up of key switches indicative of letters, numerals, symbols etc. Various data entered by these keys are transmitted to predetermined buffer registers by a multiplexer D. A register R_1 stores a magnification number of the character, a register R_2 stores the data of the character, one word of which is read out and written into a register R_3 . Arithmetic circuit AD shown in Figure 6B execute the addition and subtraction between various count contents and stored contents but registers R_4 and R_5 store specific operation outputs of the arithmetic circuit AD. A register R_6 temporarily stores the output of a counter C_4 . A register R_7 (Figure 6D) stores bits corresponding to recorded dots, and it has a memory capacity of 7 bits in this embodiment. A character generator CG (Figure 6C) has the function of converting the data of each character into a bit pattern for conducting a dot recording in accordance with a preset program. A shift register M which stores outputs of the character generator CG is composed of shift registers M_1 — M_6 , and can shift the contents vertically and horizontally. A supplement detecting circuit U detects the necessity for interpolation on the basis of the original character bit pattern, and is illustrated in detail in Figure 6H. The supplement detecting circuit U takes the respective outputs of the bit pattern stored in the register M, and logically detects the first and second interpolations. A register R_8 (Figure 6G) stores a specific operation output of the arithmetic circuit AD. A counter C_1 (Figure 6A) is a septenary counter, whilst a counter C_2 is a preset counter in which "7" is set. A coincidence circuit P_1 shown in Figure 6A detects the coincidence between the counter C_1 and the counter C_2 , and provides an output when both the numerical values coincide. A counter C_3 counts the coincidence output at that time. The counter C_4 in Figure 6B counts the magnification of the character in the vertical direction. A timing counter C_5 in Figure 6C in quinary and generates the timing pulses at terminals d_1 — d_5 in sequence. A counter C_7 in Figure 6E is a preset counter in which "5" is set. When a counter C_6 counts "5", a coincidence circuit P_3 provides an output. A counter C_8 (Figure 6F) is a decimal counter, and supplies an output to a coincidence circuit P_4 . A counter C_9 is a preset counter in which "9" is set. When the output of the counter C_8 coincides with the set value of the counter C_9 , the coincidence circuit P_4 provides an output.

A decoder DC in Figure 6G is so set as to produce, when the magnification of the character is "1", "7", "14", . . . , an output. A coincidence circuit P_5 is a circuit which detects coincidence between the output of the counter C_5 and that of a register R_8 . Monostable multivibrators N_1 — N_{14} are employed for timing outputs and for shaping waveforms. The reference DL designates a delay circuit, references F_1 — F_3 designate S—R flip-flop circuits and reference symbols G_1 — G_{16} designates gates. Reference DR indicate a driving device of a wire dot printer. In this embodiment, there is illustrated the case where dots are formed by seven pins as it is moving in the lateral direction. The supplement detecting circuit U (Figure 6C) will

be explained in more detail. Respective logical values of memory locations (1A—1E)—(9A—9E) of the registers $M_1—M_9$ respectively are supplied to input terminals of the gates indicated by the same references in Figure 6H.

Figure 6H logically represents the first and second interpolations rules, the details of which will be explained hereinafter.

As regards the first interpolation rule, the matrix of 3 rows and 3 columns is assumed to be:

$$\begin{array}{ccc} b_{p,q} & b_{p,q+1} & b_{p,q+2} \\ b_{p+1,q} & b_{p+1,q+1} & b_{p+1,q+2} \\ b_{p+2,q} & b_{p+2,q+1} & b_{p+2,q+2} \end{array}$$

and the bit of which notice is taken is assumed to be $b_{p+1,q}$. Then the bit $b_{p+1,q}$ is converted into "1" when the following relation (1) is satisfied.

$$\overline{b_{p,q}} \cdot \overline{b_{p+1,q+2}} \cdot b_{p,q+2} \cdot b_{p+1,q+1} \cdot b_{p+2,q+2} \cdot (b_{p+2,q+1} \cdot b_{p+2,q} + b_{p,q} \cdot b_{p,q+1}) \times \\ (\overline{b_{p+2,q}} \cdot \overline{b_{p+2,q+1}} + \overline{b_{p,q}} \cdot \overline{b_{p,q+1}}) = 1 \quad (1)$$

Assuming the noticed bit to be $b_{p,q+1}$, it is converted into "1" when the following relation (2) is fulfilled:

$$\overline{b_{p,q+1}} \cdot \overline{b_{p+2,q+1}} \cdot b_{p+1,q+1} \cdot b_{p+2,q+2} \cdot b_{p+2,q} \cdot (\overline{b_{p,q}} \cdot \overline{b_{p+1,q}} + \overline{b_{p,q+2}} \cdot \overline{b_{p+1,q+2}}) \times \\ (b_{p,q} \cdot b_{p+1,q} + b_{p,q+2} \cdot b_{p+1,q+2}) = 1 \quad (2)$$

Assuming the noticed bit to be $b_{p+1,q+2}$, it is converted into "1" when the following relation (3) is fulfilled:

$$\overline{b_{p+1,q+2}} \cdot \overline{b_{p+1,q}} \cdot b_{p,q} \cdot b_{p+1,q+1} \cdot b_{p+2,q} \cdot (\overline{b_{p,q+1}} \cdot \overline{b_{p,q+2}} + \overline{b_{p+2,q+1}} \cdot \overline{b_{p+2,q+2}}) \times (b_{p,q+1} \cdot \\ b_{p,q+2} + b_{p+2,q+1} \cdot b_{p+2,q+2}) = 1 \quad (3)$$

Assuming the noticed bit to be $b_{p+2,q+1}$, it is converted into "1" when the following relation (4) is fulfilled:

$$\overline{b_{p+2,q+1}} \cdot \overline{b_{p,q+1}} \cdot b_{p,q} \cdot b_{p+1,q+1} \cdot b_{p,q+2} \cdot (\overline{b_{p+1,q}} \cdot \overline{b_{p+2,q}} + \overline{b_{p+1,q+2}} \cdot \overline{b_{p+2,q+2}}) \times (b_{p+1,q} \cdot \\ b_{p+2,q} + b_{p+1,q+2} \cdot b_{p+2,q+2}) = 1 \quad (4)$$

The matrix of 2 rows and 2 columns is assumed to be:

$$\begin{array}{cc} a_{p,q} & a_{p,q+1} \\ a_{p+1,q} & a_{p+1,q+1} \end{array}$$

and the bit of which notice is taken is assumed to be $a_{p+1,q}$ or $a_{p,q+1}$. Then, the bit $a_{p+1,q}$ or $a_{p,q+1}$ is converted into "1" when the following relation is established:

$$\overline{a_{p+1,q}} \cdot \overline{a_{p,q+1}} \cdot a_{p,q} \cdot a_{p+1,q+1} = 1$$

Assuming the noticed bit to be $a_{p,q}$ or $a_{p+1,q+1}$, it is converted into "1" when the following relation is established:

$$\overline{a_{p,q}} \cdot \overline{a_{p+1,q+1}} \cdot a_{p+1,q} \cdot a_{p,q+1} = 1$$

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Accordingly, when the noticed bit is "0" and the following equation is met, the noticed bit is converted into "1".

$$a_{p+1,q} \cdot a_{p,q+1} \cdot a_{p,q} \cdot a_{p+1,q+1} + a_{p,q} \cdot a_{p+1,q+1} \cdot a_{p+1,q} \cdot a_{p,q+1} = 1 \quad (5)$$

The foregoing logical relations (1)—(5) in the case where the noticed bit is stored in the location 3C of the register M_3 are configured by the logic circuit in Figure 6H.

The operation of the apparatus will now be explained, the explanation being for the case where the original dot character of the letter "R" in Figure 2 is magnified twice as shown in Figure 3 and where it is printed after performing the interpolation.

In Figure 6A, the magnification "2" of the character and the data of the character are received as inputs from the keyboard K, and they are written through the multiplexer D into the register R_1 for magnification and the register R_2 for the data, respectively. Upon a print order PS_0 from the keyboard K, the character "R" is read out from the register R_2 and is transferred to the register R_3 having a capacity of one word. An output D_0 from the register R_3 is fed into the character generator CG (Figure 6C) and is converted into a bit pattern shown in Figure 7 in which "1" corresponds to a dot and "0" corresponds to a non-dot. Simultaneously therewith, the output PS_0 triggers the monostable multivibrator N_4 through the gate G_{16} in Figure 6C. An output PS_1 from the monostable multivibrator N_4 is fed through the gates G_{17} and G_{19} to 2 inputs of the arithmetic circuit AD, to supply logical values (1,1). The other two inputs of the arithmetic circuit AD, i.e. the outputs from the gates G_{20} and G_{21} are in the state (0,0). As a result, the inputs of the arithmetic circuit AD are supplied with (0,0 1,1) i.e. "3". Further the output PS_1 opens the gates G_{30} — G_{33} in Figure 6B and feeds (0 0 0 0) of outputs a_1 — a_4 of the cleared counter C_6 in Figure 6E to the arithmetic circuit AD. Consequently, "3" appears at outputs b_1 — b_4 of the arithmetic circuit AD. On the other hand, the output PS_1 writes "3" into the register R_3 in Figure 6B by virtue of an output PS_2 having passed through the gates G_{33} . An output from the register R_3 designates the third column of the character generator CG in Figure 6C. Accordingly, the data relating to the third column of the bit pattern in Figure 7 is provided as an output. The reason why the third column of the bit pattern of the letter "R" is read first is for the reasons set out below. In both the first and second interpolation rules previously described, when any one non-dot domain is noted and the presence or absence of the surrounding dot domains is in the prescribed relation, the interpolation is carried out for the non-dot domain so noticed. In the present embodiment, the presence and absence of the dot corresponds to the logical values "1" and "0", respectively. The noticed bit is shifted to a predetermined location in the register. Where the bit or bits in the location are "1" or "0", it is determined by the supplement detecting circuit U whether or not the surrounding bit construction falls under the first or second interpolation rules. Figures 8 and 9 show bit patterns of the logical values "1" and "0" into which the patterns of the interpolation cases previously indicated by dots are converted. A bit b_0 represents the bit of which notice is taken. Data bits at every column of the bit pattern read out from the character generator CG are stored in the registers M_3 — M_6 (Figure 6C). In the present embodiment, the noticed bit is shifted to the location 3C of the register M_3 , and the correlations of the bits with the surrounding bits are investigated.

Returning to the explanation of the operation of the present embodiment, the third column of the bit pattern in Figure 7, as stored in the character generator CG, is designated by outputs e_1 — e_4 of the register R_3 in Figure 6B. Data bits (1 0 0 1 1 0 0) of the third column in the figure are supplied through the gates G_{74} — G_{80} to the registers M_3 — M_6 . On the other hand, the counter C_5 is incremented by "1" by the output PS_2 and provide an output at its terminal d_1 . This output becomes a lateral shift signal for the registers M_1 — M_6 via the gates G_{85} and G_{84} . Therefore, the data bits of the third column are transferred to the location 3A—9A of the registers M_3 — M_6 , respectively. The reason why the registers M_1 and M_2 are provided here is that, in the first interpolation rule, at most 2 bits are required. Consequently, the monostable multivibrator N_5 is triggered by the output of the terminal d_1 . An output PS_3 from the monostable multivibrator is supplied to the inputs of the arithmetic circuit AD through the gates G_{17} — G_{21} in Figure 6A. On

the other hand, the output PS_3 opens the gates G_{38} — G_{41} in Figure 6B and supplies "3" or (0 0 1 1) from the outputs e_1 — e_4 to the inputs of the arithmetic circuit AD. Consequently (0 0 1 0) or "2" appears at the output of the arithmetic circuit AD, and it is written into the register R_6 by the output PS_2 obtained by passing the output PS_3 through the gate G_{83} . Data bits of the second column of the bit pattern of "R" in Figure 7 are designated by the outputs e_1 — e_4 of the register R_6 , and are supplied to the registers M_3 — M_6 . The counter C_6 is incremented by "1" by the output PS_2 and becomes "2" in value. The contents of the registers M_3 — M_6 are shifted by the output at the terminal d_2 thereof, so that the data bits of the third column are transferred to the locations 3B—9B of the registers M_3 — M_6 , whilst the data bits of the second column are transferred to the locations 3A—9A. Likewise, the data bits of the first column are transferred to the locations 3A—9A of the registers M_3 — M_6 . The subsequent values of the outputs E_1 — E_4 close the gates G_{74} — G_{80} to the gates G_{81} and G_{82} and supply "0" to inputs of the registers M_3 — M_6 . Therefore, the stored contents in the registers M_3 — M_6 become as in Figure 10 as a result of a total five shifts. When notice is taken of the stored contents of the location 3C of the register M_3 , i.e. $\{M_3, C\}$ in Figure 10, the bit is "1" and hence it does not become the object of interpolation. The output "1" of the location 3C of the register M_3 closes the gate G_{22} in Figure 6A and simultaneously opens the gate G_{23} . At this time, an output PS_4 of the monostable multivibrator M_6 , triggered by the shift pulse from the last terminal d_5 of the counter C_6 having shifted the registers M_1 — M_6 five times is fed through the gate G_{24} to another input of the gate G_{23} . An output from the gate G_{23} triggers the monostable multivibrator N_1 , an output PS_7 of which is supplied to the gate G_{96} in Figure 6D. Since the gate G_{96} is opened by the output of the location 3C of the register M_3 , the output of the gate G_{23} passes therethrough and is supplied to the register R_7 and is written into a location X_1 by the output PS_8 . The output PS_8 also increments the counter C_4 by "1" through the gate G_{45} (Figure 6B). Outputs h_1 — h_4 of the counter C_4 having counted "1" are supplied to the gates G_{53} — G_{56} . Since the gates G_{53} — G_{56} are opened by an output PS_5 of the monostable multivibrator N_2 (Figure 6A) which is triggered by the output PS_8 , the outputs are supplied through the gates G_{61} — G_{64} to inputs q of the coincidence circuit P_2 . Since the gates G_5 — G_8 are opened by the output PS_6 , the magnification "2" stored in the register R_1 is supplied through the gates G_{57} — G_{60} to inputs p of the coincidence circuit P_2 . The magnification "2" is not coincident with the count "1" in the counter C_4 , so that the coincidence output $p=q$ of the coincidence circuit P_2 does not change. The output PS_5 is supplied through the OR gate G_{46} to the counter C_1 (Figure 6A) and "1" is counted.

The output PS_5 of the monostable multivibrator N_2 in Figure 6A is supplied through the gate G_{24} to the gate G_{23} . Since the contents "1" of the location 3C of the register M_3 remains unchanged, the gate G_{23} is opened, and the output PS_5 passes through the gate G_{23} to trigger the monostable multivibrator N_1 and to generate the output PS_7 again. This output PS_7 opens the gate G_{96} (Figure 6D) and writes the output "1" of the location 3C of the register M_3 into the location X_1 of the register R_7 through the gate G_{97} . In consequence, "1" and "1" are respectively stored in the locations X_1 and X_2 of the register R_7 . On the other hand the output PS_8 increments the contents of the counter C_1 by "1" through the gate G_{45} to render the count contents "2" by the addition with the previous contents "1". The second output PS_5 is supplied to the counter C_4 to render the count contents "2". The output h_1 — h_4 are supplied to inputs q of the coincidence circuit P_2 through the gates G_{53} — G_{56} kept open by the output PS_5 of the monostable multivibrator N_2 and to the inputs p of the coincidence circuit P_2 through the gates G_5 — G_8 kept open by the output PS_6 of the magnification number "2" of the register R_1 and further through the gates G_{57} — G_{60} . Since both the objects of the comparison are "2", an output "1" is produced at the output $p=q$ of the coincidence circuit P_2 . An output w consequently provided from the gate G_{101} (Figure 6F) resets the counter C_4 through the gate G_{47} . On the one hand, the output w triggers the monostable multivibrator N_{10} and generates an output PS_7 . The output PS_7 increments the counter C_8 by "1" through the gate G_{108} by an output PS_8 . Further, the output PS_8 is applied as a vertical shift pulse to the registers M_1 — M_6 so that the contents of the registers M_1 — M_6 of lower digits are transferred to the registers of higher digits and that the contents of the registers M_1 — M_6 become as in Figure 11. Accordingly, the bits {2,1} in the bit-pattern of Figure 7 is stored in the location 3C of the register M_3 , and it becomes the bit of which notice is taken. Then the output PS_7 triggers the monostable multivibrator N_{11} (Figure 6F)

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and produces an output PS_9 . The output PS_9 is applied through the gate G_{24} to the gate G_{23} (Figure 6A).

Thereafter, in the same manner, "1" and "1" are stored in the register R_7 . When 7 bits, i.e. bits corresponding to dots of $\{1,2\}$ (z denotes an integer from 1 to 7) in Figure 7 are stored in the register R_7 and an output "7" is produced by the counter C_1 . Since the output from the counter C_1 coincides with "7" stored in the preset counter C_2 , a coincidence output PS_{10} is provided from the coincidence circuit P_1 (Figure 6A) and the count in the counter C_3 is increased by "1". Simultaneously, the wire driving device DR (Figure 6D) is actuated by the coincidence output PS_{10} . The respective wires of the wire driving device DR are driven in correspondence with the stored contents of the register R_7 . A wire head of the wire driving device DR continues to move. Since all the stored contents are "1" all the wires PN are driven to form 7 dots of the first column in Figure 3. After the output PS_{10} has been supplied to the wire driving device DR , an output PS_{11} is generated from the wire driving device DR . Thus, the gates $G_{65}-G_{68}$ (Figure 6B) are opened, so that "1" forming outputs f_1-f_4 of the counter C_3 is supplied through the gates $G_{61}-G_{64}$ to the inputs q of the coincidence circuit P_2 . The magnification "2" passing through the gates G_5-G_8 , opened by the output PS_{11} , is supplied through the gates $G_{69}-G_{70}$ to the inputs p of the coincidence circuit P_2 . Since the two values entered into the coincidence circuit P_2 are different, the output state $p=q$ of the coincidence circuit does not change. Accordingly, an output is provided from the gate G_{108} (Figure 6F) and this sets the flip-flop circuit F_1 . An output of the flip-flop circuit F_1 opens and gate G_{108} so that an output of the clock pulse CL is supplied through the gate G_{104} as well as the gate G_{103} to the counter C_8 . Since the counter C_8 has already counted three shift pulses, i.e. the output PS_8 , its contents are "3". When 6 clock pulses are further supplied, the count in the counter C_8 becomes "9", which coincides with the numerical value "9" in the counter C_9 preset by the coincidence circuit P_4 . The counter C_8 is reset through the gate G_{107} , by a resulting coincidence output F_1 from the coincidence circuit P_4 . Simultaneously, the flip-flop circuit F_1 is reset to close the gate G_{108} so that the supply of clock pulses to the counter C_8 is stopped. Since the fixed pulses having passed through the gate G_{103} are supplied as the vertical shift pulses of the registers M_1-M_9 , the contents of the respective registers are successively shifted from the lower digits to the higher digits six times. This is carried out in order that the contents of the registers M_1-M_9 is as shown in Figure 10 and is as initially stored in the register M_3 . That is, by shifting the contents nine times from the first stored state, the first stored contents are established again. Then, dots of $\{y,2\}$ (y denotes an integer from 1 to 7) in Figure 3 are formed in the same way as the foregoing. At the termination of the formation of the dots, the count value of the counter C_3 is "2" and the counter output is compared with the magnification "2" by the coincidence circuit P_2 . Since the two numerical values are coincident, the output $p=q$ of the coincidence P_2 changes, and the gate G_{73} is open to reset the counter C_3 . On output PS_{12} from the gate G_{73} increases the count in the counter C_6 by "1". The count in the counter C_6 serves to detect the completion of the bit pattern.

The output PS_{12} triggers the monostable multivibrator N_{12} and supplies its output to the gate G_{99} . In this stage, no output is provided from the coincidence circuit P_3 , so that the gate G_{99} is open. An output PS_{21} is accordingly provided from the gate G_{99} . The output PS_{21} increments the count in the counter C_5 by "1" through the monostable multivibrator N_4 and the gate G_{83} . The output of the arithmetic circuit AD is transferred to the register R_2 by the output PS_2 of the gate G_{83} . The column designation for the character generator CG is formed by the output of the register. The second column in Figure 7 is read out from the character generator CG so as to be stored in the locations $3C-9C$ of the registers M_3-M_9 respectively.

Thereafter, dots and non-dots are formed in the same way as described previously.

As the processing proceeds in the above manner and the count value of the counter C_6 becomes "3", the enlargement dots up to the third column of the dot pattern in Figure 2 or the dots up to the sixth column in Figure 3 are generated. In the fourth column in Figure 7, a part requiring interpolation exists. Description will now be made of the dot formation in this column. Dots at $\{1,7\}$ and $\{2,7\}$ in Figure 3 are formed in the same way as previously stated. Subsequently, the bit "0" of $\{2,4\}$ in Figure 7 is transferred to the location $3C$ of the register M_3 . Then, the output $3C$ of the register M_3 is "0", so that the gate G_{23} shown in Figure 6A is closed whilst the gate G_{24} is opened. In this condition the count C_4 exhibits a count

of "0", the counter C_1 a count of "2", the counter C_8 a count of "1" and the counter C_3 a count of "0". When the gate G_{22} is opened, the output PS_9 of the monostable multivibrator N_{11} opens the gate G_1 — G_4 via the gates G_{24} , G_{22} and by an output S_0 from the gate G_{22} .

In consequence, the magnification "2" stored in the register R_1 , i.e. the output (0 0 1 0) is supplied through the gates G_1 — G_4 and G_{13} — G_{16} to the inputs of the arithmetic circuit AD. The output S_0 opens the gates G_{34} — G_{37} to convert the count (0 0 0 0) in the counter C_3 into its 1's complement (1 1 1 1), which is supplied to the inputs of the arithmetic circuit AD. An output of (0 0 0 1) is produced by the arithmetic circuit AD and this output is transferred to the register R_4 by the output S_0 . The output S_0 triggers the monostable multivibrator N_3 and produces an output Pw_{13} . Thus the gates G_{48} — G_{51} are opened so that the contents (0 0 0 1) of the register R_4 are supplied through the gates G_{48} — G_{51} and the gates G_{57} — G_{60} to the inputs p of the coincidence circuit P_2 . The outputs PS_{13} also opens the gates G_{53} — G_{56} through the gate G_{52} , so that the count (0 0 0 0) of the counter C_4 is supplied through the gates G_{51} — G_{54} to the inputs q of the coincidence circuit P_2 . Since the values of the compared inputs differ, an output $p < q$ of the coincidence circuit P_2 changes and the gates G_{87} and G_{88} are opened.

The bit contents stored in the registers M_1 — M_3 cause the outputs u_1 — u_4 of the supplementary detecting circuit to be "0" which signifies that no interpolation is necessary. Accordingly, the output of the gate G_{91} , formerly opened becomes "0". Further, an output $p < q$ from the coincidence C_2 is changed by the output PS_{13} of the monostable multivibrator N_7 which is triggered by the output PS_{13} . The details of this operation will be made apparent in the description of interpolation hereafter. The gates G_{88} and G_{89} are opened by the output $p < q$ and the gates G_{92} and G_{93} are opened by the output PS_{16} . Since the output u_3 is "0", the output of the gate G_{92} becomes "0". The output PS_{16} triggers the monostable multivibrator N_8 which then produces an output PS_{14} . Since the contents "0" in the location 3C of the register M_3 are supplied through the gates G_{96} and G_{97} to the input of the register R_7 , they are written into the register by the output PS_{14} . The register R_7 has stored therein bits "1" and "1" corresponding to the dots {1,7} and {2,7} shown in Figure 3, so that 0, 1, 1 are stored in the locations (X_1 , X_2 , X_3). On the other hand, the output PS_{14} triggers the monostable multivibrator N_9 to generate an output PS_{15} . The output PS_{15} adds "1" to the count in the counter C_4 and the counter in the counter C_1 through the gate G_{46} illustrated in Figure 6B. Consequently, the count in the counter C_4 becomes "1" and the count in the counter C_1 becomes "3".

Thereafter the output PS_{15} is supplied to the gate G_{161} . The same operation as previously explained is again conducted through the monostable multivibrator N_{23} , the gate G_{102} and the gate G_{24} .

Thereafter, the bits "1" and "0" corresponding to the dots and non-dots of {q,7} (q denotes an integer from 4 to 7) in Figure 3 are written into the register R_7 in the same manner. When the contents stored in the register R_7 become (1, 0, 0, 0, 0, 1, 1), the count in the counter C_1 becomes "7" and the output PS_{10} is produced by the coincidence circuit C_2 . The wire driving device DR is driven to form the dots {1,7}, {2,7} and {7,7} in Figure 3.

Subsequently, the dot formation for the eighth column is initiated. Since the dot requiring no interpolation has already been explained {3,8} in Figure 3 requiring interpolation will be described. The bits corresponding to the dots {1,8} and {2,8} have already been stored in the register R_7 and the bit in the location 3C of the register R_3 is made "0". The contents of the various counters in this condition are as stated below. The count in the counter C_4 is "0", the count in the counter C_1 is "2", the count in the counter C_8 is "1", the count in the counter C_3 is "1" and the count in the counter C_6 is "3". The stored value "0" at the location 3C of the register M_3 opens the gate G_{22} . The gates G_1 — G_4 are opened by the output S_0 so that the stored magnification "2" in the register R_1 is supplied to the arithmetic circuit AD. The gates G_{34} — G_{37} are opened by the output S_0 so that the 1's complement (1, 1, 1, 0) of the count of "1" or (0, 0, 0, 1) in the counter C_3 is supplied to the input of the arithmetic circuit AD. At the output of the arithmetic circuit AD (0, 0, 0, 1) appear, and this is supplied to inputs p of the coincidence circuit P_2 through gates G_{48} — G_{51} opened by the output PS_{13} of the monostable multivibrator N_3 triggered by the output S_0 and further through the gates G_{57} — G_{60} . The output PS_6 opens the gates G_{53} — G_{56} through the gate G_{52} to supply the counter "0" in the counter C_4 to the inputs q of the coincidence circuit P_2 . The two inputs to the coincidence circuits P_2 are "1" and "0", the output

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$p > q$ from the coincidence circuit P_2 changes and the gates G_{87} and G_{88} are opened. Here, the outputs (u_1, u_2, u_3, u_4) of the supplement detecting circuit U indicate (1, 0, 0, 1), respectively. This is obvious by introducing the respective logical values "1" and "0" of the registers M_1-M_6 into the detector circuit shown in Figure 6H. Then, outputs "0" are provided from the gates G_{87} and G_{88} . Further, the gates G_{90} and G_{91} are opened by the output PS_{13} . Since the output of the gate G_{87} is "0", that of gate G_{91} becomes "0". Subsequently, the output PS_{16} of the monostable multivibrator N_7 triggered by the output PS_{13} opens the gates $G_{69}-G_{72}$ to supply the count of "1" in the counter C_3 to the inputs p of the coincidence circuit P_2 . Simultaneously therewith, the output PS_{16} opens the gates $G_{83}-G_{86}$ to supply the count of "0" in the counter P_4 to the inputs q of the coincidence circuit P_2 . The inputs compared by the coincidence circuit P_2 are "1" and "0", and an output is provided at $p < q$ so that the gates G_{86} and G_{89} are open and "1" of the output u_4 of the supplement detecting circuit U appears at the output of the gate G_{89} . Since the gate G_{92} and G_{93} are kept open by the output PS_{16} , the gate G_{93} provides an output "1", and the flip-flop circuit F_3 is set.

The flip-flop circuit F_3 holds the set state, to provide a logical "1" at its output Q and to open the gate G_{95} . The output PS_{14} of the monostable multivibrator N_8 triggered by the output PS_{16} is supplied to the input of the register R_7 through the gate G_{95} and further through the gate G_{97} . The output PS_{14} shifts the contents of the register R_7 by 1 bit, to write "1" in location X_1 . Although the bit of the location 3C of the register M_3 is "0", "1" written into the register R_7 and a correction for interpolation is carried out. That is, the bit forming an interpolating dot in the non-dot position, {3,8} is stored. Since the bits of positions {4,8} and {5,8} require no correction, "0" and "0" are written into the register R_7 . At position {6,8}, the interpolating bit "1" is again written into the register R_7 in the same manner as described above.

Thereafter, when the bit "1" corresponding to the dot {7,8} is written into the register R_7 , the output PS_{10} is provided from the coincidence circuit P_1 . The wire driving device DR shown in Figure 6D is driven to form the dots {1,8}, {2,8} and {7,8} and also to form the interpolating dots {3,8} and {6,8}. When the formation of the dots and the interpolating dots proceeds in this way and the dots of the tenth column in Figure 3 are formed, the counter C_6 counts "5" and since the count in the counter C_6 then coincides with the count in the preset counter C_7 , an output is provided from the coincidence circuit P_3 and this output is supplied to the gate G_{100} . Since the gate G_{100} is maintained open by the output of the monostable multivibrator N_{12} triggered by the output PS_{12} , the output of the coincidence circuit P_3 passes through the gate G_{100} to reset the counter C_6 and to become a signal for feeding the wire head to a predetermined position in order to provide a space of a letter or the like to be printed next. This is customary in conventional wire head printers and other head drive type printers, and the detailed description is omitted.

The interpolating function described above and the outputs of the supplement detecting circuit U and the opening and closing of the gates $G_{86}-G_{89}$ will now be explained.

Figure 12 illustrates interpolations at the time when, in the bit pattern of a letter, numeral, symbol or the like, 1 bit of the original pattern is magnified in times vertically and horizontally. There are four types of interpolation as shown at A, B, C and D in Figure 12. A represents the interpolation of a left upper part, B that of a left lower part, C that of a right upper part and D that of a right lower part.

Figure 13 shows a circuit which determines the interpolation on the basis of the four kinds of interpolation and the output of the interpolation detecting circuit. M denotes the value of the magnification m , F a position in the horizontal direction in Figure 12, and C a position in the vertical direction. The value at the time when the counter C_3 is of the scale of m corresponds to F , while the value at the time when the counter C_4 is of the scale of c corresponds to C . SG designates a subtractor. P_2 and P_7 designate coincidence circuits, which correspond to the coincidence circuit P_2 described previously. Input terminals u_1-u_4 of the gates $G_{a1}-G_{a4}$ are supplied with the outputs of the supplement detecting circuit shown in Figure 6H. In this manner, the interpolating bit is prepared on the basis of the selection of the interpolating domain and the necessity for interpolation.

When one character is formed in this way, a predetermined space is taken and 5×7 dots of the next letter, numeral or symbol are formed again. When the recording of one row is thus terminated, a carriage return is then performed.

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Hereunder, description will be made of a case where dots of the latter half of the bit pattern in Figure 3 are formed. When the dots of the one row are completed, a carriage return signal ES is generated by the wire driving device DR by conventional means, and the wire head returns to a recording initiating position. Such operation is an expedient which is customary in conventional wire printers and other apparatus of this type, and the details are omitted.

In the period between the generation of the carriage return signal and the return of the wire head to the initial position, the following preparations are made. When the printing of one row is terminated, the next operation is prepared for by the output PS_{17} provided from the gate G_{109} after forming the dots of the last column of the last character. At the termination of the printing of one row, the count in the counter C_4 is "1", and the counter C_8 stores the number of vertical shifts of the register M_1-M_9 . It is therefore necessary to transfer the contents to the register before the respective counters are reset. This operation of transferring the contents of the counter C_4 will now be explained. An output is provided from the gate G_{111} shown in Figure 6G by means of an output PS_{17} and triggers the monostable multivibrator N_{14} through the gate G_{112} . An output PS_{18} from the monostable multivibrator N_{14} causes the count of "1" in the counter C_4 to be written into the register R_6 .

The gates $G_{117}-G_{120}$ are opened by the output PS_{18} , the memory outputs of the register R_6 are passed through the gates $G_{117}-G_{120}$, and outputs k_1-k_4 from these gates are supplied to the inputs of the arithmetic circuit AD. The contents of the register R_6 are "0" during the period in which the dots of the first 7 rows of the letter or the like are formed, so that (0, 0, 0, 0) are supplied to the inputs of the arithmetic circuit AD. The output PS_{18} opens the gates G_9-G_{12} to supply the count of "3" in the counter C_8 to the inputs of the arithmetic circuit AD. Accordingly, "3" appears at the output of the arithmetic circuit AD and is written into the register R_6 by the fall of the output PS_{18} , so that the count in the counter C_8 is held. The count in the counter C_8 is not directly transferred to the register R_6 , and the reason therefor is as follows. No problem is involved in the case where, as in the present embodiment, recording of one character is completed by scanning the wire head only twice. In the case of performing several scanings, however, it needs to be known that the stored contents of the registers M_1-M_9 ought to be recorded from what row of the bit pattern of the same character as in the preceding scanning: written anew from the character generator CG, at the next scanning independent on the number of vertical shifts of the memory contents of the registered M_1-M_9 as performed till the preceding scanning, and the bit pattern written anew need be shifted in the vertical direction by the number of times of the vertical shifts.

When the wire head arrives at the initial position, the carriage return signal ES from the wire driving device DR triggers the monostable multivibrator N_4 through the gate G_{162} . The output PS_1 of the monostable multivibrator is supplied through the gate G_{83} to the counter C_6 . Accordingly, horizontal shift pulses for the register M are successively generated at the output of the counter C_6 , and the bit pattern of Figure 2 is transferred from the character generator CG to the registers M_1-M_9 . The operation at this time is the same as that described initially. Therefore, in order to form the dots from the eighth row to the fourteenth row, the stored contents of the registers M_1-M_9 are shifted in the vertical direction three times. Then, the contents of the location of the register M_6 becomes the bit "1" corresponding to the dot {4,1} in Figure 2. After a part of the dot pattern corresponding to the first column, second column and third column of the dot pattern in Figure 2 is written into the registers M_5-M_9 by the last output of the counter C_6 , the output PS_4 of the monostable multivibrator N_6 triggered by the terminal d_6 of the counter C_6 , sets the flip-flop circuit F_2 shown in Figure 6F. The gate G_{106} is opened by the output of the flip-flop circuit F_2 to pass the output pulses of the clock pulse generator CL therethrough, which are supplied through the gate G_{104} as well as the gate G_{103} to the counter C_3 and which shift the registers M_1-M_9 in the vertical direction. When the counter C_3 counts 3 pulses, the stored contents "3" of the register R_6 are supplied to the coincidence circuit P_6 through the gates $G_{115}-G_{116}$ which are opened by the output Q of the flip-flop circuit F_2 . Consequently, an output PS_{19} is provided from the coincidence circuit P_6 and resets the flip-flop circuit F_2 .

Accordingly, the 3 pulses having passed through the gate G_{103} shift the contents of the registers M_1-M_9 in the vertical direction three times. The output PS_{19} sets the contents of the register R_6 in the counter C_4 .

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Thereafter, the printing is performed in the same way as described above, to form the dots in and below the eighth row in Figure 3 and to obtain an interpolated clear letter "R" as shown in Figure 14.

This embodiment has been described in relation to a wire driving device DR having seven wires and the character magnified twice. In the case where the magnification is a whole number (e.g. 1, 7, 14 or 21) the operation proceeds in such a way that when the wire head shifts to the next scanning after terminating the scanning of enlargement bits corresponding to 1 bit of the original pattern, the printing is executed from the beginning of enlargement bits among bits of the next row in the original pattern. Hereunder, this operation will be explained. As an example, a case of forming a character with the original pattern magnified 14 times is taken. In this case the counters C_4 and C_3 must be altered to the scale of 14, respectively because the magnification becomes "14". Let it now be supposed that an area corresponding to 14 dots has been recorded by the two scans of the wire head and that the enlargement of 1 dot of the original pattern has been terminated. At this time, the count in the counter C_4 is "14", and the count in the counter C_3 is "0". Since the decoder DC shown in Figure 6G is so set as to produce an output when the magnification is 1, 7, 14, 21, . . . , and the gate G_{109} is open. When the output of the coincidence circuit P_2 becomes $p=q$, the gate G_{109} provides an output to open the gate G_{101} . In the present embodiment, when the final data of 1 row is read out, control data DS indicating that it is the final is generated. The control data triggers the monostable multivibrator N_{13} through the gate G_{110} and generates an output PS_{20} . The output PS_{20} resets the counter C_4 through the gate G_{47} , and adds "1" to the counter C_3 through the gate G_{108} , to vertically shift the original pattern by 1 bit. Thereafter, the operation is the same as previously described.

The monostable multivibrators are used in the present embodiment in order to clearly indicate the relation between the respective outputs. However, they are not strictly necessary and can be replaced by timing pulses originating from a reference clock pulse.

Although the wire dot printer has been referred to in the present embodiment, this invention is not restricted thereto but it is applicable to an electronic printer such as a discharge breakdown printer. All that is required is that the apparatus records letters, numerals, symbols etc., by dot matrices. Although the number of dot forming wires has been described as being 7 in the present embodiment it may be any suitable number although some minor modification to the present embodiment will be required.

By employing the first and second interpolating rules, the clearness of the picture does not change even when the enlargement magnification is increased. Since a computer, for example, is not employed the preferred embodiment is of a relatively small size.

WHAT WE CLAIM IS:—

1. An apparatus for clarifying a character formed by a matrix of display picture elements and non-display picture elements, the apparatus comprising: first means for storing a bit pattern in which the display picture elements and the non-display picture elements forming the character are converted into bits of a first logical value and a second logical value respectively; second means for detecting whether an array of both an arbitrary bit of the second logical value in the aforementioned bit pattern and the surrounding bits thereof coincides with a predetermined rule; third means for converting the arbitrary bit into a bit of the first logical value if the array coincides with the predetermined rule, said second means comprising means for detecting whether or not there is satisfied the condition that in the aforementioned bit pattern two bits of the first logical value are adjoined in an oblique direction and that each of two bits of the second logical value adjoins each of the aforementioned two bits of the first logical value; and said third means comprises means for converting one of the said two bits of the second logical value into one bit of the first logical value if the detected condition is satisfied.

2. An apparatus for clarifying a character formed by a matrix of display picture elements and non-display picture elements, the apparatus comprising: first means for storing a bit pattern in which the display picture elements and the non-display picture elements forming the character are converted into bits of a first logical value and a second logical value respectively; second means for detecting whether an array of both an arbitrary bit of the second logical value in the aforementioned bit pattern and the surrounding bits thereof coincides with a predetermined rule;

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Thereafter, the printing is performed in the same way as described above, to form the dots in and below the eighth row in Figure 3 and to obtain an interpolated clear letter "R" as shown in Figure 14.

This embodiment has been described in relation to a wire driving device DR having seven wires and the character magnified twice. In the case where the magnification is a whole number (e.g. 1, 7, 14 or 21) the operation proceeds in such a way that when the wire head shifts to the next scanning after terminating the scanning of enlargement bits corresponding to 1 bit of the original pattern, the printing is executed from the beginning of enlargement bits among bits of the next row in the original pattern. Hereunder, this operation will be explained. As an example, a case of forming a character with the original pattern magnified 14 times is taken. In this case the counters C_4 and C_3 must be altered to the scale of 14, respectively because the magnification becomes "14". Let it now be supposed that an area corresponding to 14 dots has been recorded by the two scans of the wire head and that the enlargement of 1 dot of the original pattern has been terminated. At this time, the count in the counter C_4 is "14", and the count in the counter C_3 is "0". Since the decoder DC shown in Figure 6G is so set as to produce an output when the magnification is 1, 7, 14, 21, . . . , and the gate G_{109} is open. When the output of the coincidence circuit P_2 becomes $p=q$, the gate G_{109} provides an output to open the gate G_{101} . In the present embodiment, when the final data of 1 row is read out, control data DS indicating that it is the final is generated. The control data triggers the monostable multivibrator N_{13} through the gate G_{110} and generates an output PS_{20} . The output PS_{20} resets the counter C_4 through the gate G_{47} , and adds "1" to the counter C_3 through the gate G_{103} , to vertically shift the original pattern by 1 bit. Thereafter, the operation is the same as previously described.

The monostable multivibrators are used in the present embodiment in order to clearly indicate the relation between the respective outputs. However, they are not strictly necessary and can be replaced by timing pulses originating from a reference clock pulse.

Although the wire dot printer has been referred to in the present embodiment, this invention is not restricted thereto but it is applicable to an electronic printer such as a discharge breakdown printer. All that is required is that the apparatus records letters, numerals, symbols etc., by dot matrices. Although the number of dot forming wires has been described as being 7 in the present embodiment it may be any suitable number although some minor modification to the present embodiment will be required.

By employing the first and second interpolating rules, the clearness of the picture does not change even when the enlargement magnification is increased. Since a computer, for example, is not employed the preferred embodiment is of a relatively small size.

WHAT WE CLAIM IS:—

1. An apparatus for clarifying a character formed by a matrix of display picture elements and non-display picture elements, the apparatus comprising: first means for storing a bit pattern in which the display picture elements and the non-display picture elements forming the character are converted into bits of a first logical value and a second logical value respectively; second means for detecting whether an array of both an arbitrary bit of the second logical value in the aforementioned bit pattern and the surrounding bits thereof coincides with a predetermined rule; third means for converting the arbitrary bit into a bit of the first logical value if the array coincides with the predetermined rule, said second means comprising means for detecting whether or not there is satisfied the condition that in the aforementioned bit pattern two bits of the first logical value are adjoined in an oblique direction and that each of two bits of the second logical value adjoins each of the aforementioned two bits of the first logical value; and said third means comprises means for converting one of the said two bits of the second logical value into one bit of the first logical value if the detected condition is satisfied.

2. An apparatus for clarifying a character formed by a matrix of display picture elements and non-display picture elements, the apparatus comprising: first means for storing a bit pattern in which the display picture elements and the non-display picture elements forming the character are converted into bits of a first logical value and a second logical value respectively; second means for detecting whether an array of both an arbitrary bit of the second logical value in the aforementioned bit pattern and the surrounding bits thereof coincides with a predetermined rule;



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third means for converting the arbitrary bit into a bit of the first logical value if the array coincides with the predetermined rule, said second means comprising means for detecting whether or not there is satisfied the condition that an arbitrary three bits of the first logical value, the first, second and third bits are formed in an oblique direction, and that two other bits of the first logical value are formed in a row or column direction such that one bit thereof adjoins the first bit and the other bit thereof adjoins the said one bit, and that the angle between the aforementioned oblique and row or column directions is within 90° ; and said third means comprises means for converting the one bit of the second logical value which adjoins the aforementioned first and second bits into a bit of the first logical value if the detected condition is satisfied.

3. An apparatus as set forth in claim 2, further including fourth means for detecting whether or not there is satisfied the condition that in the aforementioned bit pattern two bits of the first logical value are adjoined in an oblique direction and that each of two bits of the second logical value adjoin each of the aforementioned two bits of the first logical value; and fifth means for converting the one of the aforementioned two bits of the second logical value into one bit of the first logical value if the detected condition is satisfied.

4. An apparatus for increasing the size of and clarifying a character formed by a matrix of display picture elements and non-display picture elements, the apparatus comprises; first means for storing a bit pattern in which the display picture elements and the non-display picture elements forming the character are converted into bits of a first logical value and a second logical value respectively; second means for storing a row magnification of the character; third means for storing a column magnification which equals the row magnification; fourth means for storing in a register a logical value of a bit selected from the aforementioned bit pattern in accordance with a predetermined order; fifth means for detecting whether or not an array of both an arbitrary bit of the second logical value in the aforementioned bit pattern and the surrounding bits thereof coincides with a predetermined rule and, if it coincides, converting the arbitrary bit of the second logical value into a bit of the first logical value; sixth means for storing the converted bit into the aforementioned register; and dot forming means for forming dots in accordance with bits derived from the aforementioned register.

5. An apparatus as set forth in claim 4; wherein said fifth means comprises means for detecting that in an arbitrary matrix of two rows and two columns including the arbitrary bit of the second logical value, an opposite bit to the arbitrary bit in an oblique direction has the second logical value and that the remaining other two bits both have the first logical value, and means for converting the aforementioned arbitrary bit into a bit of the first logical value.

6. An apparatus as set forth in claim 4; wherein said fifth means comprises means for detecting that in an arbitrary matrix of three rows and three columns including the arbitrary bit of the second logical value, three bits of the first logical value the first, second and third bits are adjoined respectively in an oblique direction and that two other bits of the first logical value are adjoined in a row or column direction such that one bit thereof adjoins the said first bit and the other bit thereof adjoins the said one bit, and that the angle between the aforementioned oblique and row or column directions is within 90° , and that the aforementioned arbitrary bit adjoins the said first bit and the said second bit, and that the remaining other three bits have the second logical value; and means for converting the aforementioned arbitrary bit of the second logical value into a bit of the first logical value.

7. An apparatus as set forth in claim 6; wherein said fifth means further comprises means for detecting that in an arbitrary matrix of two rows and two columns including the arbitrary bit of the second logical value, an opposite bit to the arbitrary bit in an oblique direction has the second logical value and that the remaining other two bits both have the first logical value and means for converting the aforementioned arbitrary bit into a bit of the first logical value.

8. A method for clarifying a character formed by a matrix of display picture elements which are contained in display picture element domains and non-display picture elements which are contained in non-display picture element domains, the method comprising the steps: selecting an arbitrary minor matrix of two rows and two columns of two display picture elements and two non display picture elements from a matrix representative of the character; detecting whether or not there is satisfied the condition that said two display picture elements are adjacently formed in an oblique direction and that each of said two non-display picture elements



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adjoins each of the said two display picture elements; and displaying, if the aforementioned condition is satisfied, a part of the non-display picture element domain containing one of the said two non-display picture elements.

9. A method for clarifying a character formed by a matrix of display picture elements which are contained in display picture element domains and non-display picture elements which are contained in non-display picture element domains, the method comprising the steps: selecting an arbitrary minor matrix of three rows and three columns of five display picture elements and four non-display picture elements from a matrix representative of the character; detecting whether or not there is satisfied the condition that three of said five display picture elements the first, second and third display picture elements are formed in an oblique direction and that the other remaining two display picture elements are formed in a row or column direction such that one display picture element adjoins the aforementioned first display picture element and the other display picture element adjoins the aforementioned one display picture element, and that the angle between the aforementioned oblique and row or column directions is within 90° ; and displaying, if the aforementioned condition is satisfied, a part of the non-display picture element domain containing one of the aforementioned two non-display picture elements.

10. A method for increasing the size of and clarifying a character formed by a matrix of display picture elements and non-display picture elements, the method comprising the steps: storing a bit pattern in which the display picture elements and the non-display picture elements forming the character are converted into bits of a first logical value and a second logical value respectively; presetting a row magnification and a column magnification which equals the row magnification; reading out by the number of the row or column magnification a logical value of a bit selected from the aforementioned bit pattern in accordance with a predetermined order; detecting whether or not the array of both an arbitrary bit of the second logical value in the aforementioned bit pattern and the surrounding bits thereof coincides with a predetermined rule and, if it coincides, converting the arbitrary bit of the second logical value into a bit of the first logical value; reading out the converted bit; and forming dots in accordance with the aforementioned bits read out.

11. A method as set forth in claim 10; wherein the step of detecting comprises detecting whether or not there is in an arbitrary minor matrix of two rows and two columns including the arbitrary bit of the second logical value, an opposite bit to the arbitrary bit in an oblique direction having the second logical value and in which the remaining other two bits both have the first logical value; and converting the aforementioned arbitrary bit into a bit of the first logical value.

12. A method as set forth in claim 11; wherein the step of detecting comprises detecting whether or not there is an array which in an arbitrary minor matrix of three rows and three columns including an arbitrary bit of the second logical value, three bits of the first logical value the first, second and third bits adjoined respectively in an oblique direction and in which two other bits of the first logical value are adjoined in a row or column direction with the one bit thereof adjoining the aforementioned first bit and the other bit thereof adjoining the said one bit and in which the angle between the aforementioned oblique and row or column directions falls within 90° , and in which the aforementioned arbitrary bit adjoins the aforementioned first bit and the second bit and the remaining other three bits have the second logical value; and converting the aforementioned arbitrary bit into a bit of the first logical value.

13. An apparatus for clarifying a character formed by a matrix of display picture elements substantially as herein described with reference to and as shown in the accompanying drawings.

14. A method for clarifying a character formed by a matrix of display picture elements substantially as herein described with reference to the accompanying drawings.

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