FIG. 1

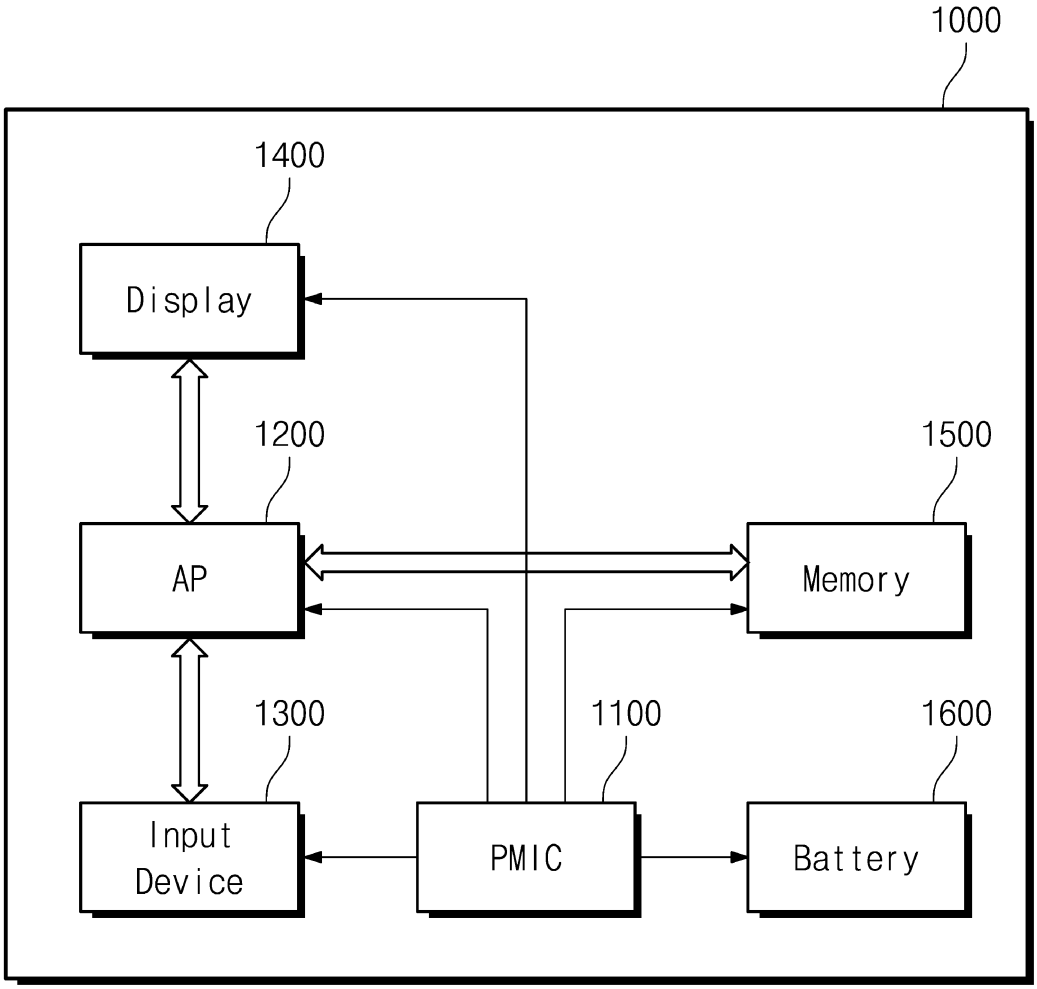

1000
1400
Display
1200
AP
1500
Memory
1300
Input Device
1100
PMIC
1600
Battery

FIG. 2

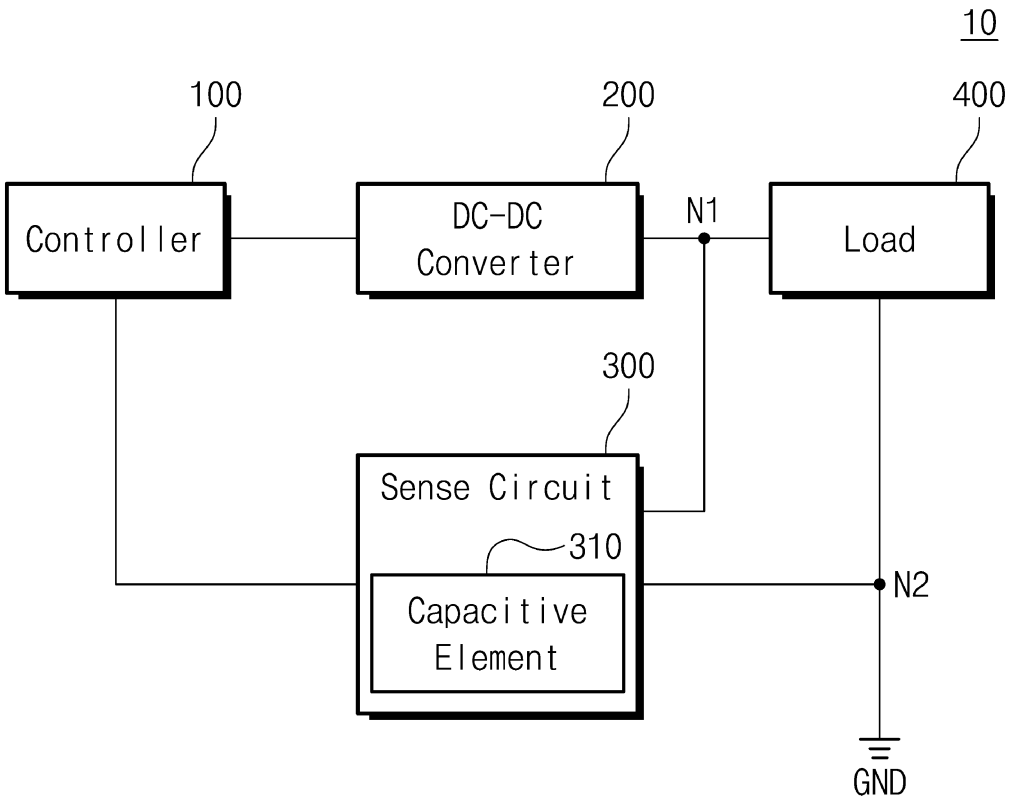

10
100
200
400
Controller
DC-DC
Converter
N1
Load
300
Sense Circuit
310
Capacitive
Element
N2
GND

FIG. 3

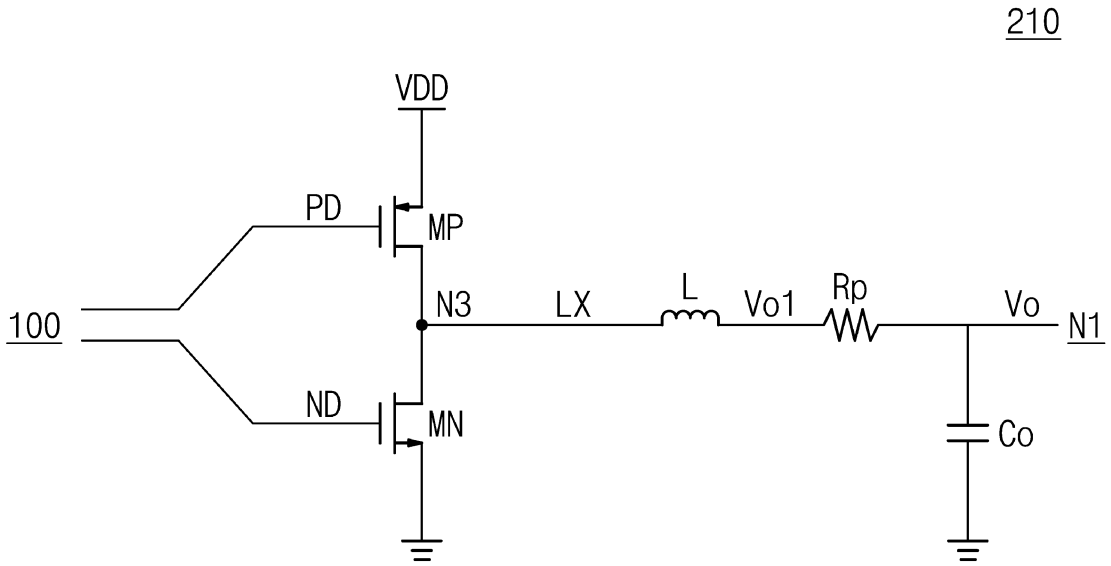

210
VDD
PD
MP
100
N3
LX
L
Vo1
Rp
Vo
N1
ND
MN
Co

FIG. 4

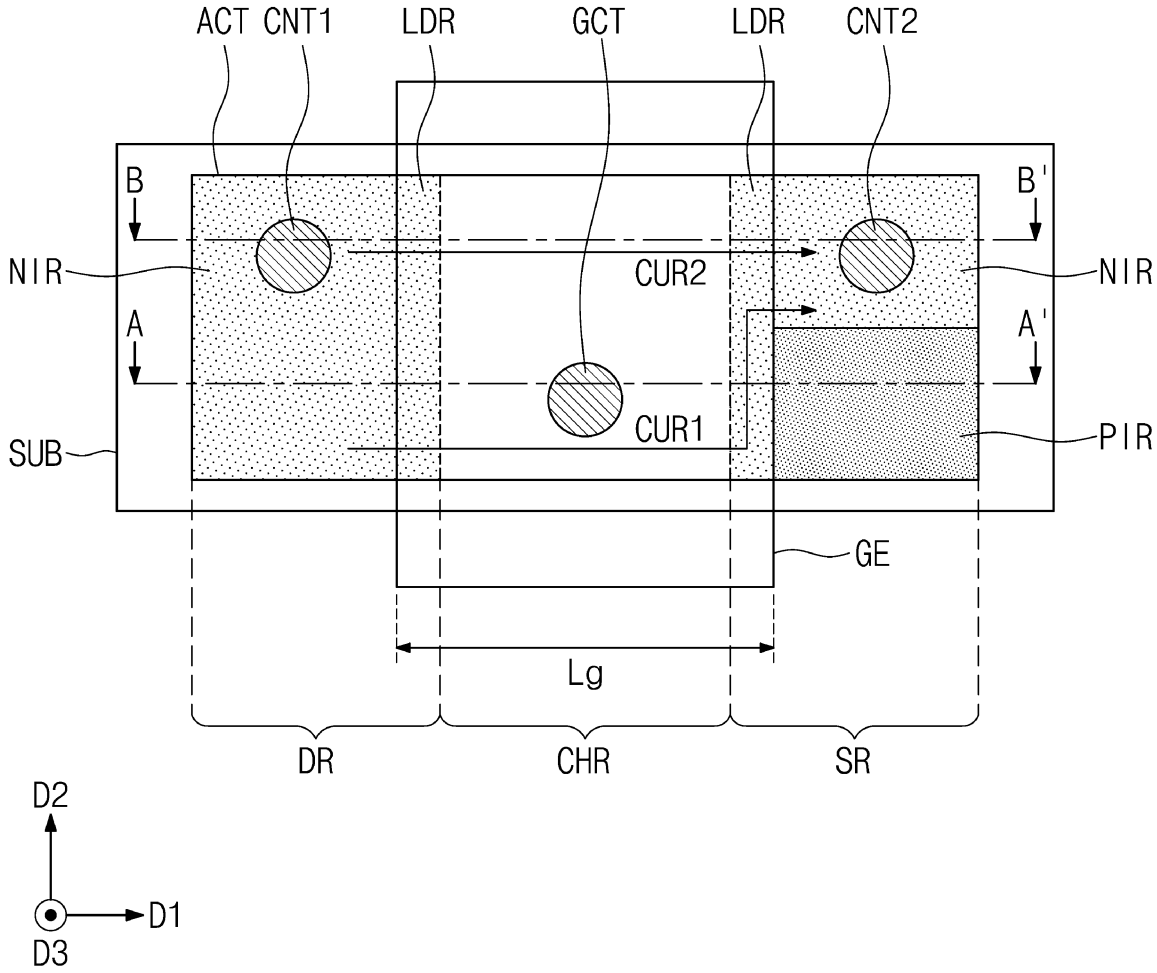

ACT
CNT1
LDR
GCT
LDR
CNT2
B
B'
NIR
CUR2
NIR
A
A'
CUR1
SUB
PIR
GE
Lg
DR
CHR
SR
D2
D1
D3

FIG. 5A

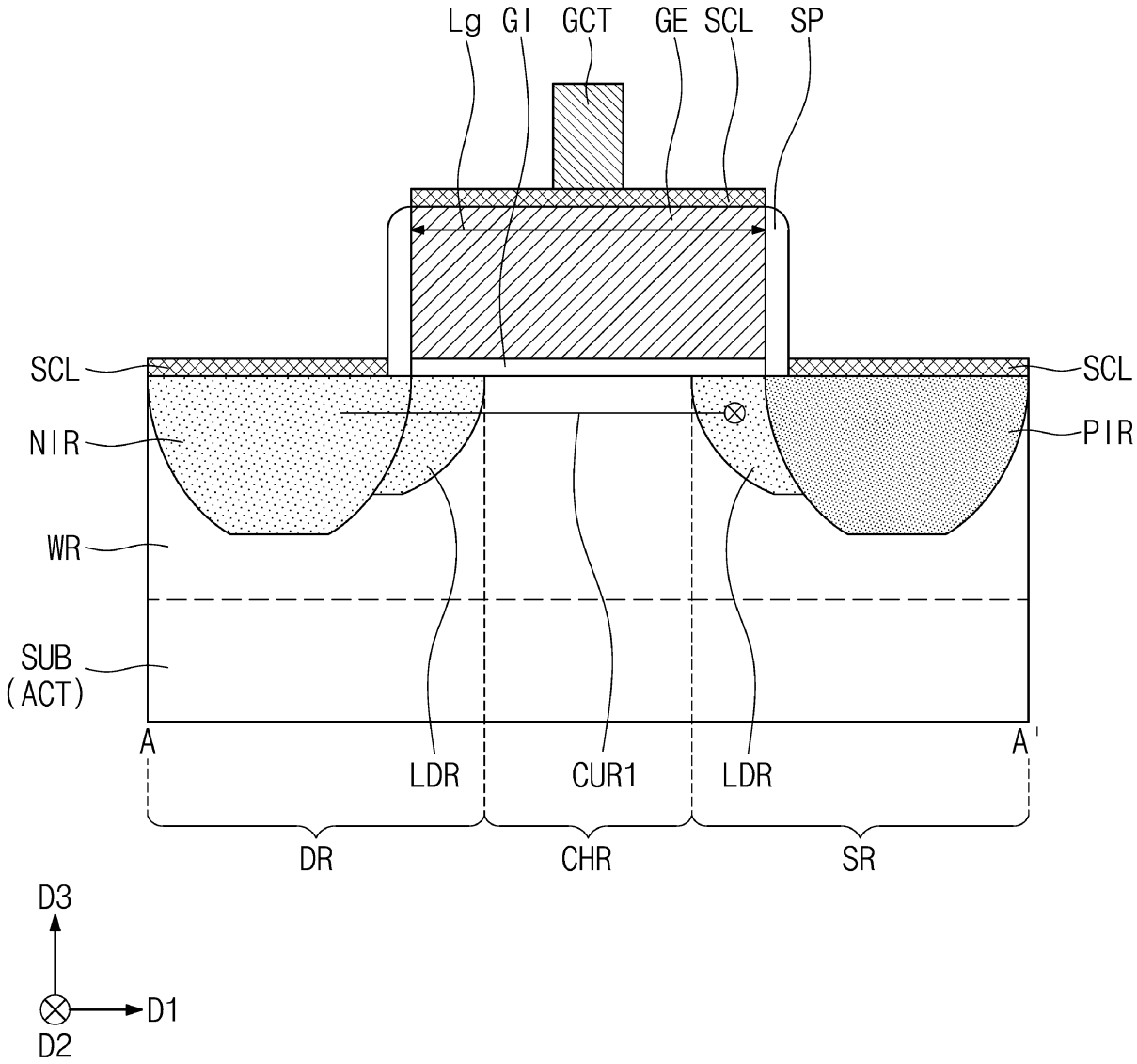

Lg
GI
GCT
GE
SCL
SP
SCL
SCL
NIR
PIR
WR
SUB
(ACT)
A
A'
LDR
CUR1
LDR
DR
CHR
SR
D3
D1
D2

FIG. 5B

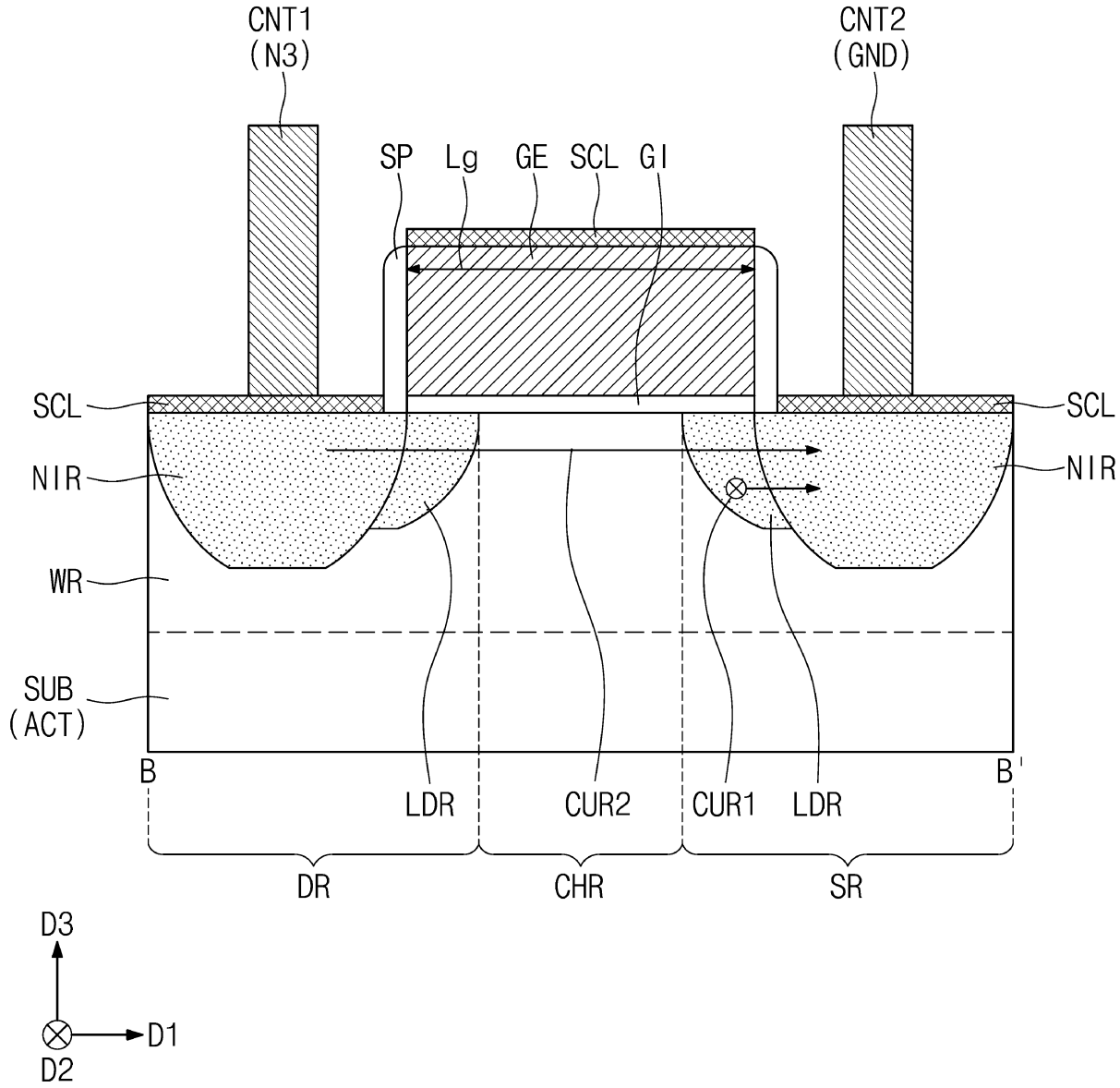

CNT1
(N3)
CNT2
(GND)
SP
Lg
GE
SCL
GI
SCL
SCL
NIR
NIR
WR
SUB
(ACT)
B
B'
LDR
CUR2
CUR1
LDR
DR
CHR
SR
D3
D1
D2

FIG. 6

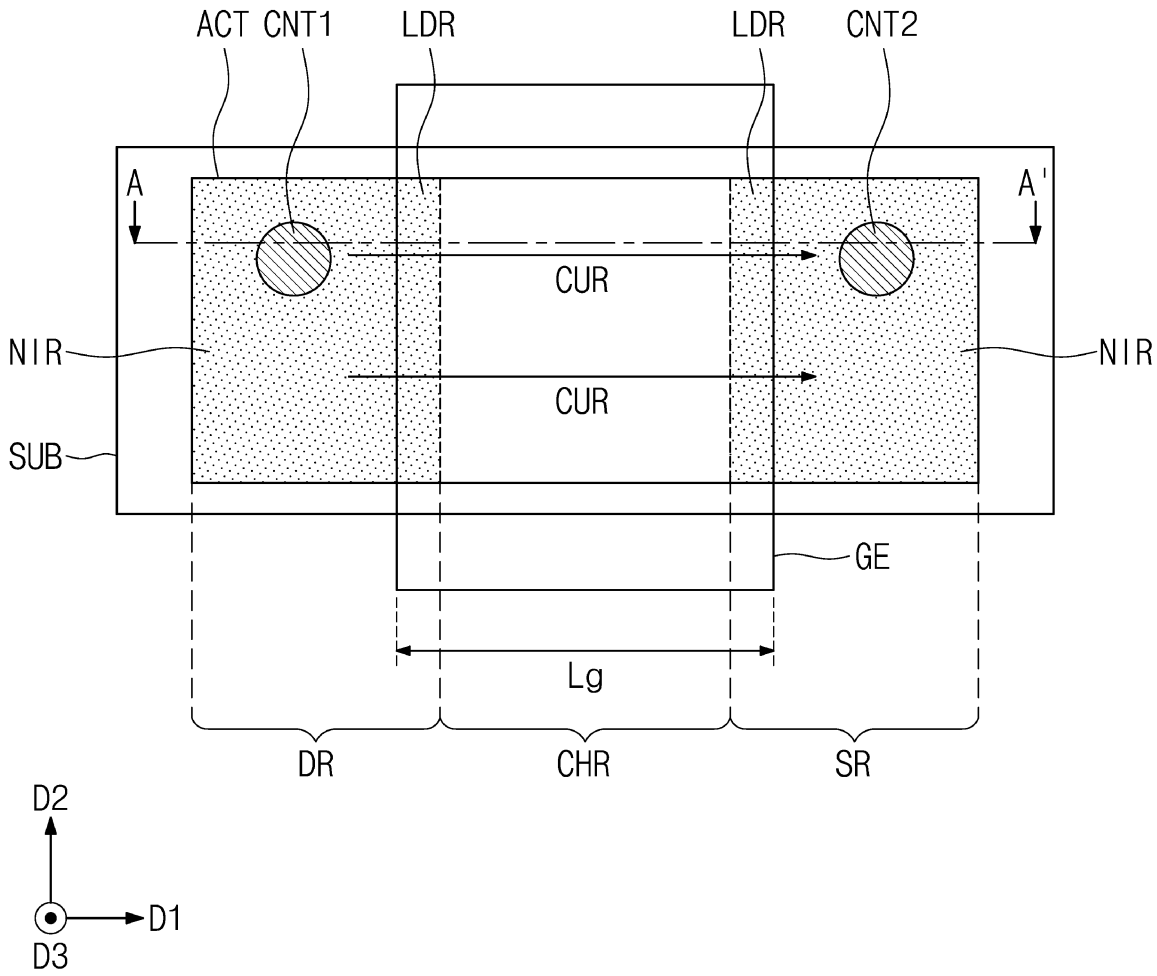

ACT
CNT1
LDR
LDR
CNT2
A
A'
CUR
CUR
NIR
NIR
SUB
GE
Lg
DR
CHR
SR
D2
D1
D3

FIG. 7

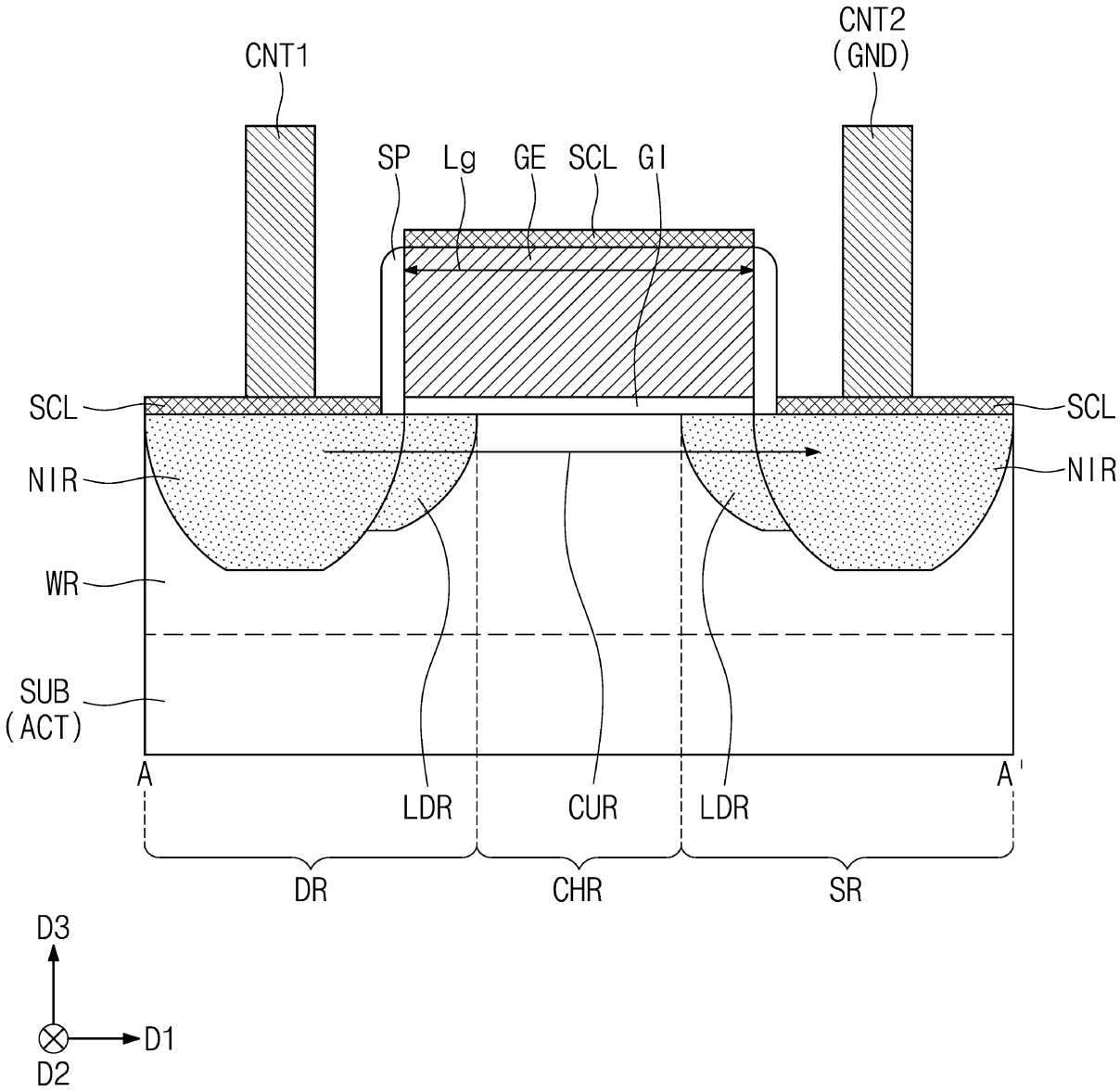

CNT1
CNT2
(GND)
SP
Lg
GE
SCL
GI
SCL
SCL
NIR
NIR
WR
SUB
(ACT)
A
A'
LDR
CUR
LDR
DR
CHR
SR
D3
D1
D2

FIG. 8

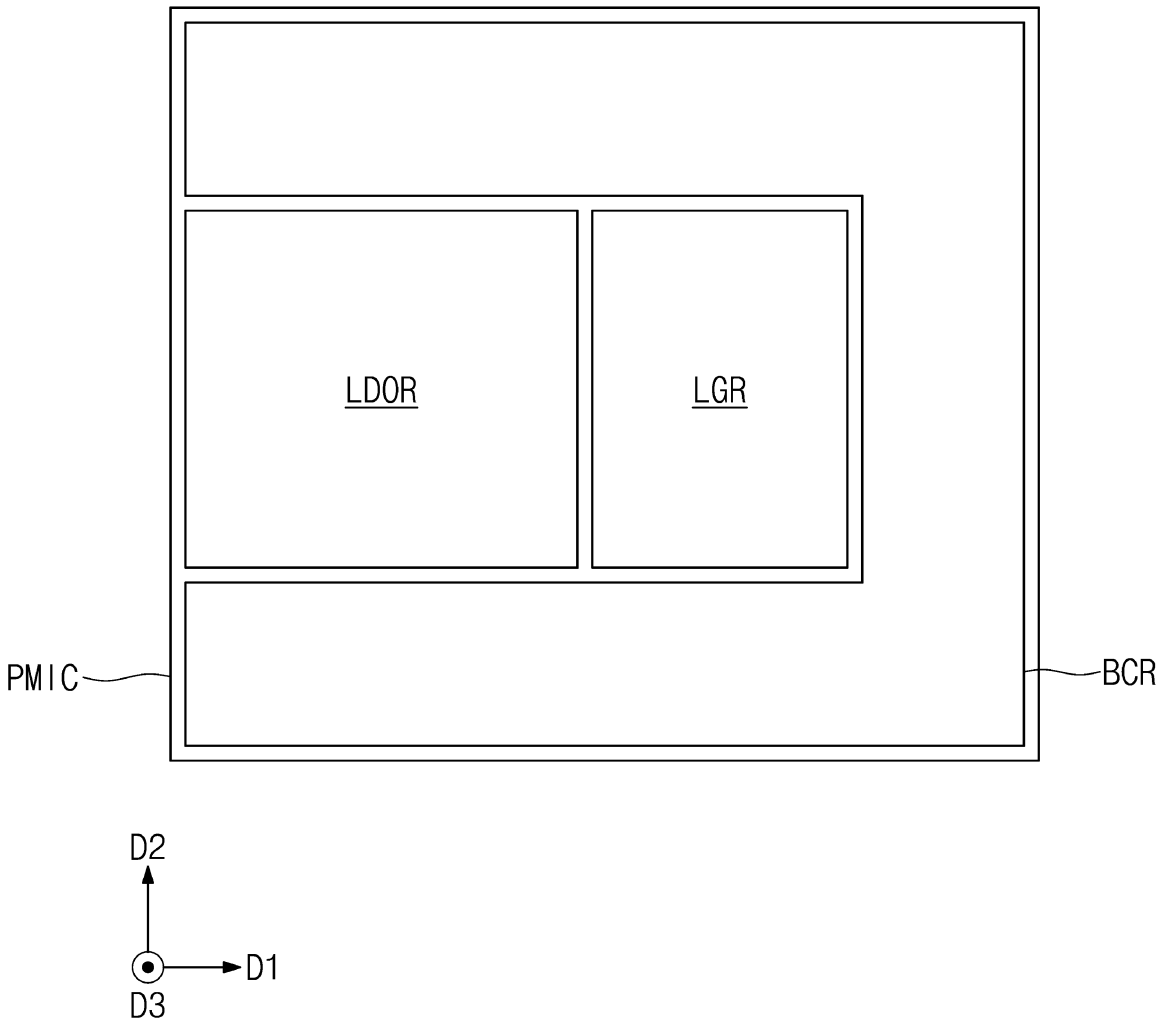


FIG. 9

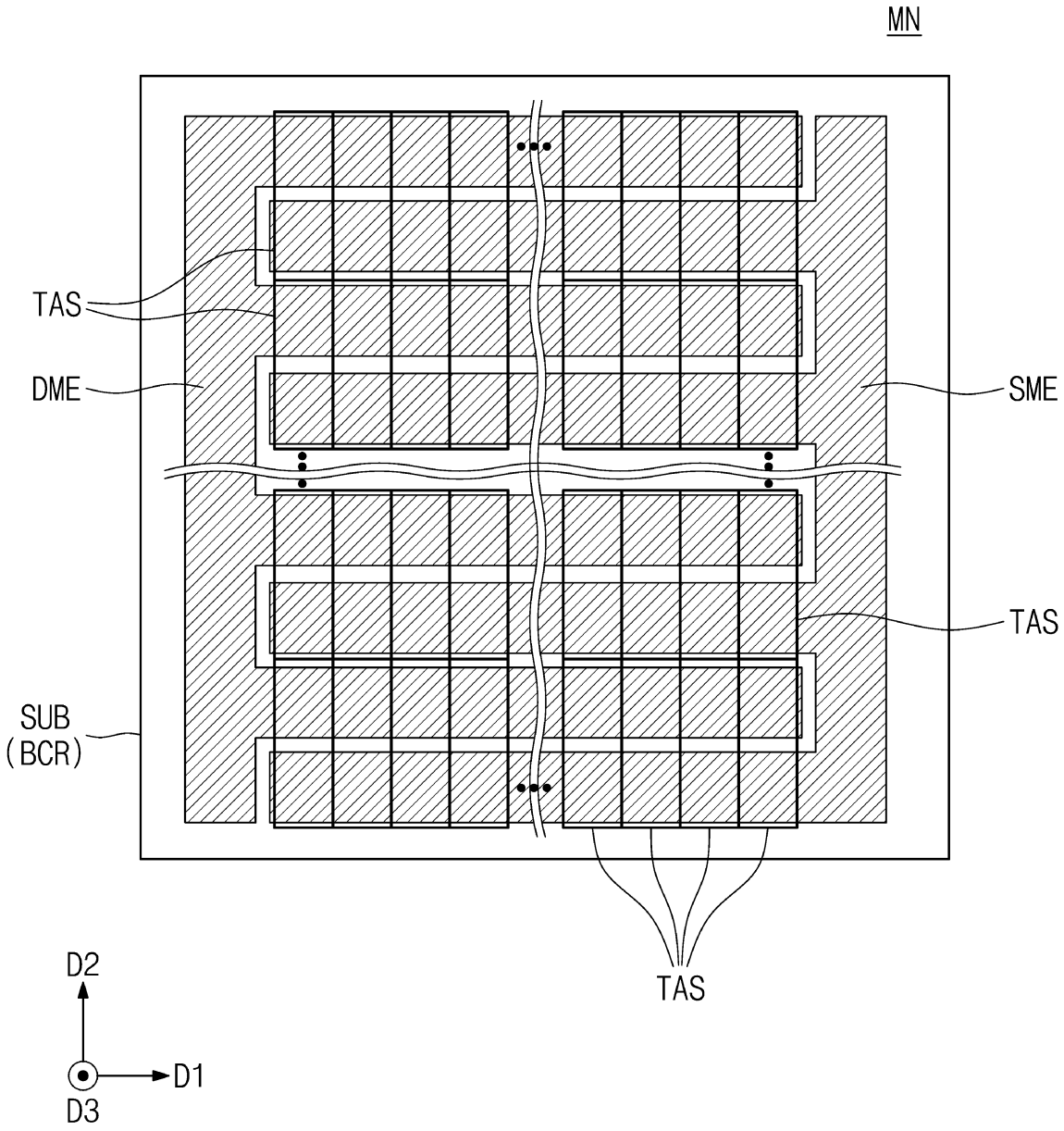


FIG. 10

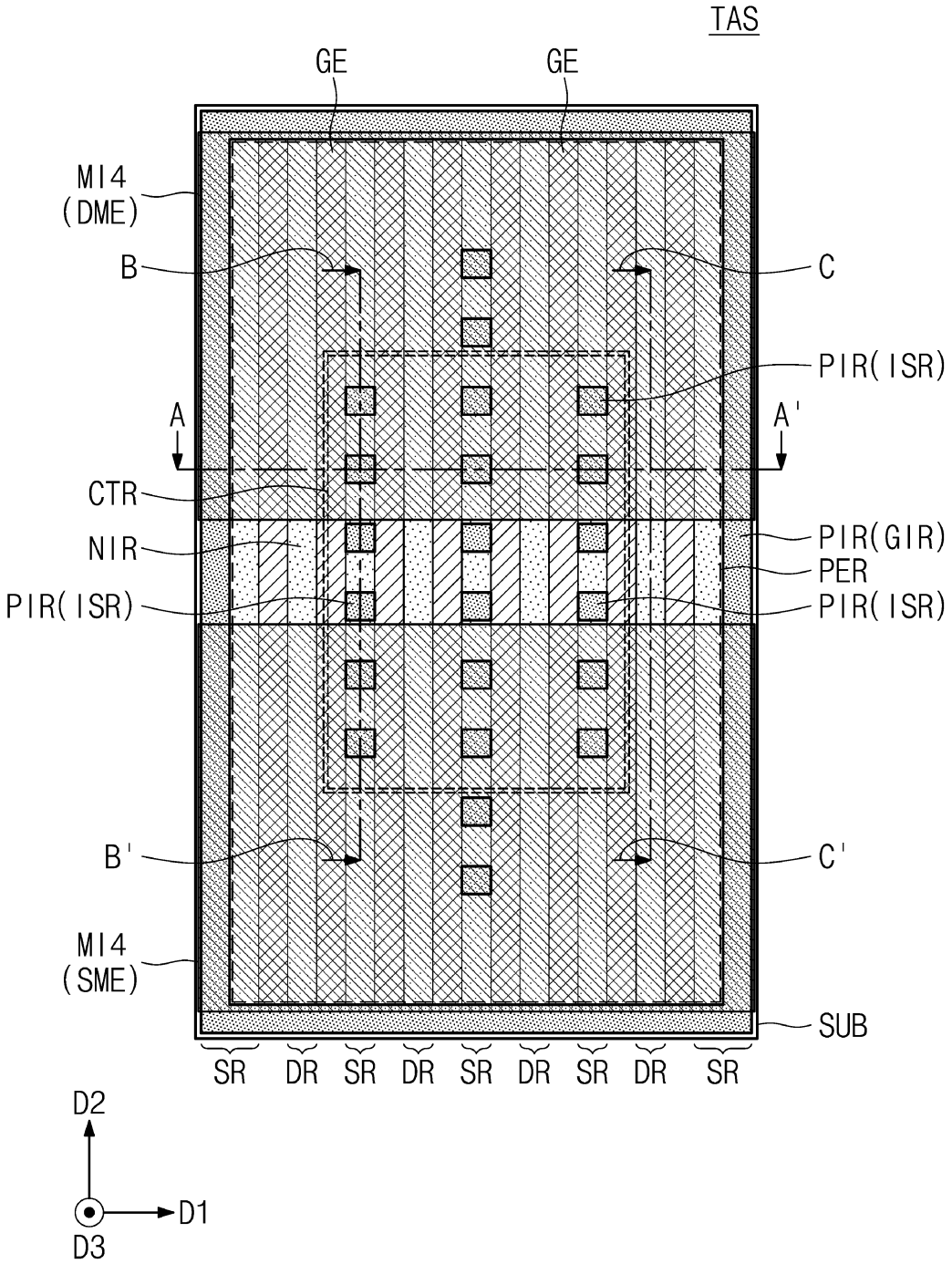

TAS
GE
GE
MI4
(DME)
B
C
PIR(ISR)
A
A'
CTR
NIR
PIR(GIR)
PER
PIR(ISR)
PIR(ISR)
B'
C'
MI4
(SME)
SUB
SR
DR
SR
DR
SR
DR
SR
DR
SR
D2
D1
D3

FIG. 11A

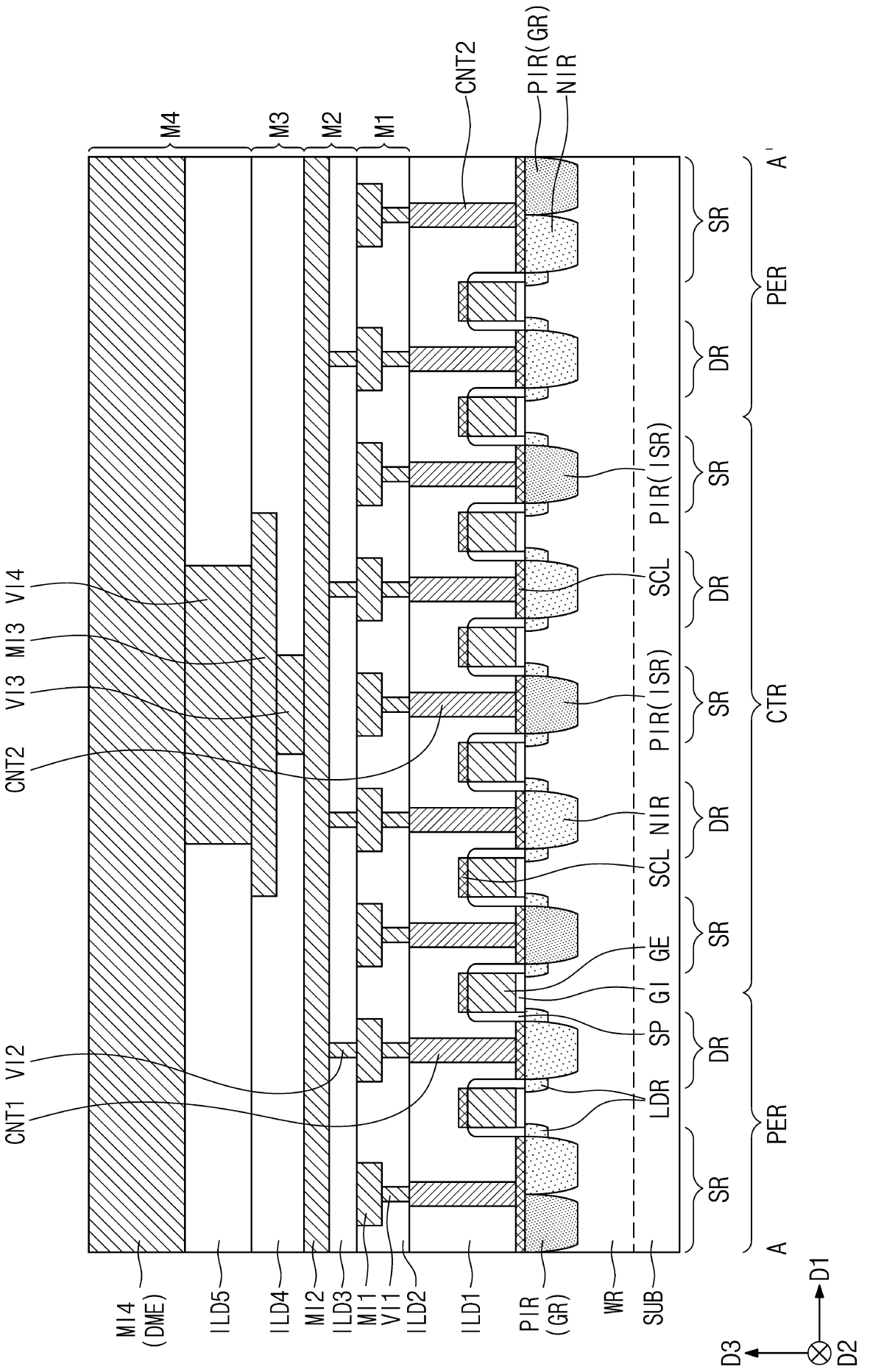

M4
M3
M2
M1
CNT2
PIR(GR)
NIR
VI4
MI3
VI3
CNT2
VI2
CNT1
SR
DR
SR
DR
SR
DR
SR
DR
SR
PIR(ISR)
SCL
PIR(ISR)
SCL
NIR
GE
GI
SP
LDR
A
PER
CTR
PER
A'
MI4 (DME)
ILD5
ILD4
MI2
ILD3
MI1
VI1
ILD2
ILD1
PIR (GR)
WR
SUB
D3
D1
D2

FIG. 11B

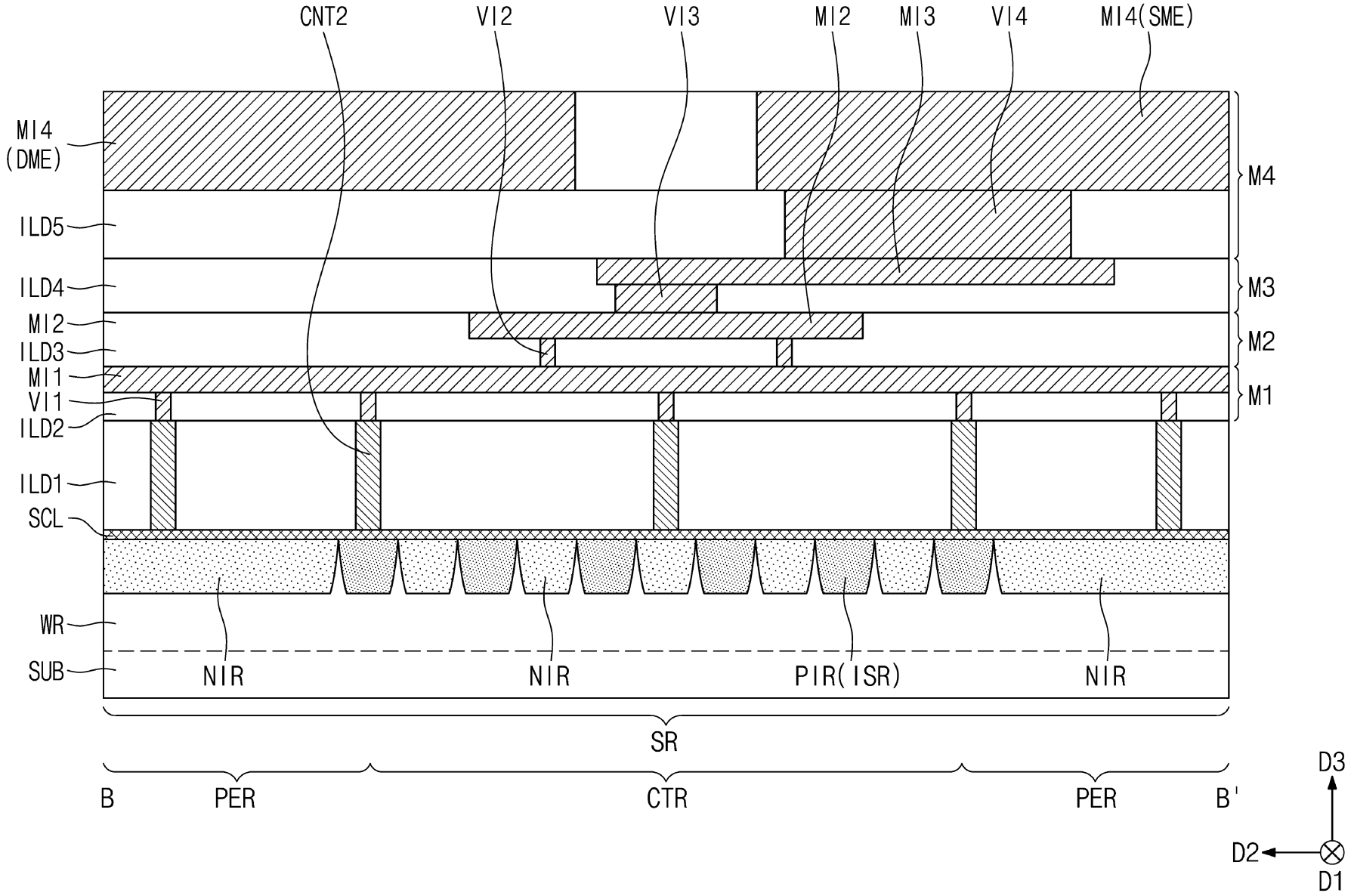

CNT2
VI2
VI3
MI2
MI3
VI4
MI4(SME)
MI4
(DME)
ILD5
ILD4
MI2
ILD3
MI1
VI1
ILD2
ILD1
SCL
WR
SUB
M4
M3
M2
M1
NIR
NIR
PIR(ISR)
NIR
SR
B
PER
CTR
PER
B'
D3
D2
D1

FIG. 11C

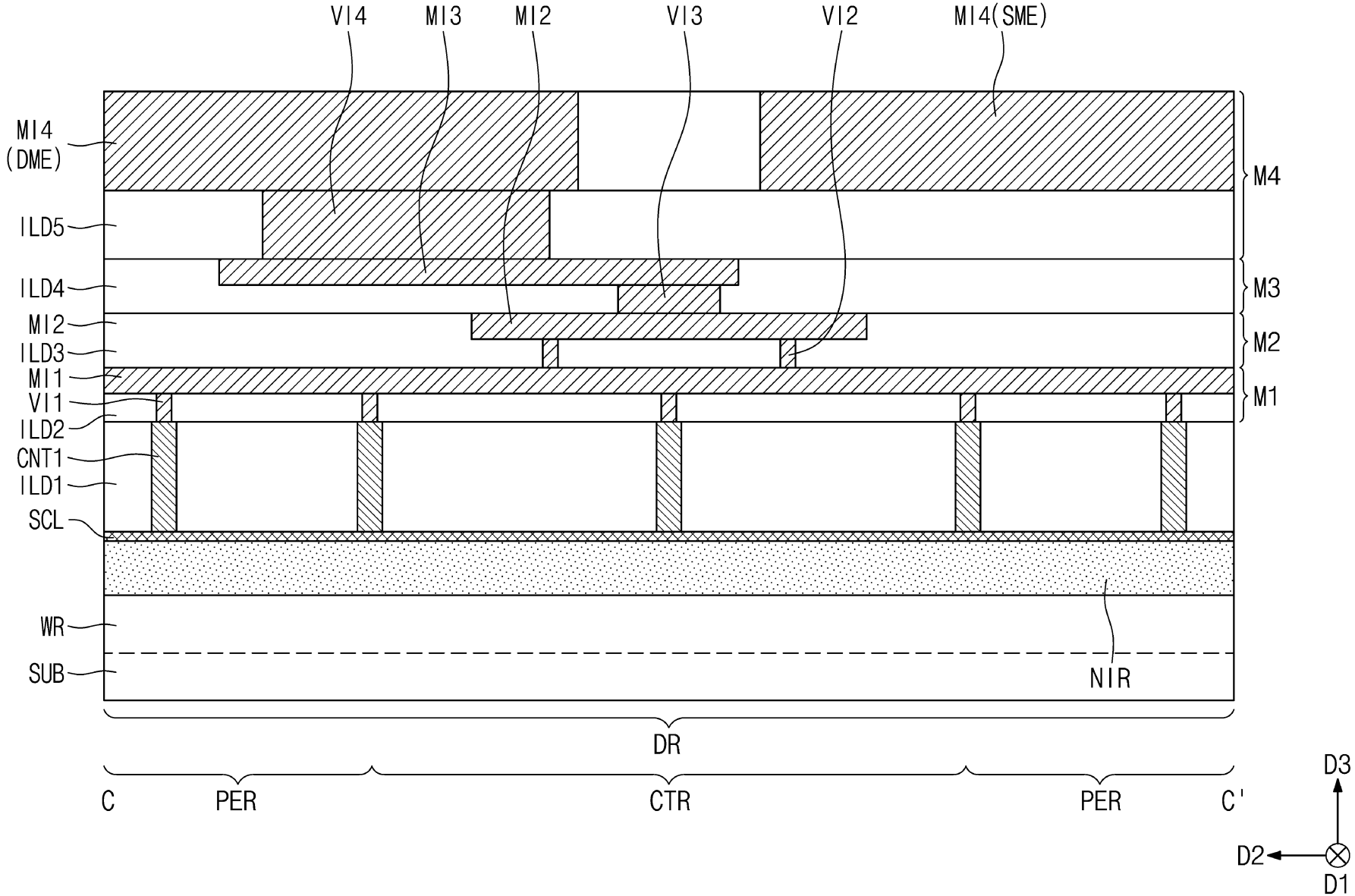

VI4
MI3
MI2
VI3
VI2
MI4(SME)
MI4
(DME)
ILD5
ILD4
MI2
ILD3
MI1
VI1
ILD2
CNT1
ILD1
SCL
WR
SUB
NIR
M4
M3
M2
M1
DR
C
PER
CTR
PER
C'
D3
D2
D1

FIG. 12

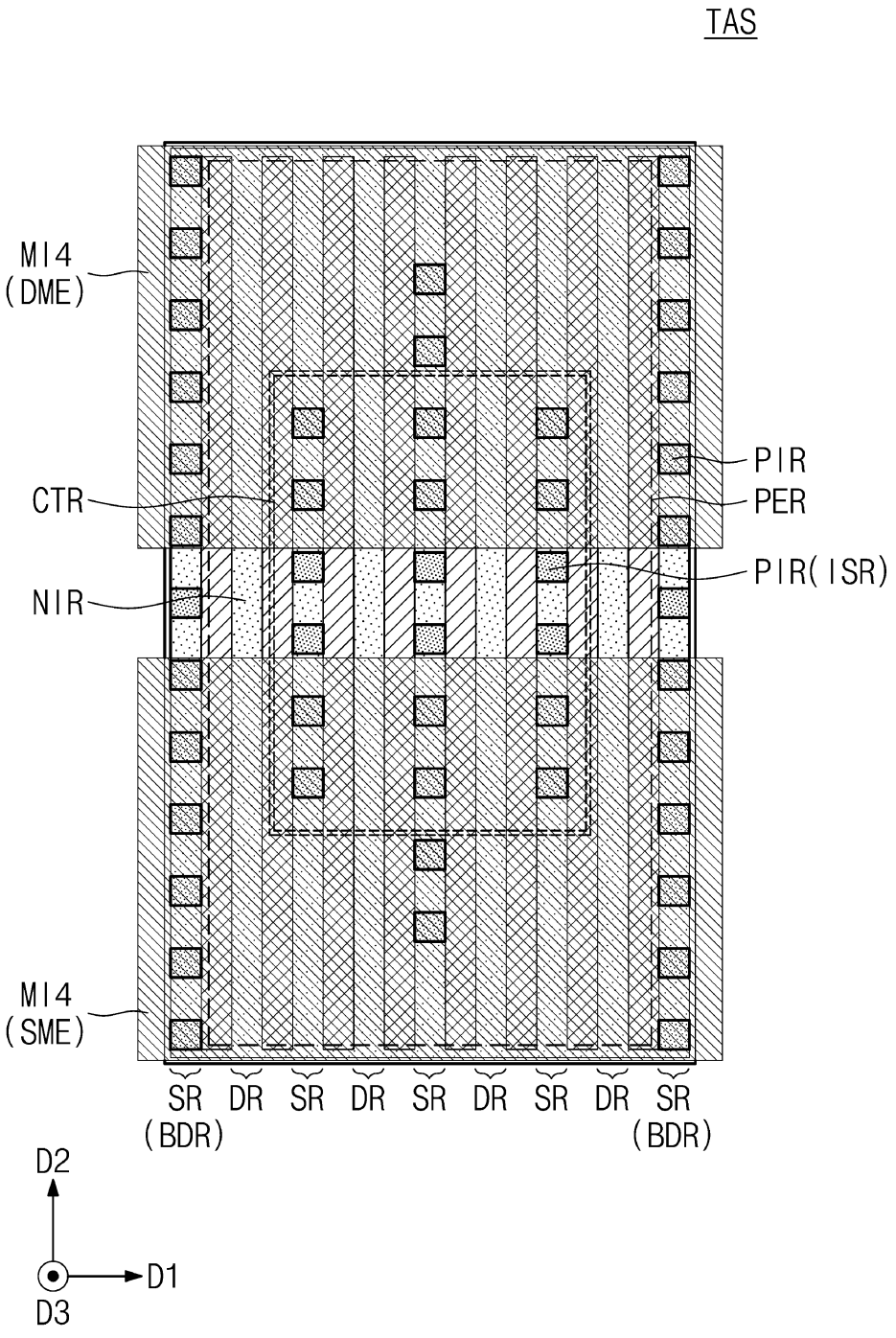

TAS
MI4
(DME)
CTR
NIR
MI4
(SME)
PIR
PER
PIR(ISR)
SR
(BDR)
DR
SR
DR
SR
DR
SR
DR
SR
(BDR)
D2
D1
D3

FIG. 13

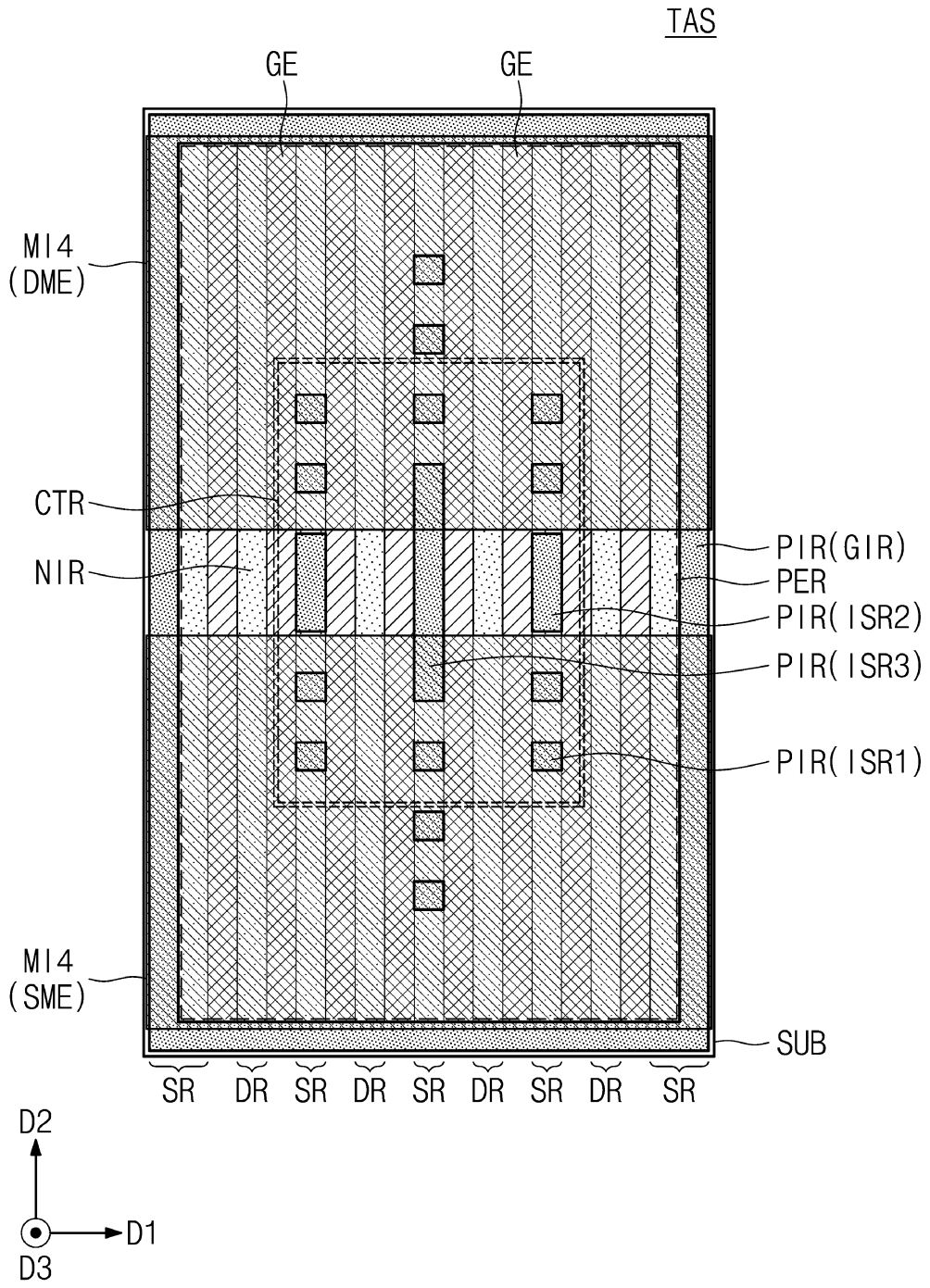

TAS
GE
GE
MI4
(DME)
CTR
NIR
PIR(GIR)
PER
PIR(ISR2)
PIR(ISR3)
PIR(ISR1)
MI4
(SME)
SUB
SR
DR
SR
DR
SR
DR
SR
DR
SR
D2
D1
D3

FIG. 14

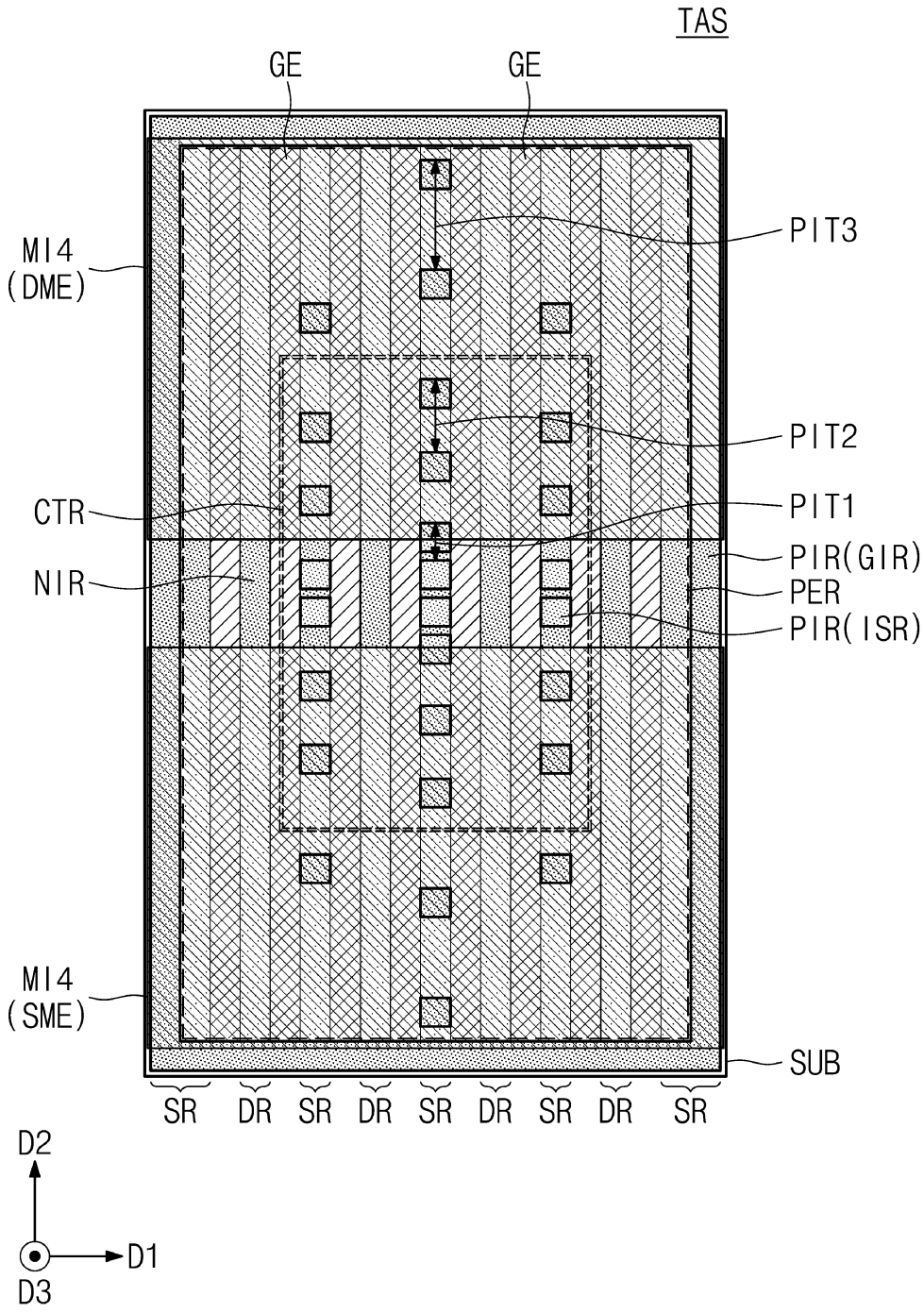

TAS
GE
GE
MI4
(DME)
PIT3
PIT2
CTR
PIT1
NIR
PIR(GIR)
PER
PIR(ISR)
MI4
(SME)
SUB
SR
DR
SR
DR
SR
DR
SR
DR
SR
D2
D1
D3

FIG. 15

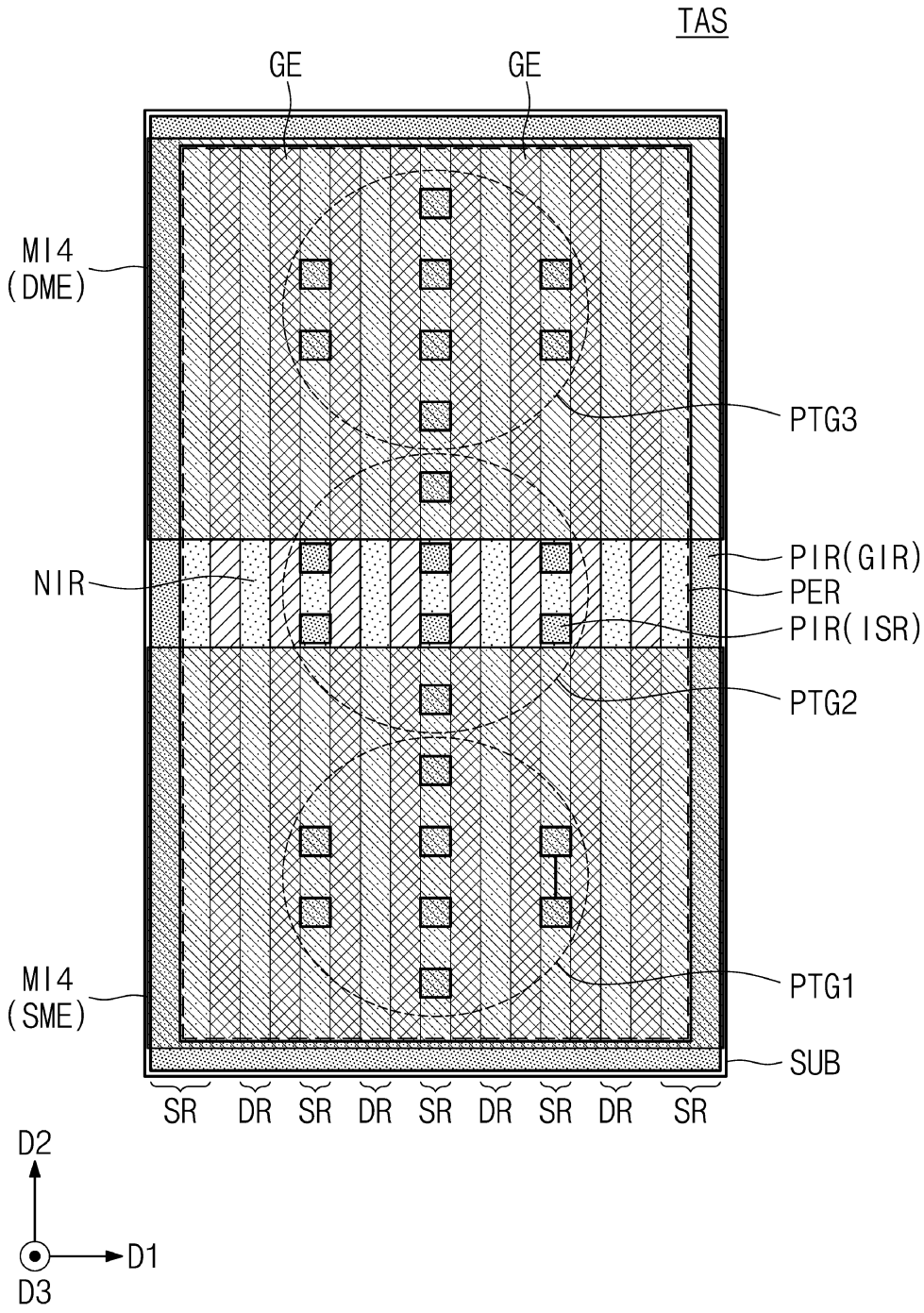

TAS
GE
GE
MI4
(DME)
PTG3
NIR
PIR(GIR)
PER
PIR(ISR)
PTG2
MI4
(SME)
PTG1
SUB
SR
DR
SR
DR
SR
DR
SR
DR
SR
D2
D1
D3

FIG. 16

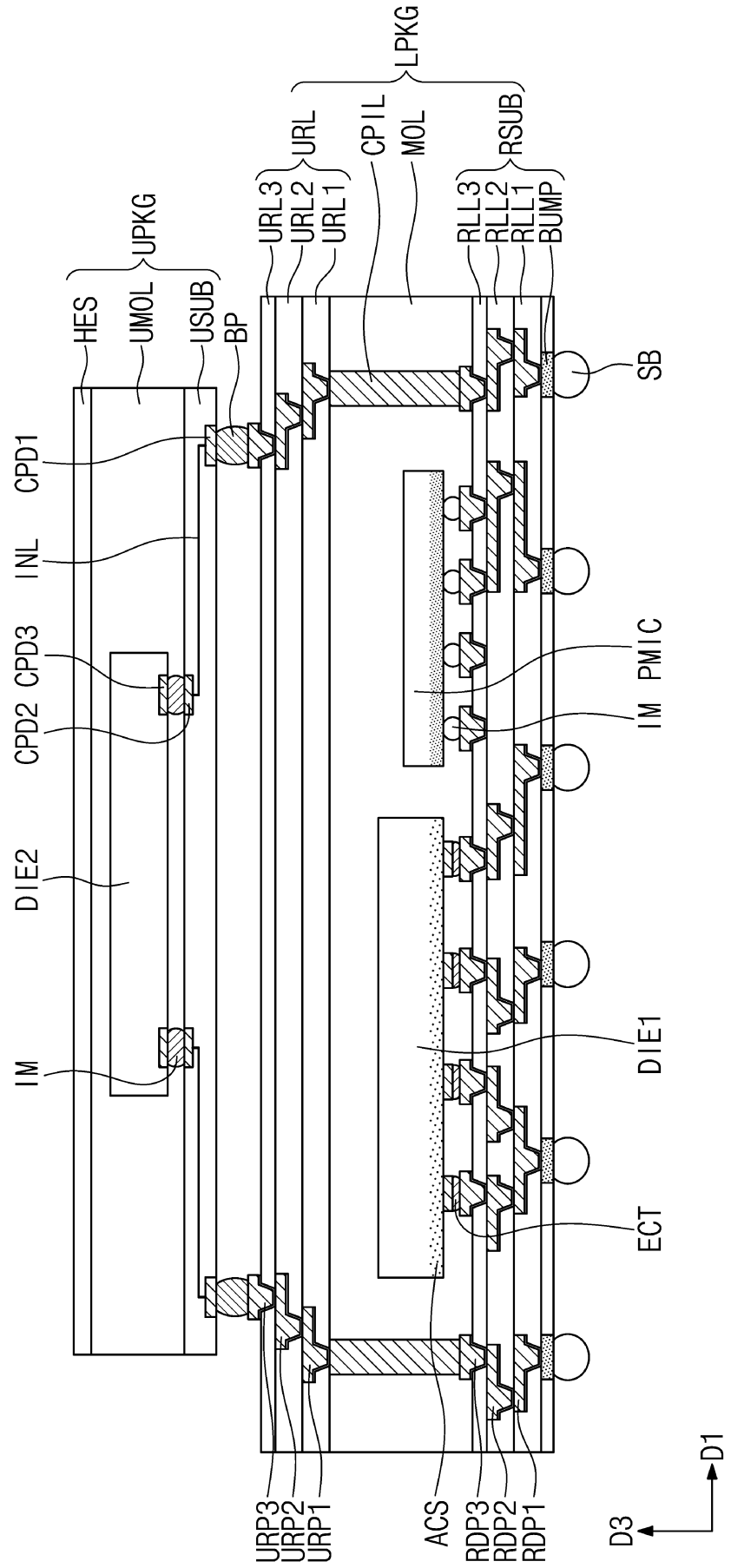
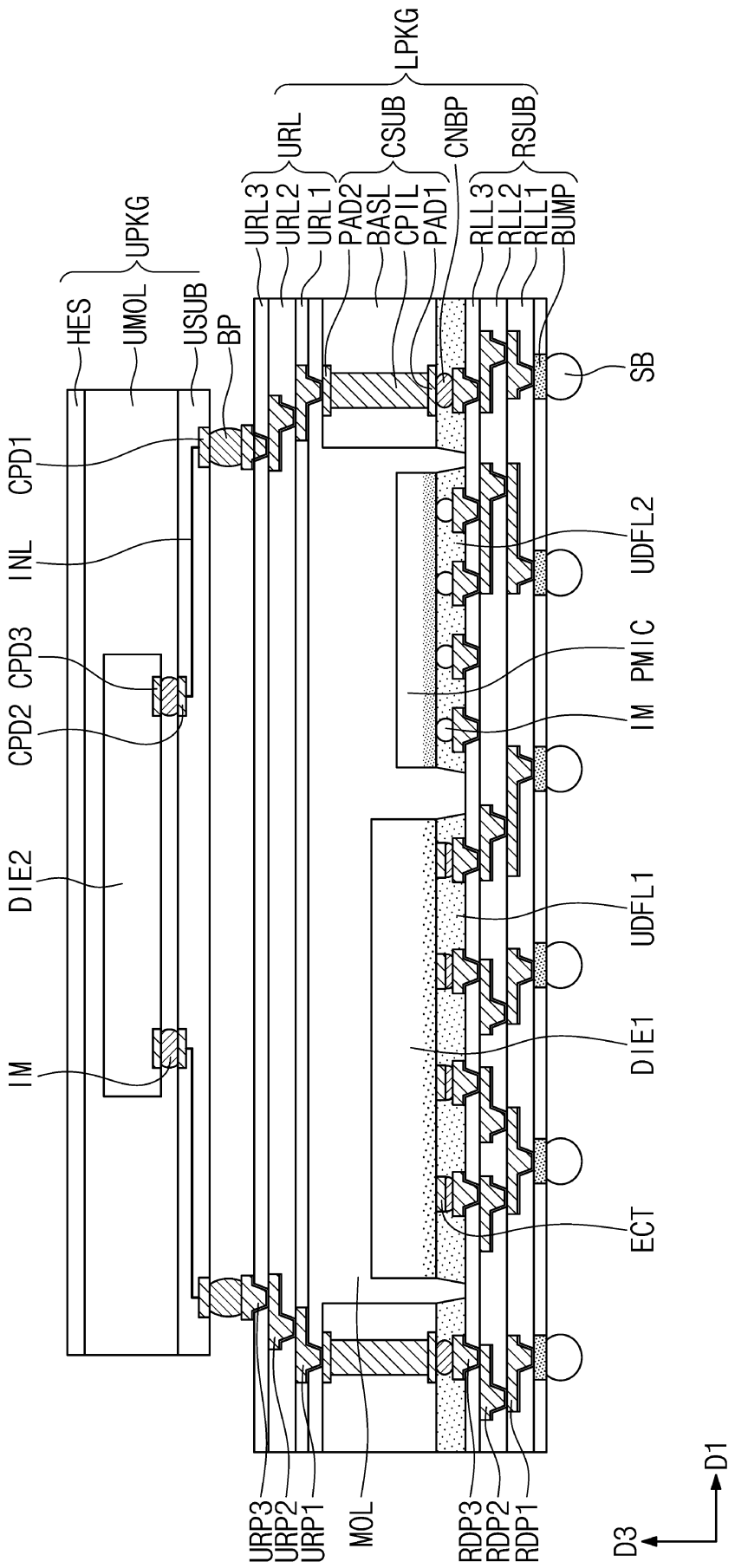

HES
UMOL
USUB
BP
UPKG
URL3
URL2
URL1
URL
CPIL
MOL
RLL3
RLL2
RLL1
BUMP
RSUB
LPKG
SB
CPD1
INL
CPD3
CPD2
DIE2
IM
PMIC
IM
DIE1
ECT
URP3
URP2
URP1
ACS
RDP3
RDP2
RDP1
D3
D1

FIG. 17


HES
UMOL
USUB
BP
UPKG
URL3
URL2
URL1
PAD2
BASL
CPIL
PAD1
CNBP
RLL3
RLL2
RLL1
BUMP
URL
CSUB
RSUB
LPKG
SB
CPD1
INL
CPD3
CPD2
DIE2
IM
UDFL2
PMIC
IM
UDFL1
DIE1
ECT
URP3
URP2
URP1
MOL
RDP3
RDP2
RDP1
D3
D1