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(54) Title: SILICON-CONTAINING LAYER FOR BIT LINE RESISTANCE REDUCTION

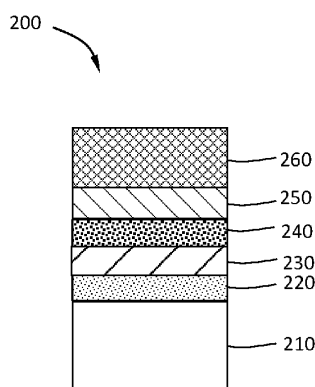


FIG. 2

(57) Abstract: Bit line stacks and methods of forming bit line stacks are described herein. A bit line stack comprises: a polysilicon layer; an adhesion layer on the polysilicon layer; a barrier metal layer on the adhesion layer; an interface layer on the barrier metal layer; a resistance reducing layer on the interface layer; and a conductive layer on the resistance reducing layer. A bit line stack having the resistance reducing layer has a resistance at least 5% lower than a comparable bit line stack without the resistance reducing layer. The resistance reducing layer may include silicon oxide or silicon nitride. The resistance reducing layer may be formed using one or more of a physical vapor deposition (PVD), a radio frequency-PVD, a pulsed-PVD, chemical vapor deposition (CVD), atomic layer deposition (ALD) or sputtering process.

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