What is claimed is:

1. A three-dimensional semiconductor device comprising:

a lower structure;

a stacked structure disposed in a first region and a second region on the lower structure, the stacked structure including gate patterns stacked in a vertical direction, perpendicular to an upper surface of the lower structure, the gate patterns including pad regions disposed in a stepped structure in the second region; and

vertical channel structures disposed on the lower structure and having a side surface facing the gate patterns, wherein:

the stacked structure includes a first stacked region, a second stacked region and a third stacked region that are sequentially arranged in the second region in a first direction,

the first stacked region includes a first stepped region, having a stepped structure changing in a unit of a first height,

the second stacked region includes a second stepped region, having a stepped structure, lowered in a unit of a second height, greater than the first height in the first direction,

the third stacked region includes ~~an~~ a first upwardly stepped region and a first downwardly stepped region,

the first upwardly stepped region of the third stacked region has a stepped structure raising in a unit of the second height in the first direction, ~~and~~

the first downwardly stepped region of the third stacked region has a stepped structure lowered in a unit of the second height in the first direction,

the second stepped region of the second stacked region, the first upwardly stepped region of the third stacked region and the first downwardly stepped region of the third stacked region are sequentially arranged in the first direction, and

the first upwardly stepped region of the third stacked region is at a lower level than the second stepped region of the second stacked region, and

the first downwardly stepped region of the third stacked region is at a lower level than the first upwardly stepped region of the third stacked region.

2. The three-dimensional semiconductor device according to claim 1, wherein the second stacked region has a sidewall facing the first upwardly stepped region at the same level as the first upwardly stepped region, and

a slope of the sidewall of the second stacked region is steeper than a slope of the first upwardly stepped region~~the upwardly stepped region of the third stacked region and the downwardly stepped region of the third stacked region are sequentially arranged in the first direction~~.

3. The three-dimensional semiconductor device according to claim 1 or claim 2, wherein:

~~the upwardly stepped region of~~ the third stacked region further includes ~~a first upwardly stepped region and~~ a second upwardly stepped region, ~~positioned on different height levels and~~

the second upwardly stepped region is at a higher level than the first upwardly stepped region,

the first upwardly stepped region and the second upwardly stepped region are sequentially arranged in a second direction,

~~the downwardly stepped region of~~ the third stacked region further includes ~~a first downwardly stepped region and~~ a second downwardly stepped region, ~~which are positioned on different height levels and~~

the second downwardly stepped region is at a higher level than the first downwardly stepped region,

the first downwardly stepped region and the second downwardly stepped region are sequentially arranged in the second direction, and

the second direction is parallel to the upper surface of the lower structure and perpendicular to the first direction.

4. The three-dimensional semiconductor device according to claim 3, wherein:

~~the first upwardly stepped region of the third stacked region and the first downwardly stepped region of the third stacked region are sequentially arranged in the first direction,~~

the second upwardly stepped region of the third stacked region and the second downwardly stepped region of the third stacked region are sequentially arranged in the first direction,

pad regions of the first downwardly stepped region of the third stacked region are positioned on a lower level than pad regions of the first upwardly stepped region of the third stacked region, and

pad regions of the second downwardly stepped region of the third stacked region are positioned on a lower level than pad regions of the second upwardly stepped region of the third stacked region.

5. The three-dimensional semiconductor device according to claim 4, wherein:

the pad regions in the first upwardly stepped region of the third stacked region are disposed in a stepped structure in which the pad regions are raised in a unit of the first height in the second direction and in a unit of the second height in the first direction, and

the pad regions of the second upwardly stepped region of the third stacked region are disposed in a stepped structure in which the pad regions are raised in a unit of the second height in the first direction.

6. The three-dimensional semiconductor device according to claim 4, wherein:

the pad regions of the first downwardly stepped region of the third stacked region are disposed in a stepped structure in which the pad regions are raised in a unit of the first height in the second direction and lowered in a unit of the second height in the first direction, and

the pad regions of the second downwardly stepped region of the third stacked region are disposed in a stepped structure in which the pad regions are lowered in a unit of the second height in the first direction.

7. The three-dimensional semiconductor device according to claim 4, wherein:

the second stacked region includes a first downwardly stepped region in which the pad regions that are lowered in a unit of the second height in the first direction and raised in a unit of the first height in the second direction are positioned, and a second downwardly stepped region in which the pad regions that are lowered in a unit of the second height in the first direction are positioned, and

the pad regions of the second downwardly stepped region of the second stacked region are positioned on a same high level as the pad regions adjacent to the second downwardly stepped region of the second stacked region, among the pad regions of the first downwardly stepped region of the second stacked region.

8. The three-dimensional semiconductor device according to claim 7, wherein:

the pad regions of the first upwardly stepped region of the third stacked region are lowered from the first downwardly stepped region of the second stacked region in a unit of a third height, and then raised in a unit of the second height in the first direction,

the pad regions of the first downwardly stepped region of the third stacked region are lowered from the first upwardly stepped region of the third stacked region in a unit of the third height, and then lowered in a unit of the second height in the first direction,

the pad regions of the second downwardly stepped region of the third stacked region are lowered from the second upwardly stepped region of the third stacked region in a unit of the third height, and then lowered in a unit of the second height in the first direction, and

the third height is higher than the second height.

9. The three-dimensional semiconductor device according to any one of claims 1 to 8, wherein:

the third stacked region includes a plurality of stacked portions, and

each of the stacked portions includes an upwardly stepped region of the third stacked region and a downwardly stepped region of the third stacked region which are sequentially arranged in the first direction.

10. The three-dimensional semiconductor device according to claim 9, wherein:

the plurality of stacked portions includes a first stacked portion adjacent to the second stacked region, and an n^{th} stacked portion positioned 'n^{th}' from the first stacked portion in the first direction,

the first stacked portion includes an upwardly stepped region in which the pad regions are lowered from the second stacked region in a unit of a third height, and then raised in a unit of a second height,

the n^{th} stacked portion includes an upwardly stepped region in which the pad regions are lowered from the downwardly stepped region of the $(n-1)^{th}$ stacked portion in a unit of a third height, and then raised in a unit of a second height, and

where 'n' is a positive integer greater than 2.

11. The three-dimensional semiconductor device according to claim 10, wherein a slope of a region lowered in a unit of the third height between the first stacked portion and the second stacked region is different from a slope of a region lowered in a unit of the third height between the $(n-1)^{th}$ stacked portion and the n^{th} stacked portion.

12. A three-dimensional semiconductor device comprising:

a lower structure;

a stacked structure disposed on the lower structure, and including gate patterns stacked in a vertical direction, perpendicular to an upper surface of the lower structure; and

vertical channel structures disposed on the lower structure and having a side surface facing the gate patterns, wherein:

the stacked structure includes a first stepped region having a stepped structure changing in a unit of a first height, a second stepped region in which pad regions that are lowered in a unit of a second height greater than the first height in a first direction are positioned, an upwardly stepped region in which pad regions that are raised in ~~a~~ the first

direction are positioned, and a downwardly stepped region in which pad regions lowered in the first direction are positioned,

the first stepped region, the second stepped region, the upwardly stepped region, and the downwardly stepped region are sequentially arranged in the first direction,

the upwardly stepped region includes a first upwardly stepped region in which pad regions that are raised in a unit of the second height in the first direction are positioned and a second upwardly stepped region in which pad regions that are raised in a unit of the second height in the first direction are positioned, and the first upwardly stepped region and the second upwardly stepped region are positioned on different height levels and are sequentially arranged in a second direction,

the downwardly stepped region includes a first downwardly stepped region in which pad regions that are lowered in a unit of the second height in the first direction are positioned and a second downwardly stepped region in which pad regions that are lowered in a unit of the second height in the first direction are positioned, and the first downwardly stepped region and the second downwardly stepped region are positioned on different height levels and are sequentially arranged in the second direction, ~~and~~

the second direction is parallel to an upper surface of the lower structure and perpendicular to the first direction,

the first upwardly stepped region and the first downwardly stepped region are sequentially arranged in the first direction,

the first upwardly stepped region is at a lower level than the second stepped region,

the first downwardly stepped region is at a lower level than the first upwardly stepped region,

the second downwardly stepped region is at a lower level than the second upwardly stepped region and is at a higher level than the first downwardly stepped region.

13. The three-dimensional semiconductor device according to claim 12, wherein:

the first upwardly stepped region is a region in which the pad regions that are raised in a unit of ~~a~~ the first height in the second direction ~~and in a unit of a second height higher than the first height in the first direction~~ are positioned, and

the second upwardly stepped region is a region in which the pad regions that are positioned on a level higher than the first upwardly stepped region ~~and are raised in a unit of the second height in the first direction~~ are positioned.

14. The three-dimensional semiconductor device according to claim 12 or claim 13, wherein:

the first downwardly stepped region is a region in which the pad regions that are raised in a unit of the first height in the second direction ~~and lowered in a unit of the second height in the first direction~~ are positioned, and

the second downwardly stepped region is a region in which the pad regions that are positioned on a level higher than the first downwardly stepped region ~~and are raised in a unit of the second height in the first direction~~ are positioned.

15. A three-dimensional semiconductor device comprising:

a first gate group on a lower structure; ~~and~~

a second gate group on the first gate group; and

an upper gate group on the second gate group, wherein:

the first gate group includes a first downwardly stepped region and a second downwardly stepped region,

the second gate group includes a first upwardly stepped region and a second upwardly stepped region,

the first and second downwardly stepped regions of the first gate group include~~s~~ first pad regions lowered in a first direction, parallel to an upper surface of the lower structure and that are raised in a second direction, parallel to an upper surface of the lower structure and perpendicular to the first direction, and

the first and second upwardly stepped regions of the second gate group includes second pad regions that are sequentially raised in the first direction and are raised in the second direction,

the upper gate group includes an upper downwardly stepped region including upper pad regions lowered in the first direction,

the upper downwardly stepped region, the first upwardly stepped region and the first downwardly stepped region are sequentially arranged in the first direction,

the first upwardly stepped region is at a lower level than the upper downwardly stepped region, and

the first downwardly stepped region is at a lower level than the first upwardly stepped region,

the second upwardly stepped region is at a higher level than the first upwardly region, and

the second downwardly stepped region is at a lower level than the second upwardly stepped region and is at a higher level than the first downwardly stepped region.

16. The three-dimensional semiconductor device according to claim 15, wherein:

each of the first and second gate groups includes:

first gate portions stacked and spaced in a vertical direction;

second gate portions stacked and spaced in the vertical direction; and

connection patterns connecting the first gate portions and the second gate portions, and

the first gate portion, the second gate portion, and the connection pattern positioned on a same plane among the first gate portions, the second gate portions and the connection patterns are formed one conductor electrically connected to each other.

17. The three-dimensional semiconductor device according to claim 15 or claim 16, wherein:

the first pad regions are disposed in a stepped structure that are raised in a unit of a first height in the second direction and that are lowered in a unit of a second height, greater than the first height in the first direction, and

the second pad regions are disposed in a stepped structure that are raised in a unit of the first height in the second direction and that are raised in a unit of the second height in the first direction.

18. The three-dimensional semiconductor device according to claim 16 or claim 17, further comprising:

peripheral contact structures passing through the first and second gate groups, wherein:

the lower structure includes a first substrate, a peripheral circuit structure including peripheral pads on the first substrate, and a second substrate on the peripheral circuit structure, and

the peripheral contact structures contact the peripheral pads.

19. The three-dimensional semiconductor device according to claim 18, further comprising:

an insulation region passing through the first and second gate groups, wherein the peripheral contact structures pass through the insulation region.

20. The three-dimensional semiconductor device according to claim 19, wherein:

the first pad regions include first lower pad regions positioned on a lowest level and first upper pad regions positioned on a highest level among the first pad regions disposed in the first direction, and

the insulation region includes one or both of a first insulation region passing through at least a portion of the first lower pad regions and a second insulation region passing through at least a portion of the first upper pad regions.