METHOD FOR FABRICATING SEMICONDUCTOR COMPONENTS USING MASKLESS BACK SIDE ALIGNMENT TO CONDUCTIVE VIAS

Background

[0001] Semiconductor components, such as chip scale packages, are being made thinner and smaller than previous generation components. At the same time, electrical and packaging requirements for semiconductor components are becoming more stringent. One challenge during fabrication of semiconductor components is the alignment of elements on the back side of a semiconductor substrate to elements on the circuit side. For example, conductive vias interconnect circuit side elements, such as circuit side conductors and bond pads, to back side elements, such as back side conductors and terminal contacts. The conductive vias are becoming smaller, such that conventional fabrication processes for aligning the conductive vias to back side elements are becoming more difficult.

[0002] Figures 1A-1E illustrate a semiconductor fabrication process in which the alignment of conductive vias in a semiconductor substrate to back side features on the substrate is an issue. As shown in Figure 1A, a semiconductor wafer 10 includes a plurality of semiconductor substrates 12, such as semiconductor dice. The semiconductor wafer 10, and each of the semiconductor substrates 12 as well, include a circuit side 16 and a back side 18. In addition, each semiconductor substrate 12 includes a plurality of conductive vias 14 extending from circuit side 16 to the back side 18 thereof. Each conductive via 14 comprises a through via 20 in the semiconductor substrate 12 lined with a via insulator 22 and filled with a conductive metal.

[0003] As also shown in Figure 1A, each semiconductor substrate 12 also includes a plurality of redistribution conductors 24 on the circuit side 16 in electrical communication with the conductive vias 14. The redistribution conductors 24 are insulated from the semiconductor substrate 12 by an inner dielectric layer 26, and are covered by an outer dielectric layer 28. The wafer 10 is attached to a wafer carrier 30 using a carrier adhesive 32, which permits back side fabrication processes, such as back side thinning and planarization, to be performed. These processes planarize the substrate 12, and form planarized contactors 42 (Figure 1A) on the ends of the conductive vias 14. The wafer carrier 30 also allows other processes to be performed, such as the formation of back side elements (e.g., terminal contacts). In the present

case, a photo patterning process is being performed to form back side conductors 34 in electrical communication with the conductive vias 14.

[0004] As shown in Figure 1B, the photo patterning process is initiated by depositing a layer of resist 36 on the back side 18 of the wafer 10. The layer of resist 36 can be deposited using a conventional process such as spin coating. Next, as shown in Figure 1C, the layer of resist 36 can be exposed and developed to form a photo mask 38 on the back side 18 of the wafer 10. The photo mask 38 includes a plurality of openings 40 which should align with the exposed contactors 42 on the conductive vias 14. Alignment can be achieved using alignment marks on the circuit side 16 and on the back side 18 of the wafer 10. However, due to the size of the conductive vias 14 and the size of the openings 40, and the limitations of conventional photo exposure equipment, alignment can be difficult to achieve. As shown in Figure 2A, in order to facilitate alignment, the conductive vias 14 can be made larger than the openings 40 (represented by dotted lines in Figure 2A) in the photo mask 38. For example, the conductive vias 14 can have an inside diameter (ID) of about 18 μm, and the openings 40 in the photo mask 38 can have a diameter (OD) of about 11 μm . This allows misalignment of about 3.5 μm on each side of the conductive vias 14 to occur.

[0005] Figure 2A illustrates the optimal alignment situation wherein the centers of the conductive vias 14 and the centers of the openings 40 are in perfect alignment. However, as shown in Figure 2B, in actual practice, the openings 40 in the photo mask 38 does not perfectly align with the conductive vias 14. As will be further explained, this situation can cause short circuits 44 (Figure 2D) to form between the conductors 34 (Figure 2D) and the substrate 12. As shown in Figure 2C, the openings 40 in the photo mask 38 may completely miss the conductive vias 14. As will be further explained, this situation can form open circuits.

[0006] As shown in Figure 1D, following formation of the photo mask 38, the contactors 42 can be etched to remove contaminants and native oxide layers. Next, as shown in Figure 1E, the conductors 34 can be formed in the openings 40 using a process such as electroless deposition. The conductors 34 can comprise a highly conductive metal such as copper. As also shown in Figure 1E, under bump metallization layers 46, 48 for terminal contacts (not shown) can be formed on the

conductors 34. The under bump metallization layers 46, 48 can be formed using a suitable process such as electroless deposition out of suitable metals.

[0007] Figures 2D and 2E illustrate potential problems caused by misalignment of the conductors 34 to the conductive vias 14. As shown in Figure 2D, misalignment by a small amount (e.g., < 5 μm) can cause short circuits 44 between the conductors 34 and the semiconductor substrate 12. As shown in Figure 2E, misalignment by a large amount (e.g., >9 μm) can cause an open circuit between the conductor 34 and the conductive via 14.

[0008] In view of the foregoing, improved methods for fabricating semiconductor components with back side elements are needed in the art. However, the foregoing examples of the related art and limitations related therewith, are intended to be illustrative and not exclusive. Other limitations of the related art will become apparent to those of skill in the art upon a reading of the specification and a study of the drawings.

Brief Description of the Drawings

[0009] Exemplary embodiments are illustrated in the referenced figures of the drawings. It is intended that the embodiments and the figures disclosed herein are to be considered illustrative rather than limiting.

[0010] Figures 1A-1E are schematic cross sectional views illustrating steps in a prior art method for fabricating semiconductor components using a back side photo alignment step;

[0011] Figure 2A is an enlarged schematic cross sectional view taken along line 2A-2A of Figure 1A illustrating a conductive via in the prior art method;

[0012] Figure 2B is an enlarged schematic cross sectional view taken along line 2B-2B of Figure 1C illustrating optimal alignment between the conductive via and a back side resist opening;

[0013] Figure 2C is an enlarged schematic cross sectional view equivalent to Figure 2B illustrating misalignment between the conductive via and the back side resist opening;

[0014] Figure 2D is an enlarged schematic cross sectional view taken along line 2D of Figure 1F illustrating misalignment between the conductive via and a back side conductor producing a short;

[0015] Figure 2E is an enlarged schematic cross sectional view taken equivalent to Figure 2D illustrating misalignment between the conductive via and a back side conductor producing an open;

[0016] Figures 3A-3E are schematic cross sectional views illustrating a method for fabricating semiconductor components using mask less back side conductive via alignment;

[0017] Figure 4A is an enlarged schematic cross sectional view taken along line 4A of Figure 3B illustrating a conductive following an etch back step;

[0018] Figure 4B is an enlarged schematic cross sectional view taken along line 4B of Figure 3C illustrating the conductive via following a polymer deposition step;

[0019] Figure 4C is an enlarged schematic cross sectional view taken along line 4C of Figure 3D illustrating the conductive via following a planarization step;

[0020] Figure 4D is an enlarged schematic cross sectional view taken along line 4D of Figure 3E illustrating alignment of the conductive via and a back side conductor;

[0021] Figure 5A is an enlarged schematic cross sectional view equivalent to Figure 4A illustrating a back side terminal contact in electrical communication with the back side conductor;

[0022] Figure 5B is an enlarged schematic cross sectional view equivalent to Figure 4A illustrating a back side redistribution conductor and terminal contact in electrical communication with the back side conductor;

[0023] Figure 6A is a plan view of a semiconductor component fabricated in accordance with the method of Figures 3A-3E;

[0024] Figure 6B is a side elevation view of the semiconductor component;

[0025] Figure 6C is a cross sectional view of the semiconductor component taken along section line 6C-6C of Figure 6B; and

[0026] Figure 7 is a schematic side elevation view of stacked components fabricated in accordance with the method of Figures 3A-3E.

Detailed Description

[0027] As used herein, "semiconductor component" means an electronic element that includes a semiconductor substrate having integrated circuits and

semiconductor devices. "Wafer-level" means a process conducted on an element, such as a semiconductor wafer, containing multiple semiconductor components. "Chip scale" means a semiconductor component having an outline about the same as that of a semiconductor die.

[0028] Referring to Figures 3A-3E, a method for fabricating semiconductor components using maskless back side alignment to conductive vias is illustrated. As shown in Figure 3A, a semiconductor wafer 50 can be provided. The semiconductor wafer 50 includes a plurality of semiconductor substrates 52, such as semiconductor dice, containing semiconductor devices and integrated circuits. The semiconductor wafer 50, and each of the semiconductor substrates 52 as well, include a circuit side 54 wherein the semiconductor devices and integrated circuits are located, and a back side 56. In addition, each semiconductor substrate 52 includes a plurality of conductive vias 58 extending from circuit side 54 to the back side 56 thereof. The conductive vias 58 are in electrical communication with the semiconductor devices and integrated circuits in the semiconductor substrate 52.

[0029] As shown in Figure 3A, each conductive via 58 comprises a through, generally circular via 60 in the semiconductor substrate 52 lined with a via insulator 62 and filled with a conductive metal. The conductive metal can comprise a highly conductive metal such as copper, nickel, gold, aluminum, titanium, iridium, tungsten, silver, platinum, palladium, tantalum, molybdenum, zinc, tin, solder and alloys of these metals. The via insulator 62 can comprise an electrically insulating material such as a polymer (e.g., polyimide) or SiO_2. As also shown in Figure 3A, each semiconductor substrate 52 also includes a plurality of circuit side redistribution conductors 66 on the circuit side 54 in electrical communication with the conductive vias 58. The circuit side redistribution conductors 66 are insulated from the semiconductor substrate 52 by an inner dielectric layer 64, and are covered by an outer dielectric layer 68.

[0030] All of the elements described so far including the semiconductor substrate 52 with semiconductor devices and integrated circuits therein, the conductive vias 58, the circuit side redistribution conductors 66, and the dielectric layers 64, 68 can be formed using well known semiconductor fabrication processes. For example, the conductive vias 58 can be formed by etching or laser machining the vias 60 through the substrate 52, forming the via insulators 62 in the vias using a

process such as polymer deposition or oxide growth, and then depositing a metal in the vias using a process such as electrolytic deposition, electroless deposition, CVD, stenciling, or screen printing. Another method for forming the conductive vias 58 is to form the vias 60 part way though the substrate 52, filling the vias 60 with the conductive metal, and then thinning the substrate 52 using a process such as etching or sawing to expose the conductive metal.

[0031] The wafer 50 is attached to a wafer carrier 70 using a carrier adhesive 72, such as a double sided tape, which can be de-bonded using UV radiation. The wafer carrier 70 permits back side fabrication processes, such as back side thinning, to be performed. Thinning can be performed using a mechanical planarization apparatus, such as a grinder, or a chemical mechanical planarization (CMP) apparatus, to form a thinned back side 56T. Following back side thinning, the wafer 50 can have a thickness of from about 100 μm to about 725 μm. The wafer carrier 70 also allows other back side processes to be performed, such as the formation of back side elements (e.g., terminal contacts).

[0032] Next, as shown in Figures 3B and 4A, a removing step is performed to remove portions of the back side 56 of the substrate 52, and expose terminal portions 76 (Figure 4A) of the conductive vias 58. The removing step can be performed using a wet etching process, a dry etching process, or a plasma etching process, such as reactive ion etching (REI). For example, for etching a semiconductor substrate 52 made of silicon, a wet etching process can be performed using a solution of tetramethyl ammonium hydroxide (TMAH), or alternately a solution of potassium hydroxide (KOH). As shown in Figure 4A, the removing step can be performed to remove about 5-10 μm of the semiconductor substrate 52, leaving the exposed terminal portions 76 of the conductive vias 58 with a height X from the thinned back side 56T of from 5-10 μm.

[0033] Next, as shown in Figures 3C and 4B, a polymer deposition step is performed to form a polymer layer 78 which covers the thinned back side 56T of the semiconductor substrate 52, and encapsulates the exposed terminal portions 76 of the conductive vias 58. The polymer layer 78 can comprise a curable polymer such as silicone, polyimide or epoxy. In addition, the polymer layer 78 can include fillers, such as silicates, for adjusting the coefficient of thermal expansion (CTE), and the viscosity of the polymer material. The polymer layer 78 can be deposited on the

thinned back side 56T using a suitable process such as spin coating, nozzle deposition, screen printing, stenciling or lithography. For example, with spin coating, a spin on polymer can be applied to the thinned back side 56T of the semiconductor wafer 50, which is then spun rapidly using a spin coater to drive off liquids. Following spin coating the polymer material can be cured. The thickness of the resulting deposited material depends on the viscosity of the solution and the spin speed. This thickness is selected to encapsulate the terminal portions 76 (Figure 4A) of the conductive vias 58. By way of example, the polymer layer 78 can have a thickness of from 10-25 μm.

[0034] Next, as shown in Figures 3D and 4C, a planarization step is performed to form planarized contactors 74 on the conductive vias 58. The planarization step also planarizes the polymer layer 78 and forms a planarized polymer surface 80. The planarization step can be performed using chemical mechanical planarization (CMP). For example, suitable CMP apparatus are commercially available from manufacturers such as Westech, SEZ, Plasma Polishing Systems, or TRUSI. The planarization step can also be performed by mechanical planarization using a grinder, or by fly cutting using a surface planar unit, such as a DISCO fully automatic surface planar unit. The planarization step can be control to endpoint at the surface of the conductive via 58, or to remove a small amount of the conductive via 58. A representative thickness of the polymer layer 78 following the planarization step can be from 5-10μm.

[0035] Next, as shown in Figures 3E and 4D, a metallization step is performed to form under bump metallization layers (UBM) 82, 84 on the planarized contactors 74 of the conductive vias 58. The under bump metallization layers (UBM) 82, 84 can be formed using a deposition or plating process, such as electroless deposition, electrolytic deposition or CVD. The under bump metallization (UBM) layers 82, 84 can comprise one or more layers configured to provide surfaces for forming or bonding terminal contacts 86 (Figure 5A). For example, the under bump metallization (UBM) layer 82 can comprise an adhesion layer formed of a metal such as nickel, zinc, chromium, or palladium. The under bump metallization layer 84 can comprise a solder wettable metal layer formed of a metal such as tin, palladium or gold.

[0036] The present method for fabricating semiconductor components (Figures 3A-3E) eliminates the photo mask 38 (Figure 1C) of the prior art method (Figures 1A-1E). In addition, the present method (Figures 3A-3E) eliminates alignment of the mask 38 (Figure 1C) to the conductive vias 14, and eliminates the formation of conductors 34 (Figure 1E). With the present method (Figures 3A-3E), the terminal portions 76 (Figure 4A) of the conductive vias 58 form conductors, which are self aligned to the conductive vias 58. This allows the conductive vias 58 to have an OD of about 10 μm or less. In addition, there is no possibility of forming a short circuit 44 (Figure 2D) or of forming an open circuit (Figure 2E). In this regard, the polymer layer 78 provides additional electrical insulation between the terminal portion 76 (Figure 4A) and the semiconductor substrate 52, such that shorting cannot occur.

[0037] Referring to Figures 5A and 5B, additional back side processes can be performed to form back side elements in electrical communication with the conductive vias 58. For example, as shown in Figure 5A, terminal contacts 86 can be formed on the under bump metallization layers 82, 84. The terminal contacts 86 can comprise solder, another metal or a conductive polymer, formed using a suitable deposition process, such as stenciling and reflow of a solder alloy onto the under bump metallization layers 82, 84. As shown in Figure 5B, back side redistribution conductors 88 can also be formed on the planarized surface 80 of the polymer layer 78 in electrical communication with the conductive vias 58. The back side redistribution conductors 88 can be formed using a suitable process such as electroless deposition through a mask, or by patterning a deposited layer of metal. In addition, terminal contacts 86 can be formed on the back side redistribution conductors 88, substantially as previously described.

[0038] Following the back side processing step, the semiconductor wafer 50 can be diced to form a plurality of chip scale semiconductor components 90 (Figure 6). Dicing can be accomplished using a process such as lasering, sawing, water jetting or etching. Following the dicing step, the semiconductor components 90 (Figure 6) can be removed from the carrier 70.

[0039] As shown in Figures 6A-6C, each semiconductor component 90 includes a semiconductor substrate 52 having a plurality of conductive vias 58. Each conductive via 58 includes a terminal portion 76 which forms a self aligned back side

conductor, which is substantially equivalent to a prior art back side conductor 34 (Figure 1E). In addition, the semiconductor component 90 includes a back side polymer layer 78 encapsulating the terminal portions 76 of the conductive vias 58, and terminal contacts 86 in electrical communication with the conductive vias 58. The semiconductor component 90 also includes an inner dielectric layer 64, circuit side redistribution conductors 66 in electrical communication with the conductive vias 58, and a circuit side outer dielectric layer 68. The outer dielectric layer 68 can include openings 92 (Figure 6C) which align with the conductive vias 58 (or alternately with contacts in electrical communication with the conductive vias 58), which permit stacking of multiple semiconductor components 90.

[0040] Referring to Figure 7, a stacked semiconductor component 96 includes a plurality of the semiconductor components 90 in a stacked array including an upper component 90-1, a middle component 90-2 and a lower component 90-3, mounted to a module substrate 94. The terminal contacts 86 on the upper component 90-1 can be bonded to the conductive vias 58 on the middle component 90-2, and the terminal contacts 86 on the middle component 90-2 can be bonded to the conductive vias 58 on the lower component 90-3. In addition, the terminal contacts 86 on the lower component 90-3 can be bonded to electrodes on the module substrate 94. Further, underfill layers 98 can be formed between the components 90-1, 90-2, 90-3 and the module substrate 94. The alignment of the conductive vias 58 on the components 90-1, 90-2, 90-3 facilitates the fabrication of the stacked component 56.

[0041] While a number of exemplary aspects and embodiments have been discussed above, those of skill in the art will recognize certain modifications, permutations, additions and subcombinations thereof. It is therefore intended that the following appended claims and claims hereafter introduced are interpreted to include all such modifications, permutations, additions and sub-combinations as are within their true spirit and scope.

WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor component comprising:

providing a semiconductor substrate having a circuit side, a back side and a plurality of conductive vias comprising vias extending from the circuit side to the back side, an electrically insulating layer lining the vias and a metal in the vias;

forming a plurality of circuit side conductors on the circuit side in electrical contact with the conductive vias;

forming an outer dielectric layer on the circuit side having openings aligned with the conductive vias;

removing portions of the semiconductor substrate from the back side to expose terminal portions and surfaces of the conductive vias extending from the back side with a height X;

depositing a polymer layer on the back side encapsulating the terminal portions and the surfaces of the terminal portions with the polymer layer having a thickness equal to or greater than the height X;

planarizing the polymer layer, the terminal portions and the surfaces of the terminal portions to form self aligned conductors comprising the metal embedded in the polymer layer, a planarized polymer surface and planarized contactors on the conductive vias, with the planarizing step controlled to endpoint at the surfaces of the terminal portions; and

forming a plurality of terminal contacts on the planarized contactors,

2. The method of claim 1 further comprising thinning the semiconductor substrate during the planarizing step.

3. The method of claim 1 wherein the forming the terminal contacts step comprises forming under bump metallization layers on the planarized contactors.

4. The method of claim 1 wherein the planarizing step comprises chemical mechanical planarization (CMP) or grinding.

5. The method of claim 1 further comprising prior to the forming the circuit side conductors step forming a dielectric layer on the circuit side and forming the circuit side conductors on the dielectric layer.

6. A method for fabricating a semiconductor component comprising:

providing a semiconductor substrate having a circuit side, a back side and a plurality of conductive vias comprising through vias in the semiconductor substrate from the circuit side to the back side, an electrically insulating layer lining the vias and a metal in the vias;

etching the semiconductor substrate from the back side to expose terminal portions and surfaces of the conductive vias extending from the back side with a height X;

depositing a polymer layer on the back side encapsulating the terminal portions and the surfaces of the terminal portions with the polymer layer having a thickness equal to or greater than the height X;

planarizing the polymer layer to form a planarized polymer surface and the surfaces of the terminal portions of the conductive vias to form self aligned conductors comprising the metal embedded in the polymer layer and planarized contactors formed by the surfaces of the terminal portions;

controlling the planarizing step to end point at the surfaces of the terminal portions; and

forming a plurality of redistribution conductors on the planarized polymer surface in electrical contact with the planarized contactors.

7. The method of claim 6 further comprising forming a plurality of metallization layers on the redistribution conductors and forming terminal contacts on the metallization layers.

8. The method of claim 6 further comprising forming a plurality of terminal contacts on the redistribution conductors.

9. The method of claim 6 further comprising thinning the semiconductor substrate from the back side prior to the etching step.

10. The method of claim 6 wherein the depositing step is performed using a spin on process.

11. The method of claim 6 wherein the providing step provides the semiconductor substrate on a semiconductor wafer attached to a wafer carrier, and the etching, depositing and planarizing steps are performed on the semiconductor wafer attached to the carrier.

12. The method of claim 6 wherein the etching step removes from about 5-10 μm of the semiconductor substrate and the depositing step forms the polymer layer with a thickness on the back side of from 10-25μm.

13. The method of claim 6 wherein the height X of the terminal portions on the back side is about 5-10 μm and the depositing step forms the polymer layer with a thickness on the back side of from 10-25μm.

14. A method for fabricating semiconductor components comprising:

providing a semiconductor wafer comprising a circuit side, a back side, and a plurality of semiconductor substrates having a plurality of integrated circuits;

forming a plurality of conductive vias through the semiconductor substrates from the circuit side to the back side in electrical communication with the integrated circuits, each conductive via comprising a via, an insulating layer in the via and a metal filling the via;

forming a circuit side dielectric layer on the circuit side and a plurality of circuit side conductors on the circuit side dielectric layer in electrical contact with the conductive vias;

forming an outer dielectric layer on the circuit side having openings aligned with the conductivc vias;

removing portions of the back side to expose terminal portions and surfaces of the conductive vias having a height X on the back side;

depositing a polymer layer on the back side encapsulating the terminal portions with the polymer layer having a thickness equal to or greater than the height X;

planarizing the polymer layer to form a planarized polymer surface and the surfaces of the terminal portions to form self aligned conductors embedded in the polymer layer having planarized contactors formed by the surfaces of the terminal portions;

controlling the planarizing step to end point at the surfaces of the terminal portions;

forming a plurality of redistribution conductors on the planarized polymer surface in electrical contact with the planarized contactors; and

dicing the semiconductor wafer to separate the semiconductor substrates.

15. The method of claim 14 wherein the removing step comprises etching.

16. The method of claim 14 further comprising thinning the semiconductor wafer from the back side prior to the removing step.

17. The method of claim 14 wherein the depositing the polymer layer step comprises spin coating.

18. The method of claim 14 further comprising forming a plurality of back side elements on the polymer layer in electrical communication with the redistribution conductors.

19. The method of claim 14 further comprising forming under bump metallization layers on the redistribution conductors and terminal contacts on the under bump metallization layers.

20. The method of claim 14 further comprising forming a plurality of terminal contacts on the redistribution conductors.

21. A semiconductor component comprising:

a semiconductor substrate having a circuit side and a back side;

a plurality of conductive vias in the substrate, each conductive via comprising a via, an insulating layer in the via and a metal filling the via;

a polymer layer on the back side; and

a plurality of back side conductors comprising terminal portions of the conductive vias embedded in the polymer layer.

22. The semiconductor component of claim 21 wherein the conductors comprise planarized contactors.

23. The semiconductor component of claim 21 further comprising a plurality of terminal contacts on the conductors.

24. The semiconductor component of claim 21 further comprising a plurality of back side redistribution conductors on the polymer layer in electrical contact with the terminal portions.

25. The semiconductor component of claim 21 wherein the terminal portions have a height of from 5-10 μm.

26. A stacked semiconductor component comprising:

a plurality of semiconductor components in a stacked array, each component comprising:

a semiconductor substrate having a circuit side and a back side;

a plurality of conductive vias in the substrate, each conductive via comprising a via, an insulating layer in the via and a metal filling the via;

a polymer layer on the back side; and

a plurality of back side conductors comprising terminal portions of the conductive vias embedded in the polymer layer;

the components stacked back side to circuit side with the conductive vias in alignment.

27. The stacked component of claim 26 wherein each component comprises a plurality of terminal contacts bonded to the conductive vias on the component and to the conductive vias on an adjacent component.

28. The stacked component of claim 26 wherein the conductors include planarized contactors and terminal contacts on the contactors.

29. The stacked component of claim 26 further comprising a module substrate supporting the stacked array.

30. The stacked component of claim 26 wherein the components include a first component and a second component having a plurality of terminal contacts bonded to the conductive vias on the first component.