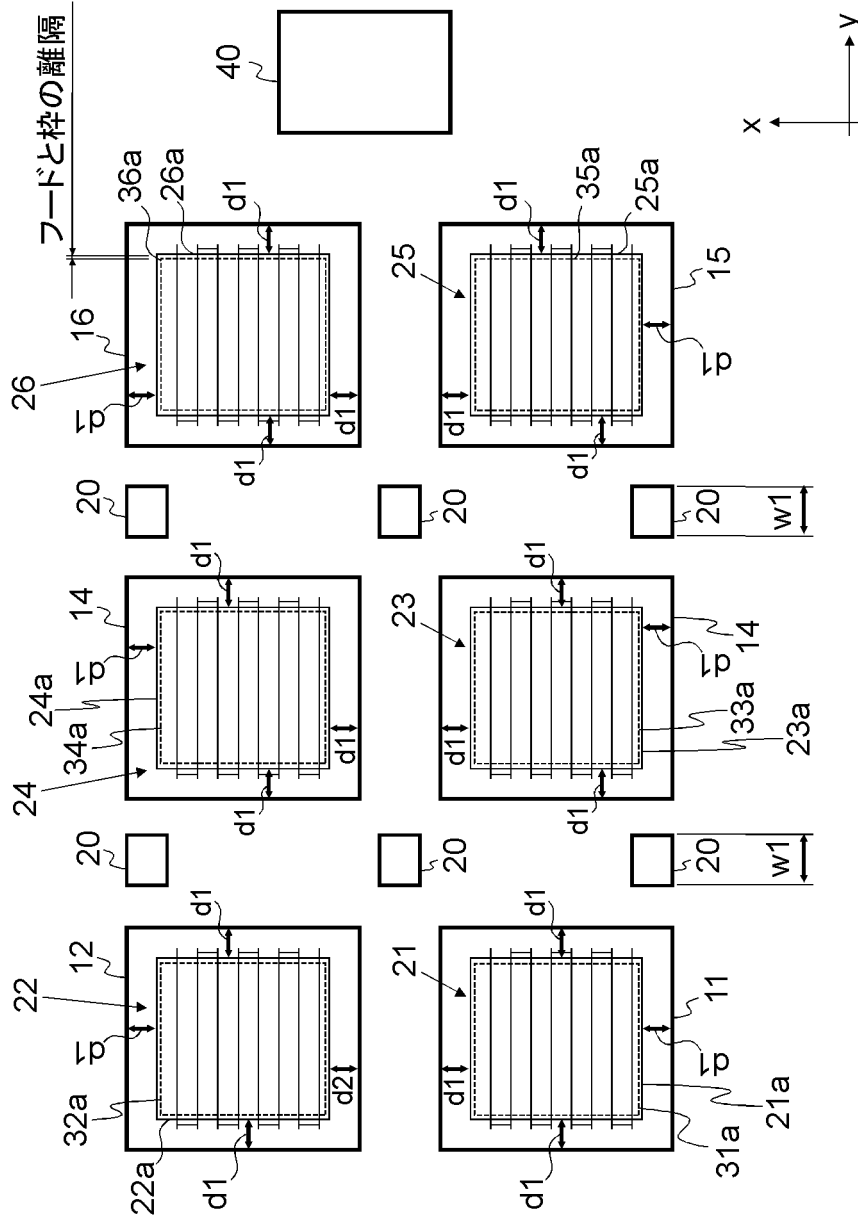
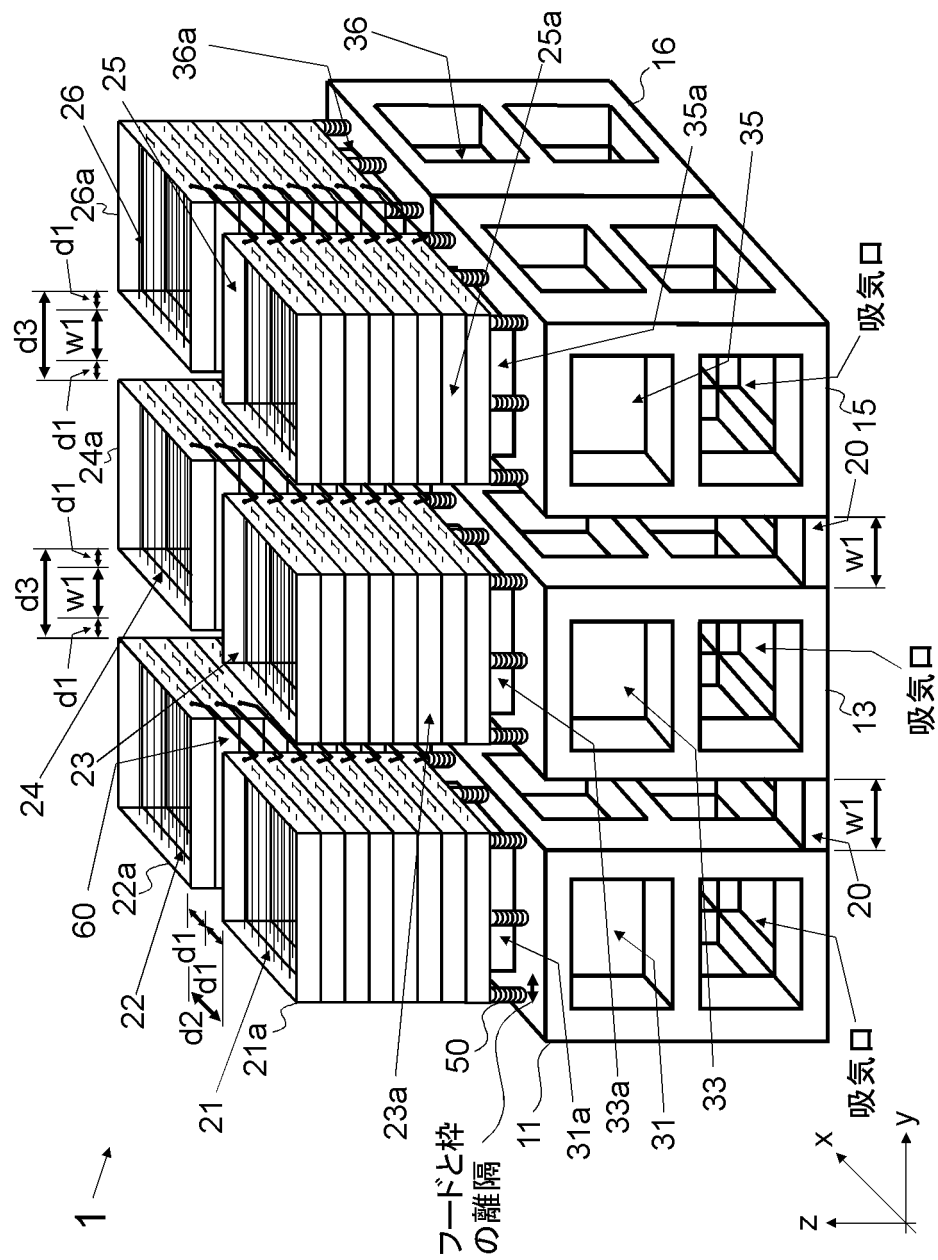


[図1]

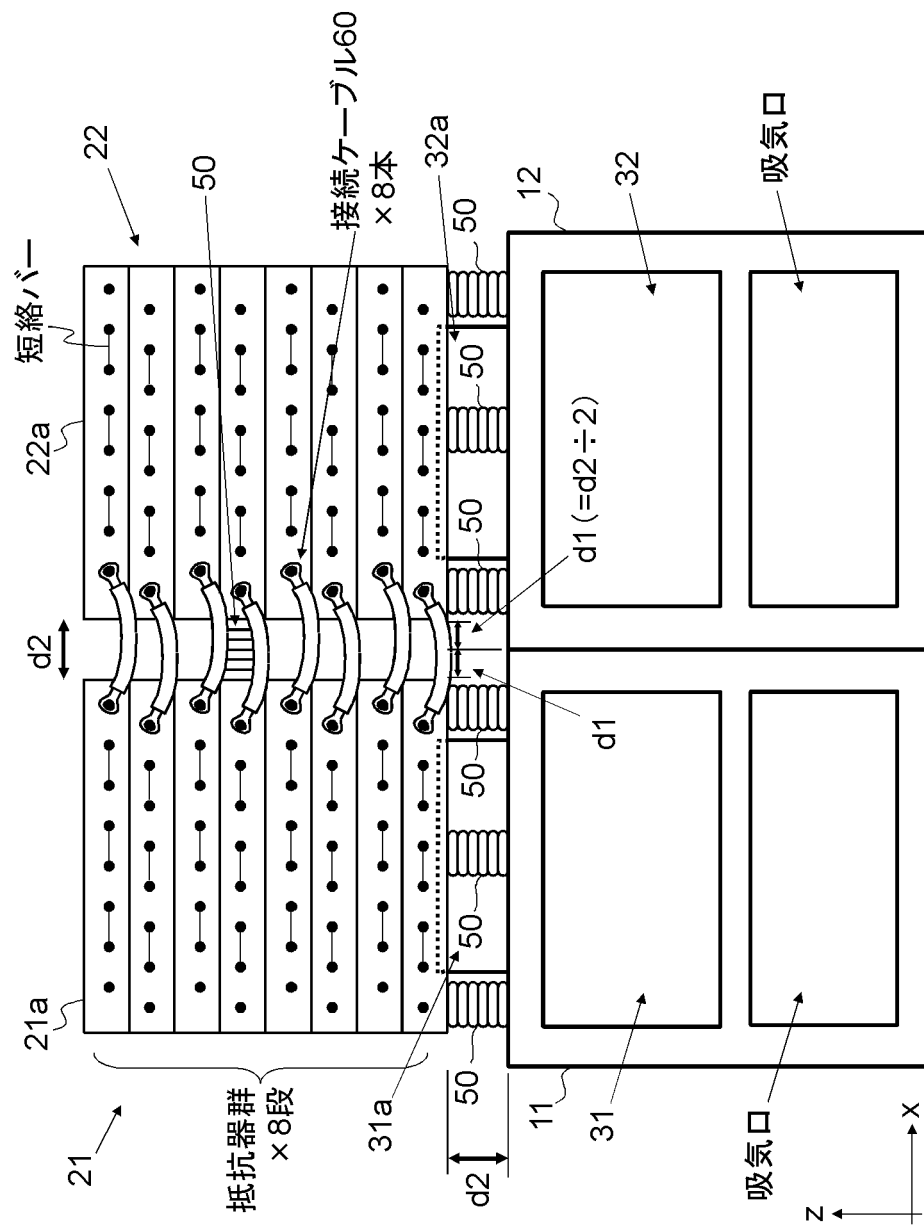


The diagram illustrates a plan view of a semiconductor device, labeled as 1. It shows a periodic arrangement of rectangular unit cells along the x-axis. Each unit cell contains a central channel region (30) flanked by source/drain regions (20). Above each unit cell is a gate electrode (10). The width of the source/drain regions is denoted as w_1 , the width of the channel regions as d_1 , and the distance between the centers of adjacent unit cells as d_3 . The device is divided into three main sections along the y-axis, labeled 11, 12, and 13. Each section contains a series of parallel horizontal lines representing the gate electrodes. The total width of the device is indicated as d_3 . A coordinate system with x and y axes is located at the top right corner.

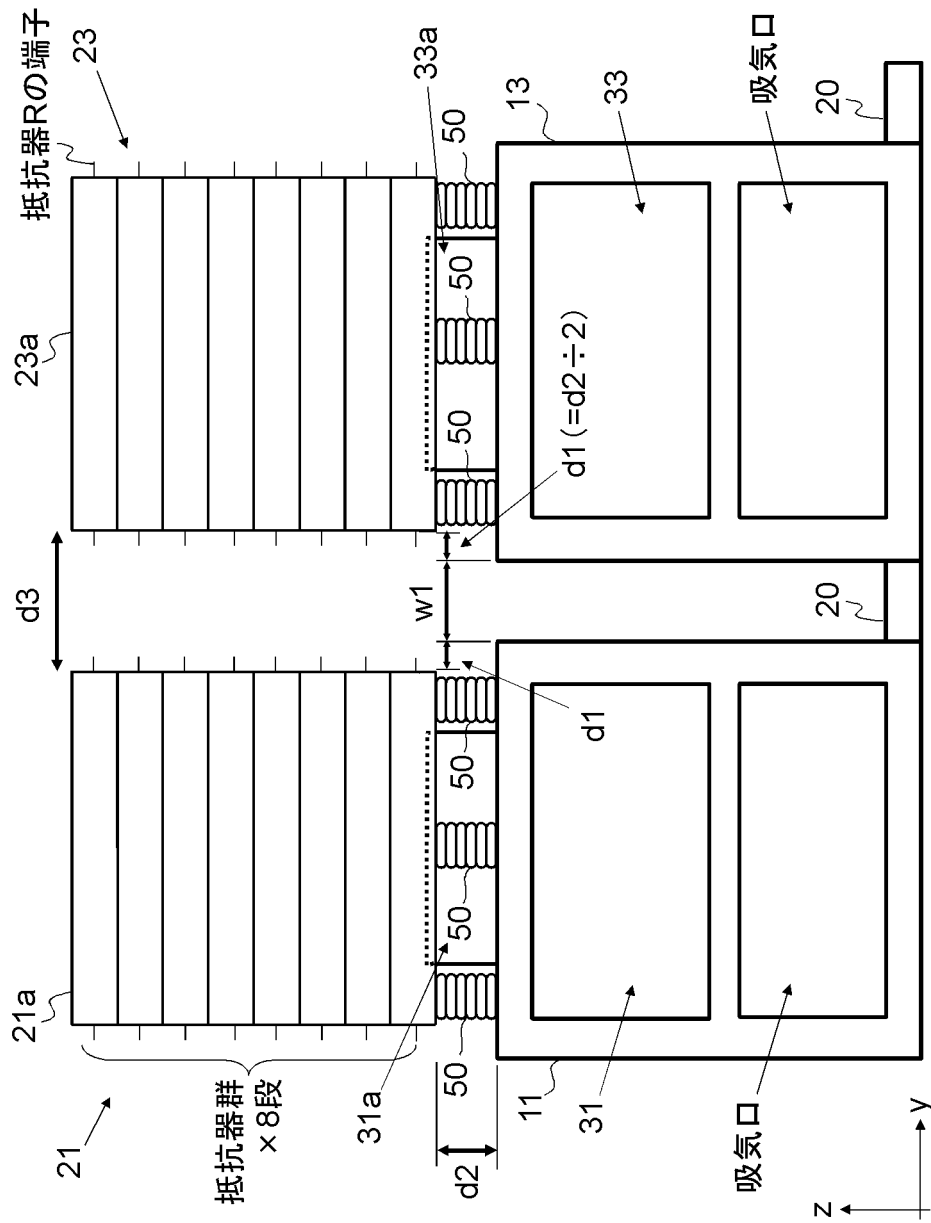
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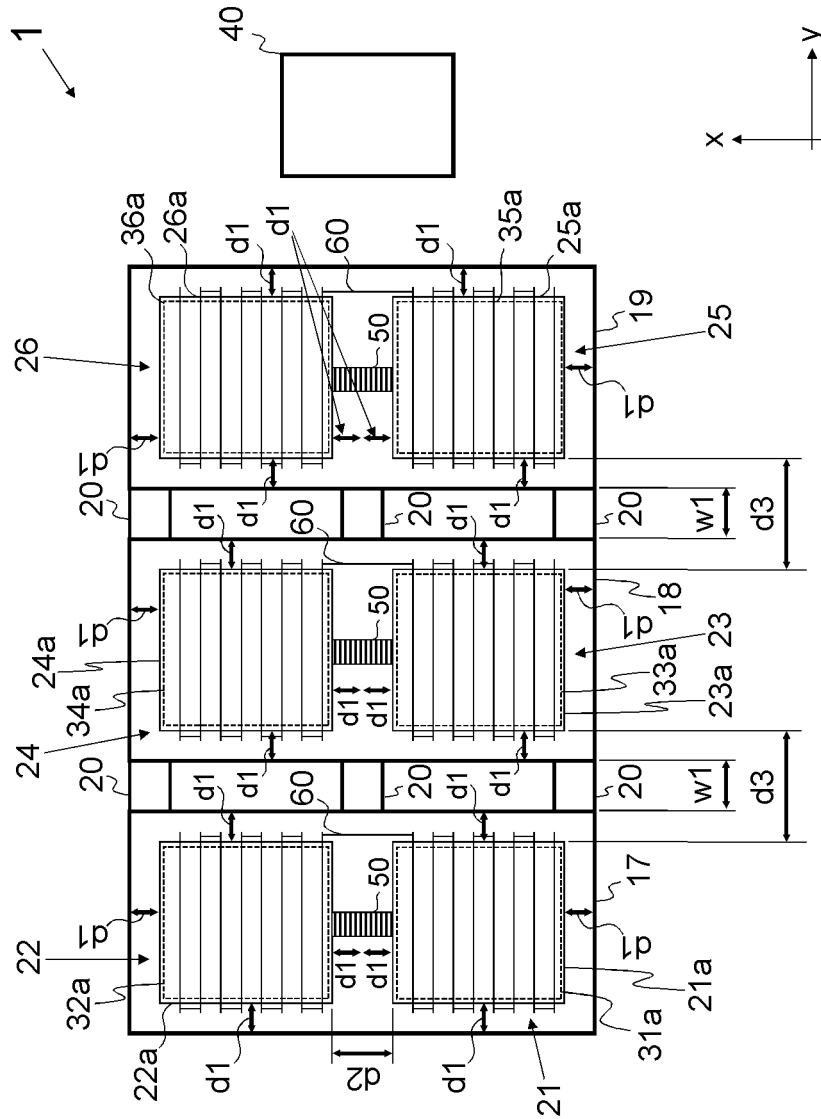
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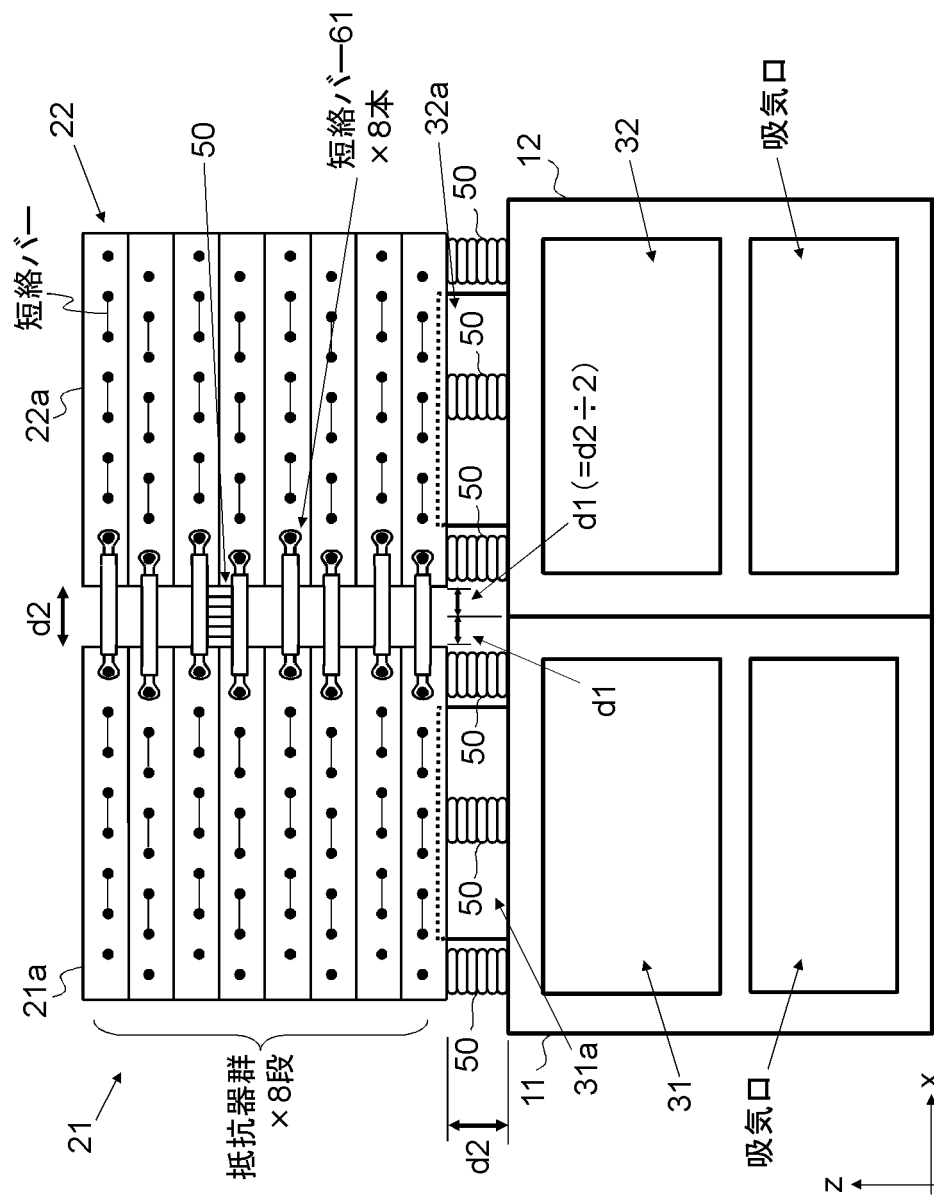
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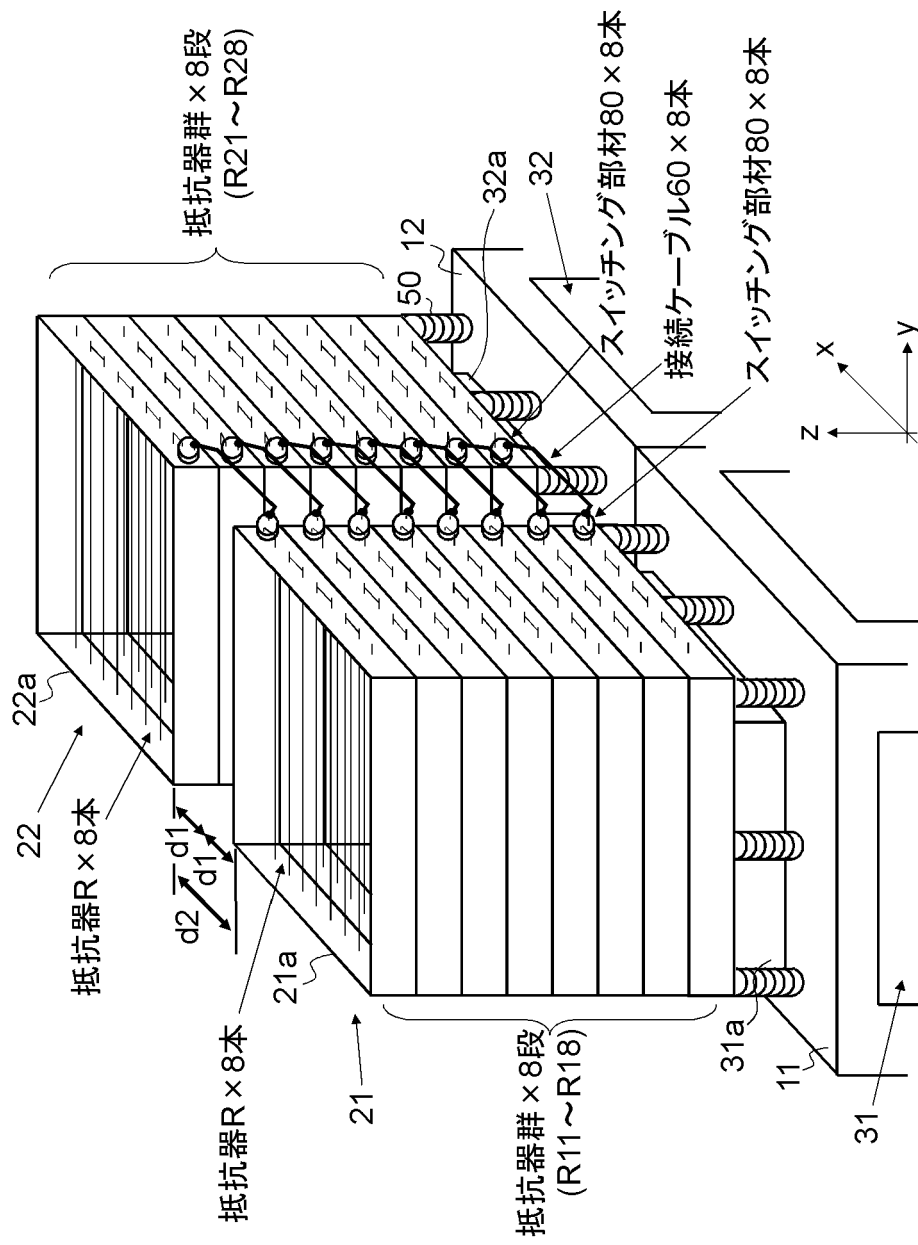
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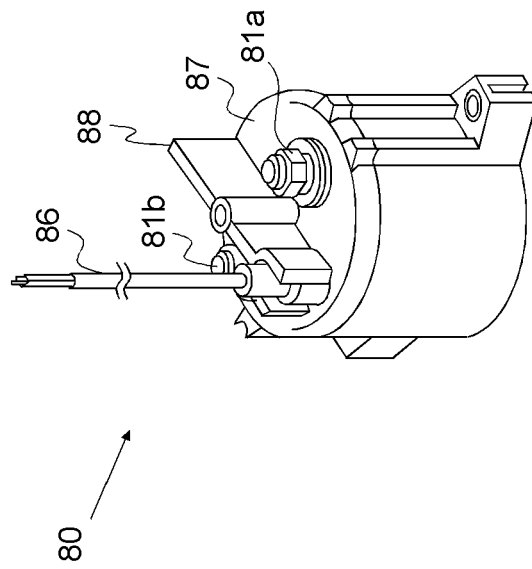
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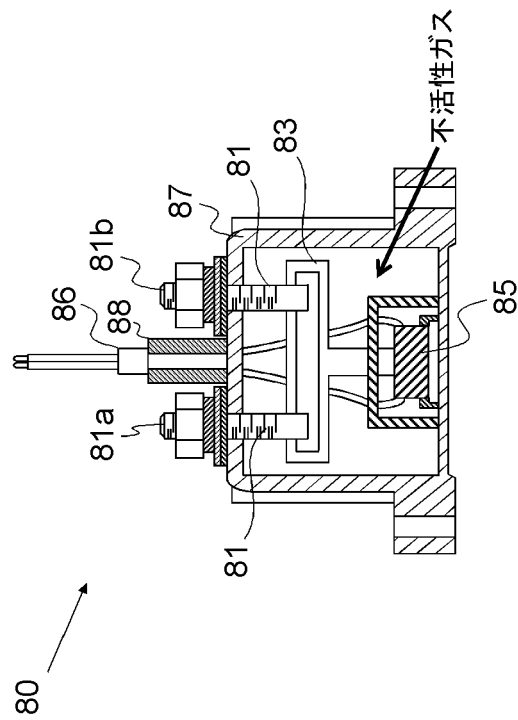
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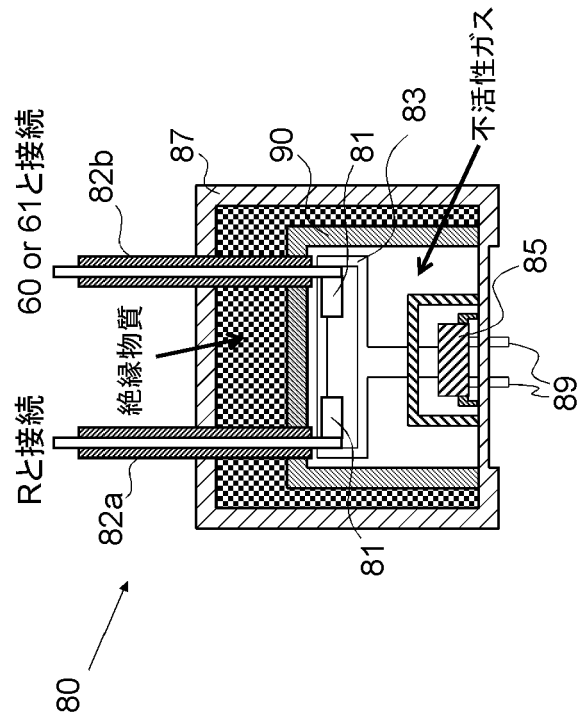
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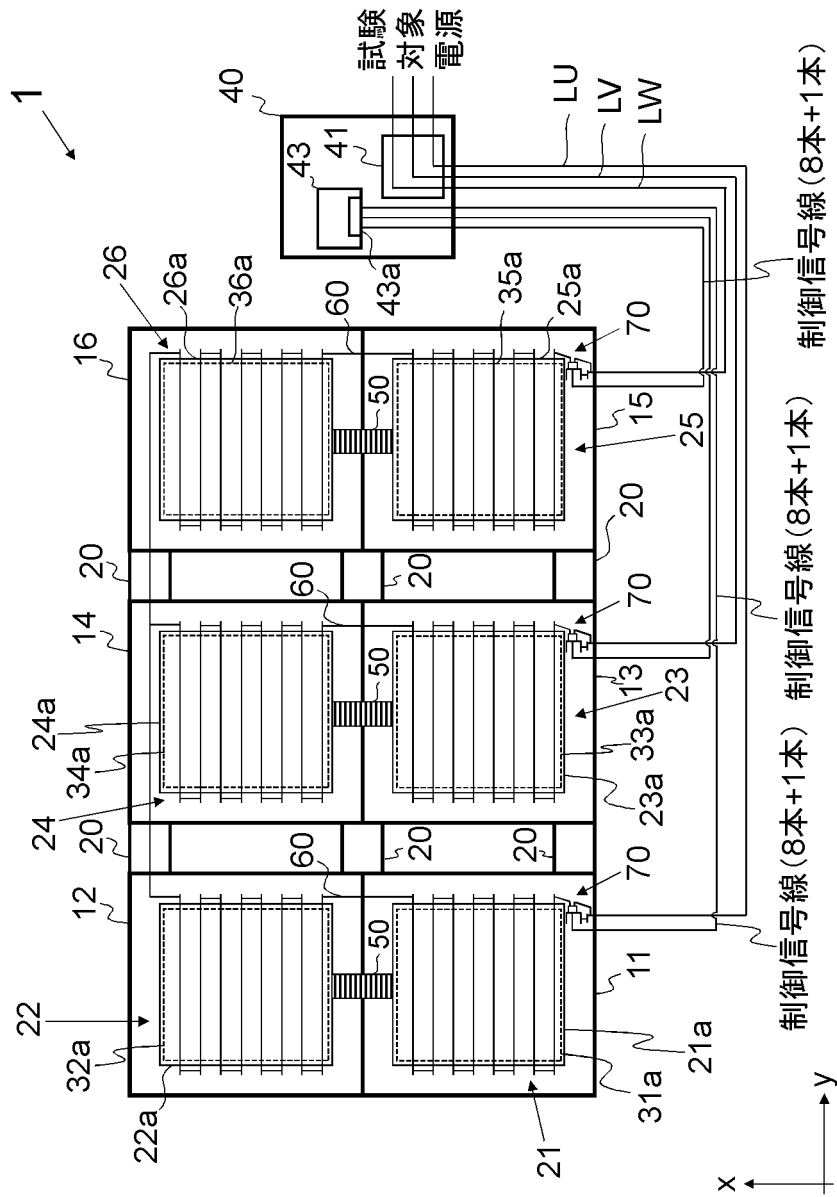
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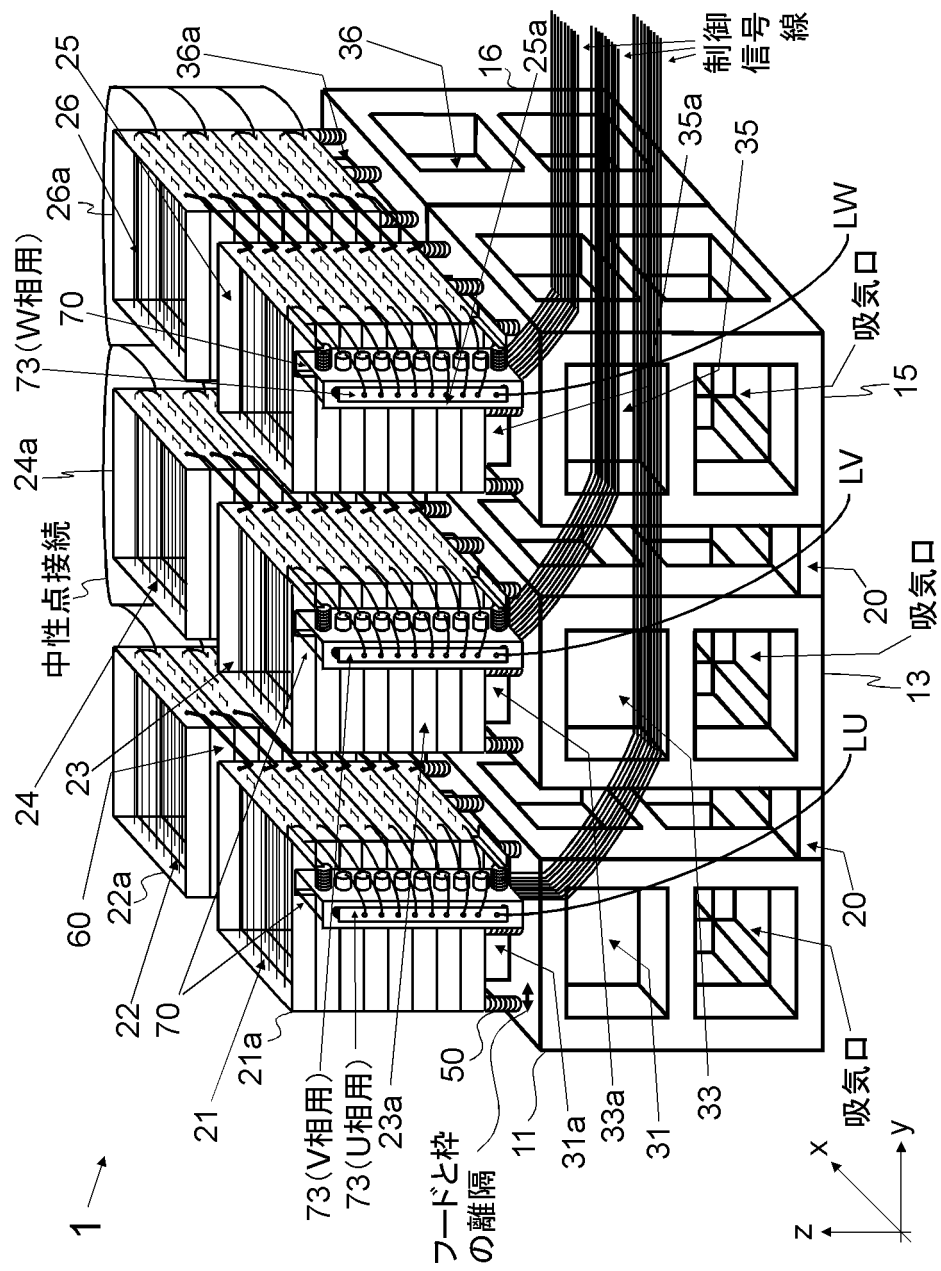
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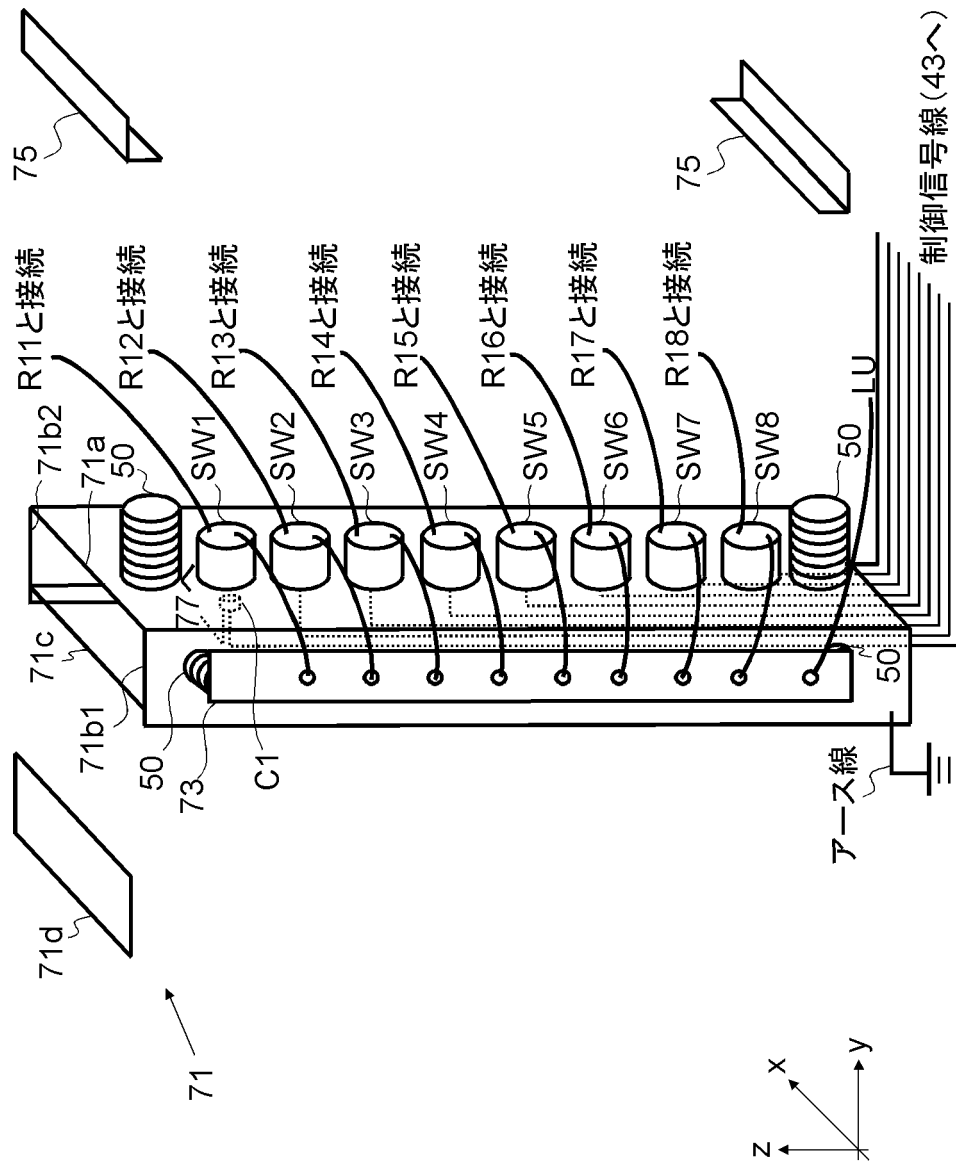
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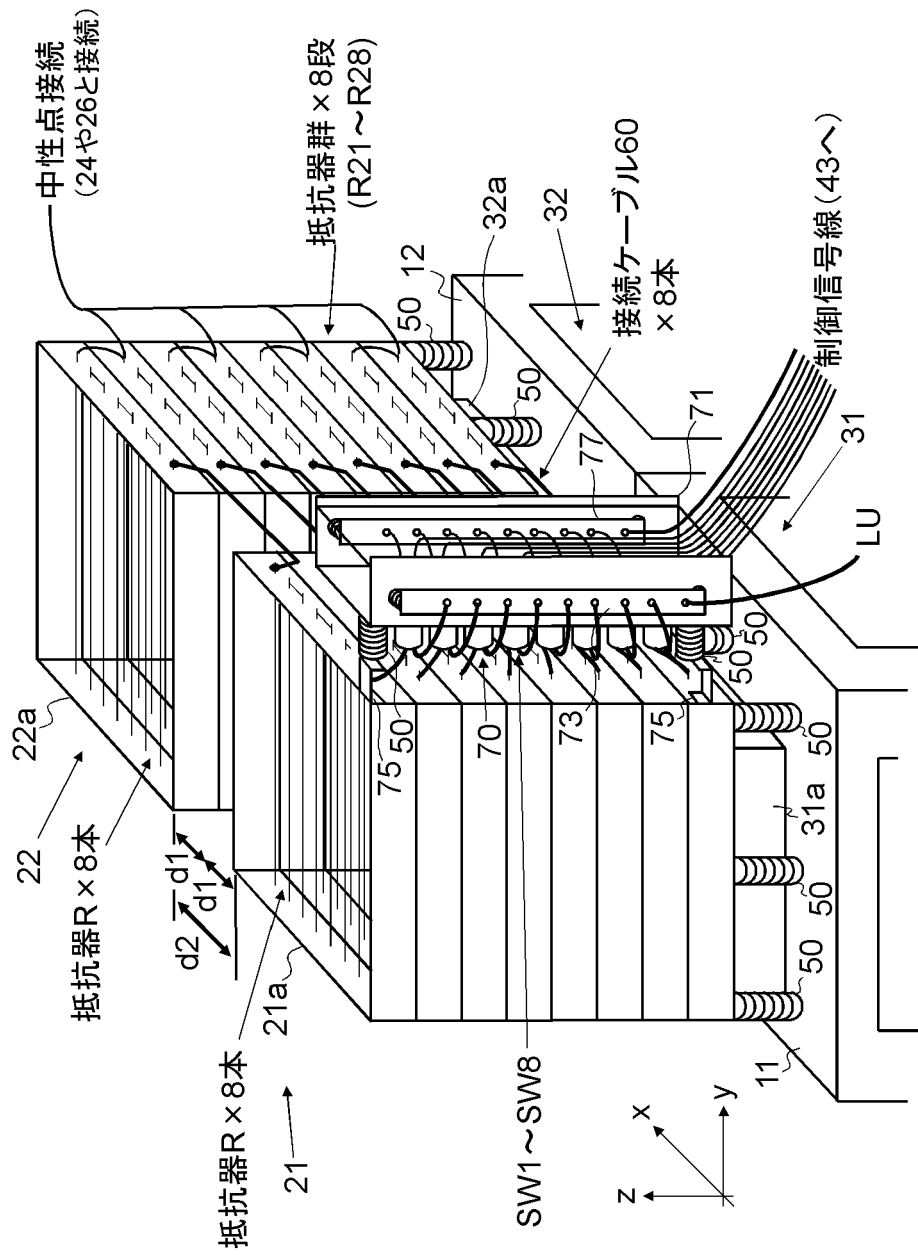
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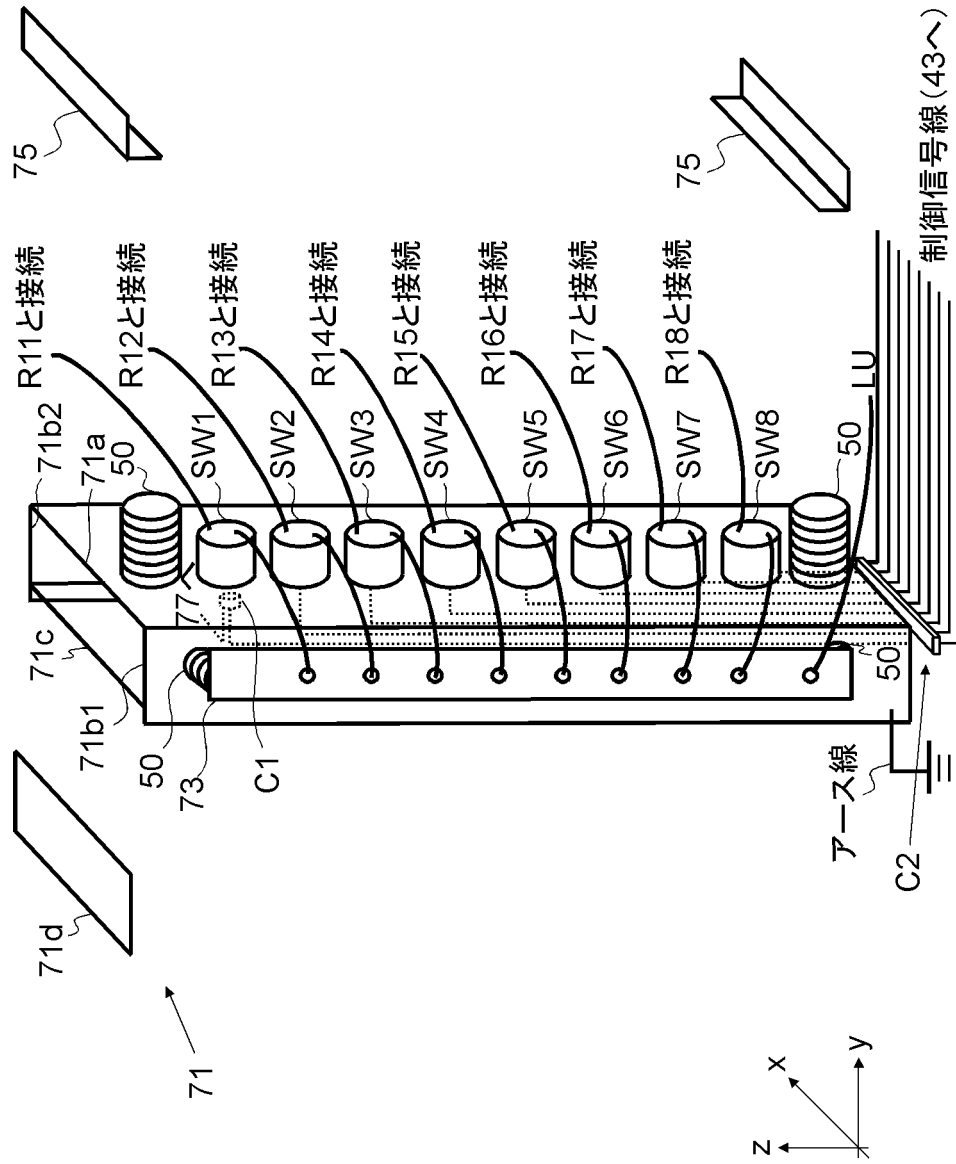
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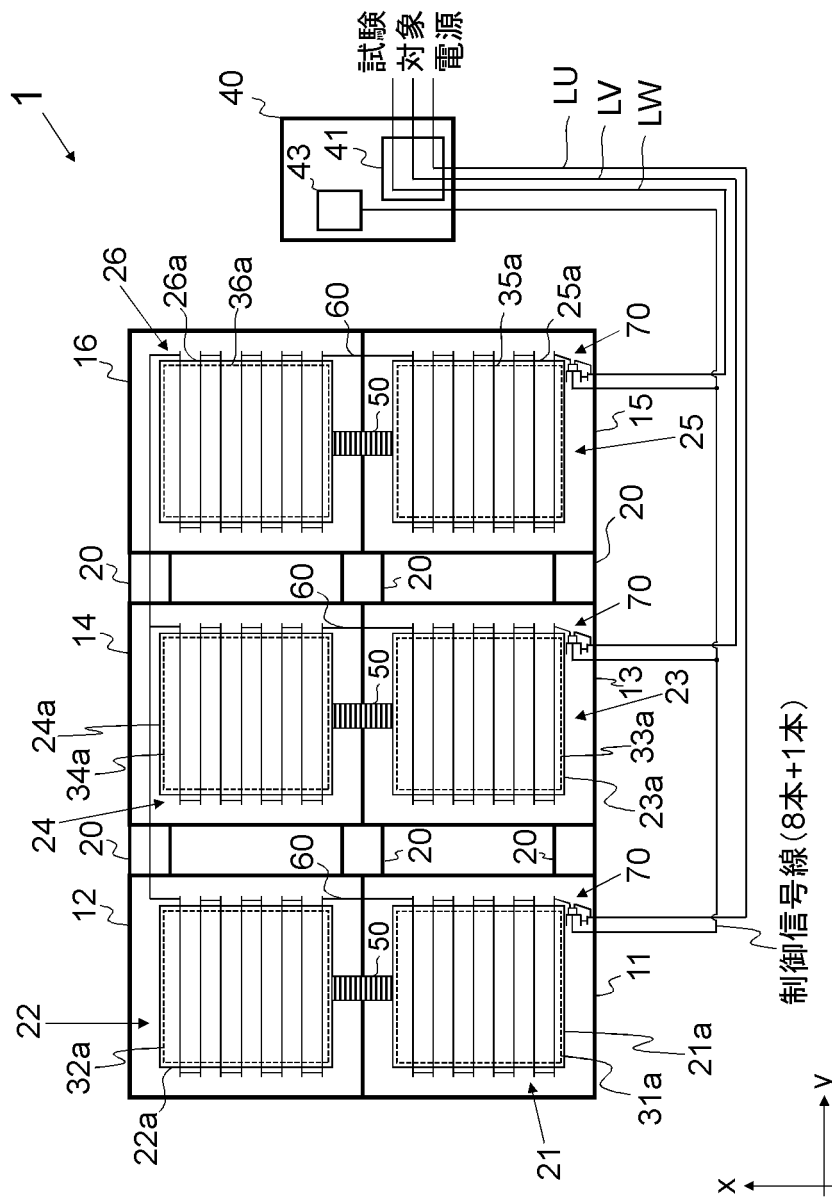
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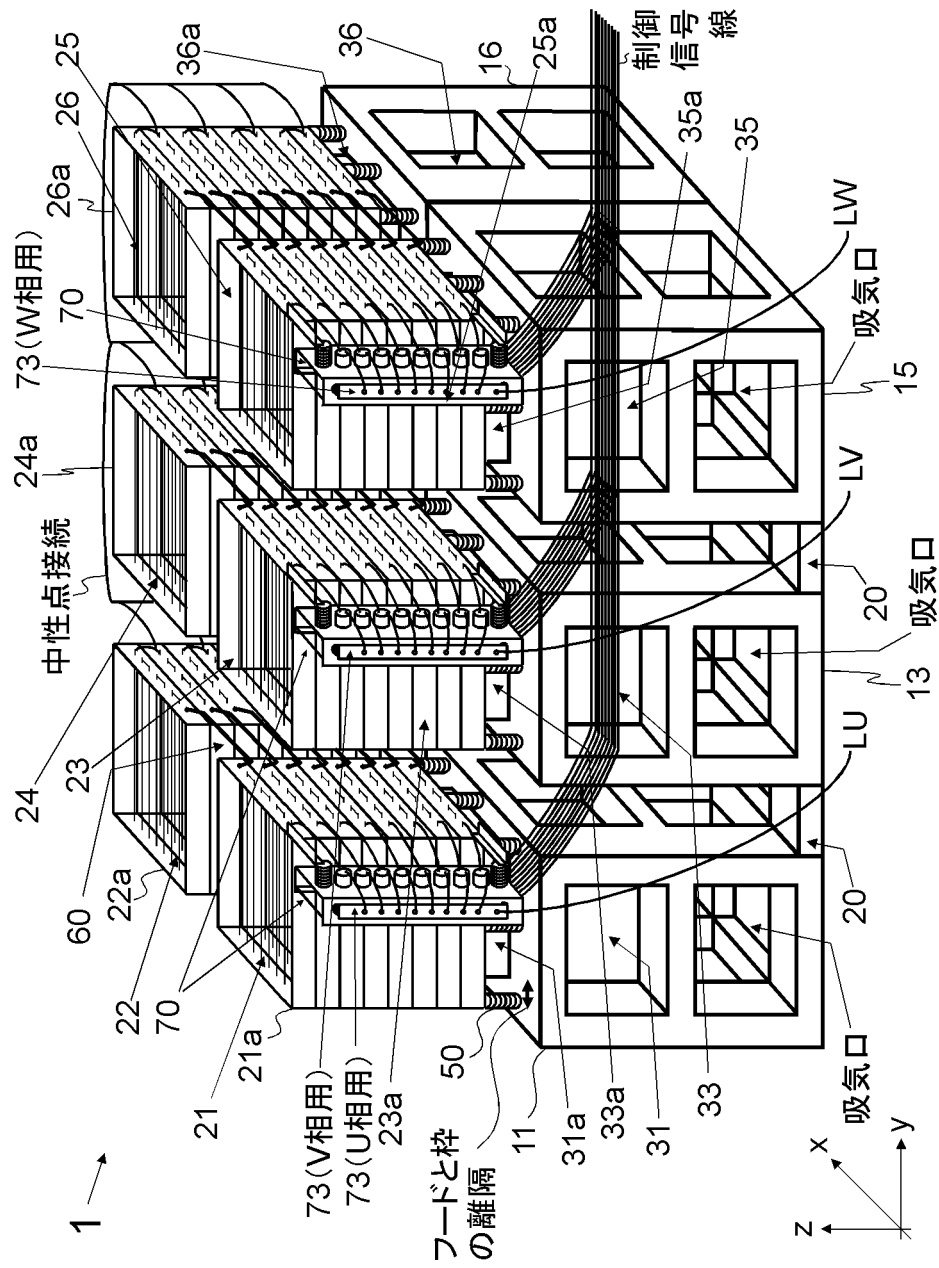
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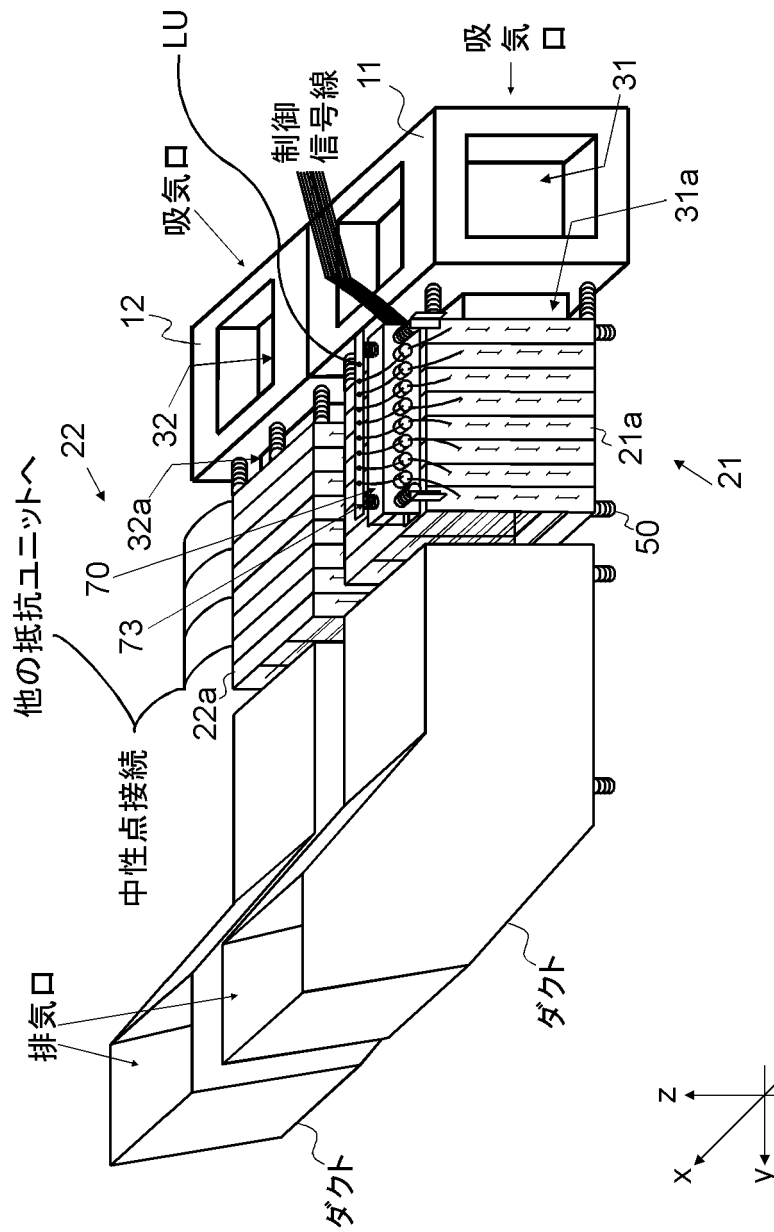
[図23]



[図24]



[図26]



[図27]

