

STRUCTURE FOR RADIOFREQUENCY APPLICATIONS

TECHNICAL FIELD OF THE INVENTION

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This invention relates to the field of integrated radio frequency devices.

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BACKGROUND OF THE INVENTION

For most applications involving the transmission or reception of radio frequency signals (10 MHz to 100 GHz), the devices require a substrate that fulfils increasingly
15 demanding specifications, particularly driven by the changing standards of mobile telephony (2G, 3G, LTE, LTE Advanced, LTE Advanced PRO, 5G ...). The properties of substrate materials must specifically ensure:

- Low insertion losses (low signal attenuation) and good
20 linearity (low signal distortion causing harmonics), typically by presenting an effective resistivity over a wide range of frequencies, greater than 1000 ohms/cm ;
- Stability of these temperature performances, particularly within the range of use of devices [-40°C;
25 150°C];
- Sufficient heat dissipation capacity, typically due to a thermal conductivity greater than 20 W/mK;
- A weak capacitive coupling between the active layer and the support substrate, typically thanks to a dielectric
30 permittivity equal to or lower than that of silicon ($\epsilon_{silicon} = 11$).

Moreover, in order to meet high volume requirements, the substrate must be compatible with the semiconductor

industry and particularly with CMOS silicon manufacturing lines. Of course, it must also have a competitive cost to be adopted by consumer applications, particularly in the field of telecommunications (telephony and cellular network, WiFi connectivity, Bluetooth). Space and military applications are particularly sensitive to performance and temperature resistance.

Radio frequency (RF) devices such as antenna switches and adaptors, power amplifiers, low noise amplifiers or even passive components (R, L, C) can be developed on different types of substrates.

For example, silicon-on-sapphire substrates known as SOS (silicon on sapphire) are known which allow the components produced using microelectronic technologies in the surface layer of silicon to benefit from the insulating properties of sapphire substrate materials, irrespective of temperature, its conductivity that is greater than 20 W/m.K and its permittivity that is less than 11. For example, the antenna switches and power amplifiers manufactured on this type of substrate exhibit very good factors of merit but are mainly used for niche applications because of the too high overall cost of the solution.

Also known are high-resistivity silicon substrates comprising a support substrate, a trapping layer (a few hundred nanometres to a few microns thick) laid out on the support substrate, a dielectric layer laid out on the trapping layer, and a semiconductor layer laid out on the dielectric layer. The support substrate usually has a resistivity greater than 1 kohm.cm . The trapping layer may comprise undoped polycrystalline silicon. The combination of a high resistivity silicon support substrate and a trapping layer, based on the state of the art, makes it possible to eliminate the parasitic conducting layer usually present under the oxide

layer buried in the SOI HR (Silicon on insulator with high resistivity silicon support substrate). The skilled person will find a review of the performance of RF devices manufactured on a high resistivity semiconductor substrate known in the Background of the Invention in "Silicon-on-insulator (SOI) Technology, Manufacture and Applications", points 10.7 and 10.8, Oleg Kononchuk and Bich-Yen Nguyen, Woodhead Publishing.

Nevertheless, a poly-silicon trapping layer has the disadvantage of undergoing partial recrystallization during high temperature heat treatment steps, which contributes to reducing the density of traps in the layer. The degradation of the RF device performance related to this decrease in the density of traps may be prohibitive for certain applications. Moreover, these substrates struggle to ensure the stability of the RF performances over the entire range of operating temperatures, particularly above 100°C. Their resistivity falls considering the generation of thermal carriers in the support substrate and the coupling device/substrate becomes a major contributor to signal attenuation and distortion. Performance degradation has also been observed when the temperature drops below 0°C. Finally, permittivity will remain very close to that of silicon (about 11).

Other support substrates, such as aluminum nitride or silicon carbide, would meet the RF properties specifications but are not compatible with the standard semiconductor industry. Their use as a support substrate for transferring the final layer of devices is conceivable. Nevertheless, the cost of these specific materials combined with that of the circuit transfer technologies is still too high for a mass adoption of these solutions.

PURPOSE OF THE INVENTION

Embodiments of the invention seek to provide a substrate suitable for radiofrequency applications, remedying all or part of the disadvantages of the prior art.

BRIEF DESCRIPTION OF THE INVENTION

10 An aspect of the disclosure provides a substrate for microelectronic radiofrequency devices comprising:
a support substrate comprising a first semiconductor material having a resistivity greater than 500 ohms.cm;
a plurality of trenches in the support substrate partially
15 filled with a second material and partially filled with a third material, the third material having a composition different than the second material., the plurality of trenches defining a plurality of first zones on a first side of the first semiconductor material and at least one
20 second zone of a second material, the second material having a resistivity greater than 10 kohms.cm, the plurality of first zones having a maximum lateral dimension of less than 10 microns, the plurality of first zones being isolated from one another by the at least one
25 second zone.

Another aspect of the disclosure provides a method for manufacturing a substrate for microelectronic radiofrequency devices, comprising:
30 providing a support substrate comprising a first semiconductor material having a resistivity greater than 500 ohms.cm, the support substrate having a first side;

etching, according to a mask, a plurality of trenches extending from the first side of the support substrate to a determined depth within the support substrate;

partially filling the plurality of trenches with a third material; and

filling remainders of the plurality of trenches with a second material to form first zones of a first material and at least one second zone on the first side of the second material, the first zones having a maximum lateral dimension of 10 microns or less, the first zones being insulated from one another by the second zone, the second material having a resistivity greater than 10 kohms.cm, the second material having a composition different than the third material.

Another aspect of the disclosure provides a method for manufacturing a substrate for microelectronic radiofrequency devices, comprising:

providing a support substrate comprising a first semiconductor

material having a resistivity greater than 500 ohms.cm; depositing, according to a mask, a plurality of pillars made from the first material and of a determined height, on the support substrate, an upper surface of the pillars defining a first side of the substrate, the pillars being insulated from each other by a plurality of trenches extending from the first side of the support substrate to a depth within the support substrate defined by the determined height of the pillars;

partially filling the plurality of trenches with a third material; and

filling remainders of the plurality of trenches with a second material to form first zones of the first material and at least one second zone on the first side of the second material, the first zones having a maximum lateral

dimension of 10 microns or less, the first zones being insulated from one another by the at least one second zone, the second material having a resistivity greater than 10 kohms.cm, the second material having a composition different than the third material.

An embodiment of the invention relates to a substrate for radiofrequency microelectronic devices comprising:

- A support substrate made of a first semiconductor material with a resistivity greater than 500 ohm.cm,
- A plurality of trenches in the support substrate, filled with a second material, and defining on a first side of the support substrate, a plurality of first zones of the first material and at least one second zone of the second material.

The substrate is remarkable in that:

- The second material has a resistivity greater than 10 kohms.cm;
- The first zones have a maximum dimension of less than 10 microns and are isolated from one another by the second zone.

The role of the upper part of the substrate according to the invention comprising the trenches filled with the second material is to block the movement of the movable charges which can be generated in the vicinity of the first side of the support substrate so that the latter maintains a high and stable resistivity level.

The restriction on the maximum dimension of the first zones and the insulation of these first zones from one another by at least one second zone made of a highly resistive

material, make it possible to block the movement of potential moving charges in the first zone semiconductor material constituting the support substrate, in the upper part. In this upper part, the charges have to travel a greater distance to pass from one first zone to another first neighbouring zone by bypassing the trenches filled with the second material. The effective resistivity of the substrate is thus increased.

This makes it possible to specifically eliminate the harmful effects of a parasitic conduction in a substrate on which RF devices are made.

According to advantageous features of embodiments of the invention, taken alone or in combination:

- The surface density of the first zones and of the second zone confers on an upper part of the substrate extending from the first side of the support substrate to a depth of the trenches an average thermal conductivity greater than 20 W/m.K, an average dielectric permittivity less than the permittivity of the first material and a resistivity higher than the resistivity of the first material;
- The second zone forms a mesh on the first side of the support substrate;
- The trench depth is between 1 micron and 100 microns;
- The first material constituting the support substrate is silicon;
- The second material filling the trenches is chosen from among a silicon oxide, a silicon nitride, a silicon oxynitride, an aluminium nitride, an amorphous or polycrystalline silicon, a carbon-rich silicon, a polymer or even a gas;

- The plurality of trenches is partially filled with the second material and partially with a third material of nature or composition different from the second material;
- The third material is chosen from among a silicon oxide, a silicon nitride, a silicon oxynitride, an aluminum nitride, an amorphous or polycrystalline silicon, a carbon-rich silicon, a polymer or even a gas;
- The second or the third material has the properties of trapping movable electrical charges that can be generated in the first material;
- The substrate comprises a dielectric layer laid out on the first side of the support substrate;
- The substrate comprises an additional layer between the dielectric layer and the first side of the support substrate, composed of the third material;
- The dielectric layer is made up of a material chosen from a silicon oxide, a silicon nitride, a silicon oxynitride, an aluminum nitride;
- The dielectric layer is composed of the second material;
- The substrate comprises a useful layer laid out on the first side of the support substrate;
- The dielectric layer is sandwiched between the useful layer and the first side of the support substrate;
- The useful layer is composed of a material chosen from semiconducting, insulating or conductive materials or piezoelectric materials.

Another embodiment of the invention relates to a structure of radiofrequency microelectronic devices comprising:

- A substrate such as above;
- A layer of microelectronic devices laid out on the substrate.

According to beneficial features of embodiments of the invention, taken alone or in combination, the microelectronic device is an antenna switch or adaptor or a power amplifier or a low noise amplifier or a passive component or a radiofrequency MEMS component or a radiofrequency filter or another circuit operating at high frequencies.

Another embodiment of the invention further relates to a substrate for radiofrequency microelectronic devices comprising:

- Providing a support substrate made of a first semiconductor material with a resistivity greater than 500 ohm.cm,
- Etching, according to a mask, of a plurality of trenches extending from the first side of the support substrate to a determined depth;
- Filling the plurality of trenches with a second material to form, on the first side, first areas of first material and at least one second zone of the second material;

The method is remarkable in that the first zones, whose maximum dimension is less than 10 microns, are insulated from one another by the second zone whose second material has a resistivity greater than 10 kohms.cm.

Another embodiment of the invention relates to a substrate for radiofrequency microelectronic devices comprising:

- Providing a support substrate made of a first semiconductor material with a resistivity greater than 500 ohms.cm;
- The local coating, according to a mask, of a plurality of pillars formed from the first material and of a given height, on the support substrate; an upper surface of the pillars defining a first side of the substrate and the pillars being insulated from each other by a plurality of trenches extending from the first side of the substrate

to a depth defined by the determined height of the pillars;

- Filling the plurality of trenches with a second material to form first areas of first material on the first side and at least one second zone of the second material.

The method is remarkable in that the first zones, whose maximum dimension is less than 10 microns, are insulated from one another by the second zone whose second material has a resistivity greater than 10 kohms.cm.

BRIEF DESCRIPTION OF THE DRAWINGS

Other characteristics and advantages of the invention will emerge from the detailed description of the invention which follows in the References to the accompanying drawings in which:

- Figs. 1a to 1d show steps of the method to manufacture a substrate according to the invention;
- Figs. 2 and 3 show two variants of substrates according to the invention, in plan view and in cross-section;
- Figs. 4a and 4b show other variants of substrates according to the invention, in sectional view;
- Figs. 5a, 5b, 6a to 6d, and 9 show substrates according to the invention;
- Figs. 7 and 8 show structures of radio-frequency microelectronic devices according to the invention;
- Fig. 10 shows a graph representing the effective resistivity of the substrate, depending on the operating frequency of radiofrequency microelectronic devices, in structures according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

In the descriptive part, the same references in the figures may be used for elements of the same type. The figures are schematic representations which, for the sake of clarity, are not to scale. In particular, the thicknesses of the layers along the Z axis are not to scale with respect to the lateral dimensions along the X and Y axis; and the relative thicknesses of the layers between them are not necessarily respected in the figures.

The invention relates to a method for producing a substrate suitable for radiofrequency microelectronic devices, shown in Figs. 1a to 1c. The method includes providing a support substrate 10 with a first semiconductor material 10' whose resistivity is greater than 500 ohms.cm (Fig. 1a). Advantageously, the resistivity of the first material will even be chosen to be greater than 1,000 ohms.cm, or even greater than 3,000 ohms.cm. As illustration, the first material 10' may be monocrystalline silicon.

According to the invention, the method also includes a phase of etching the first side 1 of the substrate 10, according to a mask, with a plurality of trenches 2 extending from the first side 1 of the support substrate 10 to a determined depth. This etching phase may be preceded by a photolithography phase conventionally implemented to define the patterns to be etched according to the said mask and to protect the patterns which are not to be etched by a masking layer. The etching may be carried out by known techniques of chemical etching, wet or dry. The masking layer deposited on the first side 1 of the support substrate 10 can then be removed, thus obtaining substrate 10 comprising the trenches 2, illustrated in Fig. 1b.

According to a variant, the trenches 2 may be produced by the local coating, according to a mask, of a plurality of pillars made up of the first material and of a given height on the support substrate 10. After coating, the upper surface of the pillars defines a first side of substrate 10 and the pillars are insulated from each other by a plurality of trenches extending from the said first side to a depth defined by the height of the pillars. Such local coating may, for example, be carried out by selective epitaxy: in this case, the areas to be free of coating are covered by a masking layer (in particular silicon oxide or nitride). The epitaxy then takes place locally, on the unmasked areas. After epitaxy, the masking layer present at the bottom of the trenches can be retained or removed by wet or dry etching.

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The manufacturing process further comprises a phase of filling the plurality of trenches 2 with a second material 20. The second material 20 will be chosen for its electrical properties: it will in particular have a resistivity greater than 10 kohms.cm. The second material 20 may be chosen from electrical insulators, such as silicon oxide, silicon nitride, a silicon oxynitride or aluminum nitride. It may alternatively be chosen from highly resistive semiconductors such as amorphous, polycrystalline, intrinsic silicon or with chosen compositions, for example, to stabilise the temperature resistivity (in particular if it is carbon-doped or carbon-rich silicon). Finally, the second material 20 may also be chosen from insulating polymers.

As illustration, the phase of filling the trenches 2 can be carried out by chemical, vapour or liquid coating or by heat treatment (for example by thermal oxidation in the case of filling with silicon oxide). Advantageously, the second material 20 can withstand high heat treatments (notably up to 1000°C or even 1200°C.) required for the subsequent

fabrication of certain RF devices. In some cases, the second material 20 will only have to undergo medium or low temperature treatments (less than 500°C, or even 350°C) during the subsequent steps of manufacturing the devices on substrate 100: this will allow other options for the second material 20, such as polymers, for example deposited by "sol-gel"-type techniques (spin-coating).

The substrate 100 obtained at this stage of the manufacturing process is illustrated in Fig. 1c.

According to a variant illustrated in Fig. 1d, the trenches 2 may be partially filled by the second material 20 and partially by a third material 23, of different nature and/or composition from the second material 20. The third material 23 may be chosen from the materials stated as being able to constitute the second material 20. Advantageously, the third material 23 will first be deposited on the internal walls of the trenches 2; the second material 20 then being deposited on the third material 23 to fill the trenches 2. As an example and without being considered as limiting, a first polycrystalline silicon coat may be made on the internal walls of the trenches 2; a second silicon nitride coating can then be made on the polycrystalline silicon to fill the trenches 2. In this example, the third material 23 is made of polycrystalline silicon and the second material 20 is made of silicon nitride.

According to another variant, the trenches 2 can be kept in the state of cavities, that is to say, without filling with any solid material. The second material 20 is in this case made up of a gas or a gaseous mixture, for example air or other gases, which can be introduced later during the manufacturing process according to the invention.

According to this variant, a third material 23 may also be deposited on the internal walls of the trenches 2, the major part of the trench 2 being otherwise filled only with a gas or a gaseous mixture.

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Fig. 2a illustrates a substrate 100 in plan view, that is to say, according to the first side 1. Note that the sectional view of the same substrate 100, along a sectional plan C illustrated in Fig. 2a, is presented in Fig. 2b.

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The trenches 2 filled with the second material 20 to form the first areas 11 of the first material 10' on the first side 1 and at least one second zone 21 of the second material 20. The substrate 100 is remarkable in that the first zones 11 have a maximum dimension of less than 10 microns. According to other advantageous embodiments, the maximum dimension of the first zones 11 will even be less than 8 microns, 5 microns or even 2 microns.

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The substrate 100 is also remarkable in that the first zones 11 are isolated from each other by the second zone 21 made of the second material 20, that is to say they are not in contact with each other. Advantageously, they are electrically insulated from each other, the second material 20 having a resistivity greater than 10 kohms.cm. Advantageously, the second material 20 or the third material 23 when used has properties of trapping movable electrical charges that can be generated in the first material 10 '.

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According to the examples shown in Figs. 2a and 3a, the at least one second zone 21 forms a mesh on the first side 1 of the support substrate 10 which separates each of the first zones 11. Depending on the shape of this mesh and the dimensions of the zones 11, 21, the surface density of the first zones 11 may be different. Advantageously, the surface density of the first zones 11 will be chosen so as to confer

on an upper part 200 of substrate 100, extending from the first side 1 of the support substrate 10 to the depth of the trenches 2, a mean thermal conductivity greater than 20 W/m.K, an average dielectric permittivity lower than the permittivity of the first material 10' and an effective resistivity greater than the resistivity of the first material 10' or at least greater than 1000 ohms.cm.

To illustrate, the first zones 11 may cover between 20 and 70% of the surface of the first side 1 of the support substrate 10, the second zone 21 covering the additional surface.

The trenches 2 have a depth of between 1 micron and 100 microns. For a microelectronic device (which will be laid out laterally above the upper part 200 of substrate 100) of lateral dimension a , it can be considered that the electric field will penetrate to a depth of about $a/3$ in substrate 100. Thus, for an RF antenna switching-type device with a typical lateral dimension of 100 microns, the depth of the trenches 2 must be about 30-40 microns, so that the electric field sees only the upper part 200 of substrate 100. The electrical features (effective resistivity, permittivity) of the upper part 200 will then condition the performance of the microelectronic radiofrequency devices laid out above.

The known techniques of etching make it possible to produce trenches whose form factor (ratio of lateral dimension to depth) is usually between $1/5$ and $1/30$. For example, the shape factor of the trenches 2 according to the invention will typically be between $1/5$ and $1/30$: for a maximum lateral dimension of 10 microns, the depth of the trenches 2 may be between 50 and 100 microns; for a maximum lateral dimension of 1 micron, the depth may be between 5 microns and 30 microns.

Figs. 4a and 4b show an alternative embodiment of substrate 100 according to the invention. In the upper part 200 of substrate 100, the parts made of the first material 10' can be segmented in the direction of the depth (i.e., along the Z axis in the figures). For this purpose, at least one segmentation layer 25 of the second material 20 may be deposited over the entire surface of the first side 1 of the support substrate 10 after filling the trenches 2. This segmentation layer 25 may be, in one of the second materials 20 referred to above, identical to or different from that used to fill the trenches 2.

Subsequent steps of local coating of the first material 10' opposite the first zones 11 and the second material 20 opposite the second zones 21 will then be carried out. These steps may be repeated as many times as necessary to achieve several segmentations in the thickness of the upper part 200.

Alternatively, the segmentation of the parts constituted by the first material 10' in the upper part 200 may be performed by ion implantation in substrate 100. To illustrate, the species chosen from among oxygen, nitrogen, hydrogen, helium, etc., can be introduced at a given depth in order to constitute the layer 25 segmenting in depth the first material parts 10' of the upper part 200.

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The method for manufacturing the substrate for radiofrequency microelectronic devices according to the invention may further comprise a formative stage of a dielectric layer 30 on the first side 1 of the support substrate 10 (Fig. 5a). To illustrate, its thickness may vary between a few nanometres and 3 μm . Advantageously, the dielectric layer 30 is made from a material chosen from among silicon oxide, silicon nitride, a silicon oxynitride or aluminum nitride. It may be deposited by various known

chemical deposition techniques. The dielectric layer 30 may optionally be of the same nature as the second material 20.

According to a variant, illustrated in Fig. 5b, a layer of the second material is present beneath the dielectric layer 30. In fact, during the trench filling phase 2 of the method according to the invention, a layer of the second material 20 may be deposited in the trenches 2 and on the first side 1 of the support substrate 10. A planarization phase of this layer (for example a mechanical-chemical polishing) can then be carried out to reduce the surface topology, leaving a residual layer 22 in the second material 20 on the first side 1 of the support substrate 10.

According to another variant (not shown), the residual layer 22 may constitute all or part of the dielectric layer 30.

The manufacturing process may also include a formative stage of an additional layer 24 on the first side 1 of the support substrate 10 prior to the formation of the dielectric layer 30 (Fig. 9). Advantageously, this additional layer 24 is composed of the third material 23, the latter having properties of trapping mobile electrical charges (free carriers) capable of being generated in the first material 10'.

The substrate manufacturing method for radiofrequency microelectronic devices according to the invention may also include a formative stage of a useful layer 40, laid out on a substrate 100 or 101 according to the invention.

To illustrate, the useful layer 40 is transferred by one of the thin film transfer methods well known to those skilled in the art, including:

- The Smart CutTM process, based on an implantation of light hydrogen and/or helium ions in a donor substrate and a

bonding, for example, by molecular bonding of this donor substrate to substrate 100 or 101; a detachment phase then makes it possible to separate a thin layer from the donor substrate (the useful layer), at the embrittlement level defined by the depth of implantation of the ions. Finishing steps, which may include heat treatments at high temperature, finally provide the required crystalline and surface quality to the useful layer 40. This process is particularly suitable for the manufacture of very thin useful layers, with a thickness of between a few nanometres and about 1.5 μm , for example, for silicon layers.

- The Smart Cut process followed by an epitaxial phase, making it possible in particular to obtain thicker useful layers 40, for example from a few tens of nm to 20 μm .
- Direct bonding and mechanical, chemical and/or chemical mechanical thinning processes; they consist in assembling a donor substrate by molecular bonding directly on the substrate 100 or 101 and then in thinning the donor substrate up to the desired thickness of the useful layer 40, for example by grinding and by CMP (for "chemical mechanical polishing"). These processes are particularly suitable for transferring thick layers, for example from a few microns to several tens of microns, and up to a few hundred microns.

The aforementioned layer transfer processes are advantageously based on a molecular adhesive bonding phase of a donor substrate (from which the active layer will be derived) and the support substrate 100, 101. In the particular case where the second material 20 filling the trenches 2 is a gas or a gaseous mixture, the atmosphere in the bonding enclosure will be controlled (composition of the gas, pressure, etc.) so that the gas trapped in the trenches 2

after the assembly of the two substrates corresponds to the second material 20 expected. Specifically, the atmosphere in the bonding chamber may be brought to a very low pressure in order to achieve a quasi-vacuum configuration in the trenches 2, this type of configuration being in some cases favourable to the mechanical strength of the superficial useful layer 40.

The useful layer 40 is made up of a material or stack of materials making it possible to implement RF devices, analogous or digital. It may thus be chosen from among semiconductor, conductive or insulating materials depending on the type of RF devices targeted; more specifically, it may be made up of a material chosen from among the piezoelectric materials.

The useful layer 40 may, for example, be made of silicon, germanium silicon, germanium, III-V material, lithium niobate, lithium tantalate, aluminum nitride, PZT and the like.

Figs. 6a, 6b and 6c illustrate substrates 102 according to the invention, comprising:

- o A useful layer 40,
- o A dielectric layer 30
- o A substrate 100 comprising a support substrate 10 made of a first material 10' and:

- Trenches 2 filled with a second material 20 (Fig. 6a);
- Trenches 2, the walls of which are lined with a third material 23, and which are filled with a second material 20 (Fig. 6b);
- Trenches 2, the walls of which are lined by a third material 23, and which are filled with a second material 20; an additional layer 24 being sandwiched between the first side of the support substrate 10 and the dielectric layer 30 (Fig. 6c).

As it is well known in the field of SOI substrates for radiofrequency applications, a dielectric layer, for example formed by a silicon oxide on a silicon carrier substrate, has positive charges. These charges are compensated for by negative charges coming from the support substrate at the interface with the dielectric layer. These charges generate a surface parasitic conducting layer in the support substrate, beneath the dielectric layer: the resistivity of the support substrate at this conducting layer then drops to around 10-100 ohm.cm. The electrical performances that are sensitive to the resistivity of the support substrate (such as the linearity of the signal, the level of insertion losses, the quality factors of the passive components, etc.) are therefore severely degraded by the presence of this conducting layer.

The role of the upper part 200 of substrate 102 is specifically to block the movement of the mobile charges generated in the vicinity of the first side of the support substrate 10 so that it retains a high and stable resistivity level.

Indeed, the restriction on the maximum dimension of the first zones 11 makes it possible to block the movement of potential mobile charges in the first semiconductor material 10' constituting the support substrate 10. The charges have to travel a greater distance to pass from one first zone 11 to another first neighbouring zone 11 by bypassing the trenches 2 filled with the second material 20. The effective resistivity of the upper part 200 of substrate 102 is thus increased. This makes it possible to eliminate all or part of the harmful effects of parasitic conduction which appears under the dielectric layer in a substrate 102 comprising RF devices.

To illustrate, let us take the case of a substrate 102 as illustrated in Fig. 6b, formed of a monocrystalline silicon

substrate 10 with a nominal resistivity at 8 kohms.cm, of a deposited polycrystalline silicon as the third material 23, of a deposited silicon dioxide as the second material, the trenches 2 having a depth of 20 microns; the dielectric layer 30 is also made of silicon dioxide and the useful layer 40 is of monocrystalline silicon. Fig. 10 shows a simulation of the evolution of the effective resistivity of the upper part 200 of the support substrate 10 as a function of the operating frequency of the radiofrequency devices present in and/or on the useful layer 40. Variants A, B and C in Fig. 10 correspond to three different maximum dimensions of the first zones 11: 10 microns (A), 5 microns (B) and 2 microns (C). Variant A shows that the effective resistivity of the upper part 200 remains greater than 1,000 ohms.cm for frequencies below about 2.5 GHz. Variant B allows an effective resistivity of more than 1,000 ohms.cm to be maintained for all frequencies below 5 GHz. Finally, variant C makes it possible to obtain an effective resistivity of the upper part 200 greater than the nominal resistivity of the support substrate 10 for frequencies below 5 GHz; it also makes it possible to retain an effective resistivity of more than 1,000 ohms.cm for all frequencies below 15 GHz. The confinement in the first zones 11 of the mobile charges generated in the first material 10' (silicon) under the dielectric layer 30 of silicon oxide thus makes it possible to increase the effective resistivity of the upper part 200 of the support substrate 10: the dimensions of the first zones 11 are reduced as the effective resistivity increases and remains high over a wide frequency range.

The permittivity of the upper part 200 is also improved in relation to the permittivity of the initial support 10 substrate (silicon), due to the presence of the second material (silicon dioxide) in the trenches 2.

The density of the first 11 and second zones 21 is chosen so as to maintain an average thermal conductivity of

the support substrate 11 greater than 20 W/m.K, this is achieved by varying the dimensions (in the X,Y plane) of the second zone 21.

Finally, the stability of the RF performances above 5 100°C can be improved in the upper part 200 of substrate 10 because of the presence of the third material 23 (polycrystalline silicon) on the internal walls of the trenches 2, the third material 23 advantageously having the properties of trapping movable electrical charges since at 10 least a part of the thermal carriers generated in the first material 10' between the trenches 2 is going to be trapped at the level of the third material 23 over the entire depth of the trenches 2, to provide the upper part 200 with a more stable effective resistivity over a wide range of 15 temperatures.

Performances substantially similar of effective resistivity at room temperature, of permittivity and of thermal conductivity are expected with a substrate 102 as 20 illustrated in Fig. 6a, formed for example of a support substrate 10 made of monocrystalline silicon with a nominal resistivity at 8 kohms.cm, of a gas or gas mixture as the second material 20 (air or nitrogen at atmospheric pressure or lower controlled pressure), the trenches 2 having a depth of 25 20 microns; the dielectric layer 30 is also made of silicon dioxide and the useful layer 40 is made of monocrystalline silicon.

According to another example, a substrate 102 based on 30 Fig. 6a whose second material 20 (filling the trenches 2) is made of highly resistive poly-silicon should have improved performances with respect to the stability of effective resistivity over a wide range of temperatures and the thermal conductivity of the upper part 200; the permittivity of the

upper part 200 would, on the other hand, remain close to that of the support substrate 10 (silicon).

According to yet another example, let us take the case of a substrate 102 as illustrated in Fig. 6c, formed from a monocrystalline silicon support substrate 10 with a nominal resistivity at 8 kohms.cm, of a deposited polycrystalline silicon as the third material 23, of a second material of deposited silicon dioxide or silicon nitride, the trenches 2 having a depth of 20 microns; the additional layer 24 is made of poly-silicon, the dielectric layer 30 is also made of silicon dioxide and the useful layer 40 is of monocrystalline silicon.

The performances in terms of effective resistivity of the upper part 200 over high frequency ranges (typically up to 50 GHz) are still significantly improved compared to the previous examples: the effective resistivity reaches values up to 30 kohms.cm. In this example, the presence of the additional layer 24 of third material 23 (poly-silicon) under the dielectric layer 30 makes it possible to effectively trap the free carriers generated in the first zones 11. The confinement (in the first zones 11) of the residual mobiles charges present in the first material 10' makes it possible to further increase the effective resistivity of the upper part 200 of support substrate 10.

The maximum size of the first zones 11 is advantageously chosen depending on the devices that will be produced on substrate 102 and specifically depending on their size: for example, for an antenna switch-type device comprising transistors characterized by a channel length less than 0.3 microns and a channel width greater than 500 microns, the maximum dimension (in the X, Y planes in the figures) of the first zones 11 will be chosen from around 1 micron.

Generally, the maximum dimension of the first zones 11 and the dimensions of the second zone 21 are chosen so that each component "sees" substrate 102 as a substantially homogeneous substrate, i.e., the device should neither be laid
5 out solely above a first zone 11 or solely above the second zone 21. It is beneficial that the component (in this case the transistor) has at least one dimension which extends over a plurality of first zones 11. This makes it possible in particular to limit the inhomogeneous mechanical constraints
10 at the level of the said components, capable of generating greater dispersion in the electrical features of the components.

The depth of the trenches 2, and thus the thickness of
15 the upper part 200 of substrate 101, is also defined according to the type of RF devices that will be produced on substrate 102 (or on substrate 100 or 101). Specifically, this depth is chosen based on the power generated by the devices and the depth of penetration of the electromagnetic field in substrate
20 102. For example, for an antenna switch-type device switching a power of 1 watt, penetration of the field being around 50 microns, the depth of the trenches 2 will be selected to be of the order of 50 microns, being typically between 30 and 70 microns.

It is beneficial that for RF devices operating at
25 frequencies greater than 100 MHz, the second material 20 or the third material when it is used has properties for trapping movable electrical charges that can be generated in the first material 10', as previously shown in some examples of
30 substrates 102.

The invention also relates to a structure 110 of radiofrequency microelectronic devices (illustrated in Fig. 7) comprising:

- A substrate 100 or 101 or 102 as previously described;

- A layer of microelectronic devices 50 laid out directly on substrate 100, 101 or on the dielectric layer 30, which itself is laid out on substrate 100, 101.

According to an embodiment of the invention, the microelectronic device 50 of the structure 110 may be an antenna switch or adaptor or a power amplifier or a low-noise amplifier or a passive component (R, L, C).

As an illustration for the manufacture of this type of device, it will be possible to use a substrate 102 having a useful layer 40 made of silicon with a thickness of between 10 nm and 1.5 microns, for example 145 nm, and an underlying dielectric layer 30 made of silicon oxide having a thickness of between 20 nm and 2 microns, for example 400 nm; the first zones 11 have the shape of squares of 1 micron apart, spaced 2 microns apart and the upper part 200 extends over 50 microns thick (depth of the trenches 2 filled by the second material 20). The first material 10' is monocrystalline silicon and the second material 20 is silicon nitride. Optionally, depending on the frequency of use of the targeted components, a layer of carbon-enriched polycrystalline silicon, corresponding to the third material 23, may line the walls of the trenches 2, sandwiched between the first 10' and the second materials; it may have a thickness of a few tens of nm to 200 nm. According to yet another option, an additional polycrystalline silicon layer 24 may be sandwiched between the first side of the support substrate 10 and the dielectric layer 30; the additional layer 24 may have a thickness typically ranging from 100 nm to 1 micron.

The layer of devices 50 developed in and on the useful layer 40 comprises a plurality of active components (of the

MOS type, bipolar type, etc.) and a plurality of passive components (of capacitors, inductors, resistors, etc.).

The fabrication of the microelectronic components requires the implementation of several phases, including heat
5 treatments at high temperatures, typically at 950-1100°C, or even beyond. The upper part 200 of substrate 110, consisting of silicon (first material 10'), silicon nitride (second material 20) and optionally carbon-enriched poly-silicon (third material) is able to withstand this type of treatment
10 without undergoing any degradation likely to impact its RF properties.

According to a variant, the layer of devices 50 can be firstly developed on a substrate of the SOI type and then
15 transferred by a layer transfer technique known to those skilled in the art onto substrate 100 or 101 according to the invention, to form a structure 111 illustrated in Fig. 8.

In Fig. 8, the structure 111 comprises, on the one hand, the support substrate 10 comprising the plurality of trenches
20 2, filled with the second material 20, on which is optionally laid out a residual layer 22 made of a second material 20 acting as a dielectric layer. Above the latter, there is the layer of devices 50: the so-called "back end" portion of layers of metallic interconnections and dielectrics is laid
25 out above the residual layer 22, the so-called "front end" portion (silicon), developed partly in the useful layer 40, being itself above the back-end part. Finally, above the useful layer 40, and optionally, there is a dielectric layer 31.

30

In both cases mentioned above, the electromagnetic fields resulting from the high-frequency signals intended to be spread in the devices 50 and which will penetrate into substrate 100, 101, 102 will suffer only slight losses

(insertion losses) and distortions (harmonics), due to the effective resistivity, greater than the nominal resistivity of the first material 10' of the support substrate 10 or at least greater than 1,000 ohms.cm and stable over the entire
5 operating temperature range $[-40^{\circ}\text{C}; 150^{\circ}\text{C}]$, of the upper part 200 of the structure 110, 111: in fact, the configuration of the upper part 200 according to the invention blocks the movement of the mobile charges in the semiconductor substrate (coming from the parasitic conducting layer or thermal
10 donors). Advantageously, the structure 110,111 will have favourable heat dissipating properties, the first material being silicon. Also advantageously, the capacitive coupling between the layer of devices 50 and the support substrate 10 will be greatly reduced due to the average permittivity of the
15 upper part 200, reduced compared to that of the silicon due to the presence of the trenches filled with the second material (highly resistive or insulating).

According to another embodiment of the invention, the
20 microelectronic device 50 of the structure 110, 111 may consist of a radiofrequency MEMS (Micro Electro-Mechanical Systems) component, comprising, for example, at least one control element and a MEMS switching element consisting, for example, of a microswitch with ohmic contact or a capacitive
25 microswitch.

One of the substrates 100, 101, 102 may be used as a support substrate for the MEMS component; the fabrication of the MEMS part is then based on successive coatings of a plurality of layers (including an electrode, a dielectric, a
30 sacrificial layer, an active layer) and by making patterns on these different layers.

The first zones 11 will, for example, be in the form of hexagons of 10 microns apart, spaced 10 microns apart, and the upper part 200 will extend over 50 microns thick (depth of the

trenches 2 filled by the second material 20). The first material 10' may be monocrystalline silicon and the second material 20 made of the silicon nitride.

5 The microelectronic processes for manufacturing the control element(s) (CMOS, for example), usually carried out before the MEMS part, require, as in the previous embodiment, the application of heat treatments at high temperatures.

10 According to a variant of the invention, which can be applied to all the embodiments described, the mesh formed by the second zone 21 on the first side 1 of substrate 100 may be located in specific regions of the first side. It will thus be possible to have a plurality of second zones 21 distributed over the first side 1 of substrate 100. In the areas of the first side 1 lacking these second zones 21, therefore, is
15 found only the first material 10' of the support substrate 10. The control elements (CMOS) of the device, if they do not require an underlying substrate with resistivity, restrictive permittivity properties such as RF elements, may be developed in areas devoid of second zones 21 (i.e., without trenches 2).

20 As mentioned above, the high-frequency signals propagating in this device 50 generate electromagnetic fields (notably at the level of the MEMS switching elements) which penetrate into the support substrate 10. The losses (insertion losses), distortions (harmonics) and disruptions will be less because
25 of the high and stable effective resistivity of the upper part 200 of the support substrate 10 comprising trenches filled with the second material 20.

Advantageously, the structure 110,111 will have favourable heat dissipating properties, the first material being silicon.
30 Also advantageously, the capacitive coupling between the layer of devices 50 and the support substrate 10 will be greatly reduced due to the average permittivity of the upper part 200, reduced compared to that of the silicon due to the presence of

the trenches filled with the second material (highly resistive or insulating).

5 According to yet another embodiment of the invention, the microelectronic device 50 of the structure 110, 111 may consist of a radiofrequency filter, operating by bulk acoustic wave propagation (called "BAW" for "Bulk Acoustic Wave" or by acoustic propagation (known as "SAW" for "Surface Acoustic
10 Wave") or any other acoustic propagation mode.

 The manufacture of a SAW filter requires, for example, a useful layer 40 made of a piezoelectric material, on the surface of which an electrode comb will be developed: the acoustic wave is intended to spread between these electrodes.
15 The structure 110 according to the invention may thus comprise, as an illustration, a useful layer 40 of lithium tantalate with a thickness of between 200 nm and 20 μ m.

 The first zones 11 may have a circular shape of 5 microns in diameter, spaced 5 microns apart and the upper part 200 may extend over 100 microns in thickness (trench depth 2). The first material 10' is monocrystalline silicon and the second material 20 may be air or amorphous or polycrystalline silicon. A dielectric layer 30 may optionally be added between the useful layer 40 and the first side 1 of the
20 support substrate 10.
25

 The structure 110, in addition to being naturally more stable in temperature than a solid piezoelectric substrate, makes it possible to obtain better filter performance, notably in terms of insertion losses and linearity.

30

 The substrates 100, 101, 102 and the structures 110, 111 for radiofrequency applications according to the invention are not limited to the embodiments mentioned above. They are suitable for any application for which high frequency signals

spread and are liable to suffer undesired losses or disturbances in a support substrate: indeed, the physical and electrical features of the upper part 200 of the substrate confer on the assembly good RF properties (limiting losses, non-linearities and other disturbances), stable over the entire operating temperature range. They also confer good thermal conductivity properties and a relative permittivity of less than 11 allowing a weak capacitive coupling between the active layer and the support substrate 10. By choosing the dimensions of the first 11 and second 21 zones and the nature of the first 10', second 20 and potentially 3rd materials, it is possible to give priority to certain performances (effective resistivity, stability in temperature, thermal conductivity, permittivity) over others; depending on the applications, compromises can thus be found, on the one hand, to meet the specifications of the microelectronic devices to be developed, but also to meet the manufacturing cost of substrate 100, 101, 102 thus enabling its mass adoption.

The substrates 100, 101, 102 and the structures 110, 111 according to the invention may specifically be of interest for devices combining RF functions with high-performance digital or analogue functions (i.e., with high operating frequencies f_T , $f_{\max}$).

In some cases, the digital and/or analogue functions do not require a resistive substrate that has the properties according to the invention: the upper part 200 of the substrate according to the invention, comprising the trenches filled with the second material 20, can then be local and not present on the entire substrate 100, 101, 102. There is thus a plurality of second zones 21 on the first side 1 of the substrate, located in different regions of the first side. In the areas of the first side 1 lacking these second zones 21,

therefore, is found only the first material 10' of the support substrate 10. The digital and/or analogue functions of the device, if they do not require an underlying substrate with resistivity, restrictive permittivity properties such as RF components, may be developed in areas lacking second zones 21 (i.e., without trenches 2).

Of course, the invention is not limited to the embodiments and examples described, and variants can be provided without departing from the scope of the invention as defined by the claims.

CLAIMS

1. A substrate for microelectronic radiofrequency devices comprising:

5 a support substrate comprising a first semiconductor material having a resistivity greater than 500 ohms.cm;

10 a plurality of trenches in the support substrate partially filled with a second material and partially filled with a third material, the third material having a composition different than the second material., the plurality of trenches defining a plurality of first zones on a first side of the first semiconductor material and at least one second zone of
15 a second material, the second material having a resistivity greater than 10 kohms.cm, the plurality of first zones having a maximum lateral dimension of less than 10 microns, the plurality of first zones being isolated from one another by the at least one second
20 zone.

2. The substrate of claim 1, wherein a surface density of the plurality of first zones and the at least one second zone confers on an upper part of the substrate
25 extending from the first side of the support substrate to a depth of the plurality of trenches, an average thermal conductivity greater than 20 W/m.K, an average dielectric permittivity lower than the permittivity of the first semiconductor material, and a resistivity higher than the
30 resistivity of the first semiconductor material.

3. The substrate of claim 1, wherein the at least one second zone forms a mesh on the first side of the support substrate.

4. The substrate of claim 1, wherein the depth of the plurality of trenches is between 1 micron and 100 microns.

5

5. The substrate of claim 1, wherein the first semiconductor material comprises silicon.

6. The substrate of claim 1, wherein the second material partially filling the plurality of trenches is selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, aluminum nitride, amorphous or polycrystalline silicon, carbon-rich silicon, a polymer, or a gas.

15

7. The substrate of claim 1, wherein the third material is located on internal walls defining the plurality of trenches and the second material is located on a side of the third material opposite the first semiconductor material of the support substrate.

20

8. The substrate of claim 1, wherein the third material is selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, aluminum nitride, amorphous or polycrystalline silicon, carbon-rich silicon, a polymer, or a gas.

25

9. The substrate of claim 1, further comprising a dielectric layer on the first side of the support substrate.

30

10. The substrate of claim 9, further comprising an additional layer between the dielectric layer and the first

side of the support substrate comprised of a third material.

11. The substrate of claim 9, wherein the dielectric
5 layer comprises a material selected from the group
consisting of silicon oxide, silicon nitride, silicon
oxynitride, or aluminum nitride.

12. The substrate of claim 9, wherein the dielectric
10 layer is comprised of the second material.

13. The substrate of claim 1, further comprising a
useful layer on the first side of the support substrate.

14. The substrate of claim 13, further comprising a
15 dielectric layer on the first side of the support
substrate, wherein the dielectric layer is sandwiched
between the useful layer and the first side of the support
substrate.

15. The substrate of claim 13, wherein the useful
20 layer comprises a material selected from a group consisting
of a semiconductor material, an insulating material, a
conductive material, or a piezoelectric material.

16. A microelectronic device structure, comprising:
25 a substrate as recited in claim 1; and
a layer of microelectronic devices on the substrate.

17. The microelectronic device structure of claim 35,
30 wherein at least one of the microelectronic devices
comprises an antenna switch, an adaptor, a power amplifier,
a low noise amplifier, a passive component, a high

frequency circuit, a radio frequency MEMS component, or a radiofrequency filter.

18. A method for manufacturing a substrate for
5 microelectronic radiofrequency devices, comprising:
- providing a support substrate comprising a first semiconductor material having a resistivity greater than 500 ohms.cm, the support substrate having a first side;
 - 10 etching, according to a mask, a plurality of trenches extending from the first side of the support substrate to a determined depth within the support substrate;
 - partially filling the plurality of trenches with
15 a third material; and
 - filling remainders of the plurality of trenches with a second material to form first zones of a first material and at least one second zone on the first side of the second material, the first zones having a
20 maximum lateral dimension of 10 microns or less, the first zones being insulated from one another by the second zone, the second material having a resistivity greater than 10 kohms.cm, the second material having a composition different than the third material.

25

19. A method for manufacturing a substrate for
microelectronic radiofrequency devices, comprising:
- providing a support substrate comprising a first semiconductor material having a resistivity greater
30 than 500 ohms.cm;
 - depositing, according to a mask, a plurality of pillars made from the first material and of a determined height, on the support substrate, an upper surface of the pillars defining a first side of the

substrate, the pillars being insulated from each other by a plurality of trenches extending from the first side of the support substrate to a depth within the support substrate defined by the determined height of the pillars;

partially filling the plurality of trenches with a third material; and

filling remainders of the plurality of trenches with a second material to form first zones of the first material and at least one second zone on the first side of the second material, the first zones having a maximum lateral dimension of 10 microns or less, the first zones being insulated from one another by the at least one second zone, the second material having a resistivity greater than 10 kohms.cm, the second material having a composition different than the third material.