

Description

The invention relates to an electronic circuit for amplifying a circuit input signal differentially provided between first and second input terminals as respective first and second input voltages, the circuit comprising:

main supply means, coupled between respective sources of a high supply voltage V_{HH} and a low supply voltage V_{LL} whose difference is a power supply voltage V_{PS} that defines a power supply range, for providing opposite first and second operating currents;

first differential means for amplifying the voltage difference between first and second input points by largely dividing the first operating current into a pair of amplified first internal signals, the first and second points being respectively coupled to the first and second terminals, the first means being operatively conductive to so produce the first internal signals when the common-mode voltage V_{CM} of the circuit input signal is in a portion of the supply range extending up to V_{HH} ;

second differential means for amplifying the voltage difference between third and fourth input points by largely dividing the second operating current into a pair of amplified second internal signals, the third and fourth points being respectively coupled to the first and second terminals, the second means being operatively conductive to so produce the second internal signals when V_{CM} is in a portion of the supply range extending down to V_{LL} such that at least one of the differential means is operatively conductive as V_{CM} traverses substantially the entire supply range when V_{PS} is greater than or equal to a specified minimum level; and

summing means for combining the internal signals to generate at least one circuit output signal;

Such a circuit is known from US Patent 4,555,673 and relates to a differential amplifier suitable for use in an operational amplifier ("op amp") made in semiconductor integrated circuit form and, more specifically, to a differential amplifier that employs complementary differential portions to attain rail-to-rail input capability.

An integrated circuit often needs a lower power supply voltage to avoid heat-dissipation problems. Low supply voltage will be even more necessary in the future as integrated circuits become increasingly more dense. It thus becomes desirable that a differential amplifier used as an input stage in an op amp have rail-to-rail input capability. That is, the output signal of the amplifier should be representative of the differential input signal as its common-mode voltage travels the full range of the power supply voltage. As used here to describe the relationship between two signals, "representative" means that their amplitudes have a substantially one-to-one (typically linear) relationship as long as the amplitudes are not too great.

Referring to the drawings, Fig. 1 illustrates a general arrangement for a prior art differential amplifier that can achieve rail-to-rail input capability at moderately low power supply voltage. See U.S. Patent 4,555,673. Also see U.S. Patents 4,463,319 and 4,532,479.

The amplifier in Fig. 1 employs a pair of complementary differential input portions 10 and 12 to amplify a circuit input signal differentially supplied between input terminals T1 and T2 as input voltages V_{I1} and V_{I2} . Differential portion 10 consists of NPN transistors Q1 and Q2 whose bases receive the circuit input signal at input points P1 and P2 connected to terminals T1 and T2. The emitters of transistors Q1 and Q2 are connected together at a node N_A to receive a first operating current I_A . Differential portion 12 is formed with PNP transistors Q3 and Q4 whose bases receive the circuit input signal at input points P3 and P4 connected to terminals T1 and T2. The emitters of transistors Q3 and Q4 are connected together at a node N_B to receive a second operating current I_B . A main current supply 14 connected between sources for a high supply voltage V_{HH} and a low supply voltage V_{LL} provides currents I_A and I_B in opposite flow directions.

Portion 10 supplies amplified internal currents I_{B1} and I_{B2} from the Q1 and Q2 collectors. Portion 12 similarly provides amplified internal currents I_{D3} and I_{D4} from the Q3 and Q4 collectors. A summing circuit 16 connected between the V_{HH} and V_{LL} supplies suitably combines currents $I_{D1} - I_{D4}$ to generate a pair of complementary output currents I_O and $I_{\bar{O}}$.

In looking at amplifier operation, it is convenient to define several terms. Let " ΔV " and " V_{CM} " respectively represent the differential voltage $V_{I1} - V_{I2}$ and the common-mode voltage $(V_{I1} + V_{I2})/2$ of the circuit input signal. Let " V_{PS} " represent the power supply voltage $V_{HH} - V_{LL}$.

The prior art device in Fig. 1 can be characterized by a pair of threshold voltages V_{TA} and V_{TB} that may vary with V_{PS} . Fig. 2 shows a general example of how V_{TA} and V_{TB} may appear. Fig. 3 shows the resulting operational regions for the amplifier. The horizontal axis in Fig. 3 represents the condition where V_{CM} equals V_{LL} . Line 18 (at 45°) represents the condition where V_{CM} equals V_{HH} . The region between the horizontal axis and line 18 thereby encompasses the rail-to-rail operational range for the amplifier.

Input portion 10 is operatively conductive (turned on) when V_{CM} is sufficiently high. More specifically:

$$V_{CM} - V_{LL} \geq V_{TA} \quad (1)$$

Eq. (1) basically corresponds to the portion of the V_{PS} range between line 20A and line 18 in Fig. 3. The conductive region for portion 10 does, however, extend slightly above line 18 to a point where V_{CM} is several tenths of a volt more than V_{HH} . When portion 10 is turned on, it amplifies the voltage difference between

points P1 and P2 by splitting current I_A between currents I_{D1} and I_{D2} at values whose difference is representative of ΔV .

Input portion 12 is operatively conductive when V_{CM} is sufficiently low. In particular:

$$V_{HH} - V_{CM} \geq V_{TB} \quad (2)$$

Eq. (2) basically corresponds to the portion of the V_{PS} range between the horizontal axis and line 20B in Fig. 3. In addition, the conductive range for portion 10 extends slightly below the horizontal axis to a point where V_{CM} is several tenths of a volt less than V_{LL} . When portion 12 is turned on, it amplifies the voltage difference between points P3 and P4 by splitting current I_B between current I_{P3} and I_{P4} at values whose difference is representative of V .

Fig. 3 indicates that portion 10 is turned off in the space between the horizontal axis and line 20A-- i.e., when $V_{CM} - V_{LL}$ is less than V_{TA} . Likewise, Fig. 3 shows portion 12 as being turned off in the area between line 20B and 18. This corresponds to the condition in which $V_{HH} - V_{CM}$ is less than V_{TB} . In actually, each of portions 10 and 12 usually switches between on and off over a spacing on the order of 100 millivolts. Lines 20A and 20B are thus idealizations of narrow voltage regions.

When V_{PS} is reduced, the amount of V_{CM} space available for the non/conductive regions for portions 10 and 12 decreases. The two non-conductive regions start to overlap when V_{PS} reaches a level V_{PSO} . If V_{PS} drops below V_{PSO} , V_{CM} passes through a "dead zone" indicated by thick line 22 in which neither of portions 10 and 12 is operatively conductive. V_{PSO} is thus the value of the minimum V_{PS} level at which the differential amplifier in Fig. 1 can achieve rail-to-rail input capability.

Threshold V_{TA} and V_{TB} have respective minimum values V_{MA} and V_{MB} . See lines 24 and 26 in Fig. 3. In known embodiments of the amplifier in Fig. 1, V_{PSO} is approximately equal to $V_{MA} + V_{MB}$.

The numerical value of V_{PSO} depends on the base-emitter voltages of transistors Q1 - Q4 and on the internal construction of current supply 14. Figs. 4a and 4b depict two ways, both described in U.S. Patent 4,555,673, for implementing supply 14. Figs. 5a and 5b graphically show the specific idealized operational regions for the amplifier of Fig. 1 as implemented with the main current supplies shown respectively in Figs. 4a and 4b.

Starting with the embodiment of Fig. 4a, supply 14 consists simply of a pair of current sources S_L and S_H . Current source S_L supplies current I_A at a constant value I_L . Current source S_H provides current I_B at a constant value I_H . For current source S_L and S_H to be conductive, the voltage across each of them must be at least equal to a minimum level V_{SAT} .

V_{CM} exceeds the voltage at node N_A by $1V_{BE}$ when portion 10 is turned on. V_{BE} is the magnitude of the standard voltage across the base-emitter junction

of a bipolar transistor when it is just turned on. The voltage at node NB similarly exceeds V_{CM} by $1V_{BE}$ when portion 12 is turned on. In view of this, each of threshold minimums V_{MA} and V_{MB} equals $V_{BE} + V_{SAT}$. V_{PSO} thereby equals $2V_{BE} + 2V_{SAT}$.

At a standard collector-emitter current of several microamperes, V_{BE} is approximately 0.6 volt. V_{SAT} can be as low as 0.1 volt. Using these values for V_{BE} and V_{SAT} (in the present computation and in all the additional ones below), V_{PSO} is approximately 1.4 volts for the differential amplifier of Figs. 1 and 4a.

A disadvantage of using the current supply in Fig. 4a is that the transconductance of the amplifier changes by a factor of approximately 2 whenever either of portions 10 and 12 turns on or off. The variation in transconductance makes it difficult to optimize the frequency compensation for the amplifier when it is used in an op amp with negative feedback. The implementation shown in Fig. 4b overcomes this problem.

When the circuitry of Fig. 4b is used, supply 14 is formed with current source S_H , a PNP steering transistor QP whose base receives a reference voltage V_{RP} , and a current mirror 28 that supplies current I_A at a value largely equal to the current I_{QP} through transistor QP. Current steering through transistor QP enables the sum of I_A and I_B to approximately equal I_H . As a result, the transconductance is nearly constant as V_{CM} varies across the entire V_{PS} range.

The voltage across current mirror 28 between node N_A and the V_{LL} supply must be at least $1V_{SAT}$ for mirror 28 to be conductive. Under optimum conditions, the current steering causes lines 20A and 20B in Fig. 3 to merge into a single line 20 separated from line 18 by a vertical displacement equal to V_{MB} as depicted in Fig. 5B. V_{MA} equals $V_{BE} + V_{SAT}$ again. V_{MB} may be as low as $V_{BE} + V_{SAT}$. Consequently, V_{PSO} may again be equal to 1.4 Volts.

As the above discussion indicates, the lowest tolerable value for V_{PS} in the differential amplifier of Fig. 1 is approximately 1.4 volts. In practice, V_{PS} may have to be a few tenths of a volt higher. While this is still relatively good, it would be quite useful to get down to 1.0 volt or less. For example, a single-cell battery having an unloaded rating of 1.5 volts typically drops down to about 1.0 volt under loaded conditions near the end of its life. The amplifier of Fig. 1 cannot operate efficiently from such a battery.

It is the object of the invention to provide a differential amplifier that can achieve rail-to-rail input capability at a very low power supply voltage. In bipolar embodiments, the power supply voltage can be at or slightly below 1.0 volts. This makes the invention particularly attractive for future low-voltage op amp applications. The invention can be powered from a single-cell 1.5-volt battery during the entire battery life.

According to the invention a circuit asset forth in the opening paragraph is characterize in that the cir-

cuit further comprises:

level-shift means for selectively causing the voltages at the first and second points to be respectively higher than the first and second input voltages by respective first and second voltage level shifts and for selectively causing the voltages at the third and fourth points to be respectively lower than the first and second input voltages by respective third and fourth voltage level shifts.

The level shift means extend the conductive operational ranges of the differential means so as to reduce the value of the minimum level of the power supply voltage at which the differential amplifier achieves rail-to-rail input capability.

The circuit may be characterized further in that the level-shift means comprises:

network means, coupled between the terminals and the points, for providing the level shifts; and level-shift supply means for providing current to the network means to control the values of the level shifts.

The network means may be characterized in that the network means comprises a first level-shift element coupled between the first terminal and the first point, a second level-shift element coupled between the second terminal and the second point, a third level-shift element coupled between the first terminal and the third point, and a fourth level-shift element coupled between the second terminal and the fourth point.

The level shift supply means may be characterized in that the level-shift supply means comprises a first current source coupled between the first point and the V_{HH} source, a second current source coupled between the second point and the V_{HH} source, a third current source coupled between the third point and the V_{LL} source, a fourth current source coupled between the fourth point and the V_{LL} source, and control means for controlling conduction of the current sources. The control means preferably operates in such a way as to gradually turn off the level-shift means as the power supply voltage rises to a point where level shifting is not needed.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 shows a block and circuit diagram of a prior art differential amplifier,

Figs. 2 and 3 show graphs depicting operational features for the amplifier of Fig. 1,

Figs. 4a and 4b show circuit diagrams of prior art embodiments of the main current supply in Fig. 1, Fig. 5a and 5b show graphs showing the primary operational regions for the amplifier of Fig. 1 as respectively embodied with the current supplies of Figs. 4a and 4b,

Fig. 6 shows a block diagram of a general differential amplifier in accordance with the invention,

Fig. 7a and 7b show graphs generally illustrating the operational regions for the amplifier of Fig. 6, Fig. 8 show a block diagram of an embodiment of the level-shift current supply in Fig. 6,

Fig. 9a, 9b, and 10 show graphs generally showing operational parameters for the amplifier of Fig. 6 as embodied with the circuitry of Fig. 8,

Fig. 11 shows a block and circuit diagram of a general embodiment of the amplifier of Fig. 6,

Fig. 12 shows a block diagram of an embodiment of the level-shift current control in Fig. 11,

Figs. 13a, 13b, and 13c show graphs illustrating how level-shift voltage preferably varies as a function of input common-mode voltage for the amplifier of Fig. 11,

Figs. 14a and 14b show graphs showing the operational regions for the amplifier of Fig. 11 as respectively embodied with the current supplies of Figs. 4a and 4b,

Fig. 15 shows a circuit diagram of a preferred bipolar embodiment of the amplifier of Fig. 11,

Fig. 16 shows a circuit diagram of a preferred embodiment of the reference voltage circuitry in Fig. 15,

Fig. 17 shows a graph illustrating the operational regions for the amplifier of Fig. 15 as embodied with the complete reference voltage circuitry in Fig. 16,

Figs. 18a and 18b show graphs showing an alternative variation for level-shift current as a function of input common-mode voltage for the amplifier of Fig. 11,

Fig. 19 shows a graph illustrating the operational regions for the amplifier of Fig. 11 as embodied with the current supply of Fig. 4a for the level-shift variation indicated in Figs. 18a and 18b and

Fig. 20 shows a block and circuit diagram of another general embodiment of Fig. 6.

Like reference symbols are employed in the drawings and in the description of the preferred embodiments to represent the same or very similar item or items.

Referring to Fig. 6, it illustrates a general arrangement for a differential amplifier that amplifies a circuit input signal differentially supplied between input terminals T1 and T2 as input voltages V_{I1} and V_{I2} . This differential amplifier uses a level-shifting technique in accordance with the invention to attain rail-to-rail capability for the common-mode voltage V_{CM} of the circuit input signal at very low power supply voltage. The amplifier is particularly suitable for use as an input stage of a low-voltage op amp fabricated in semiconductor integrated circuit form.

The device in Fig. 6 centers around complementary differential input portions 30 and 32. Differential portion 30 consists of like-configured three-electrode input amplifiers A1 and A2. Differential portion 32 is formed with like-configured three-electrode input

amplifiers A3 and A4 which are complementary to amplifiers A1 and A2. The term "complementary" means opposite polarity.

Amplifiers A1 - A4 are referred to here as the "A" amplifiers. Each "A" amplifier has a first flow electrode (1E), a second flow electrode (2E), and a control electrode (CE) for controlling current flow between the flow electrodes (1E and 2E). Charge carriers, either electrons or holes, that move between the flow electrodes of each "A" amplifier originate at its first flow electrode and terminate at its second flow electrode. The current (if any) flowing in the control electrode is much smaller than that otherwise moving between the flow electrodes.

Each "A" amplifier preferably consists of a single transistor. In the case of a bipolar transistor, its emitter, collector, and base are respectively the first, second, and control electrodes. These elements are respectively the source, drain, and gate for a field-effect transistor of either the insulated-gate or junction type.

Although generally undesirable, each "A" amplifier could consist of more than one transistor. One example is a bipolar Darlington circuit in which the emitter of an input transistor is connected to the base of a trailing transistor. In this case, the control electrode of the "A" amplifier is (connected to) the base of the input transistor, while the first and second control electrodes are (connected to) the emitter and collector of the trailing transistor.

As used in describing amplifiers A1 and A2 or A3 and A4, "like-configured" means that the two amplifiers in question have corresponding elements interconnected in the same way and that each set of corresponding elements is of the same semiconductor polarity. For example, amplifiers A1 and A2 are like-configured if both are NPN transistors but not if one is an NPN transistor while the other is a PNP transistor. Likewise, Darlington circuits are like-configured as long as the input transistors are of the same polarity and the trailing transistors are of the same polarity (even if different from that of the input transistors).

Turning back to Fig. 6, the first electrode of amplifiers A1 and A2 are connected together to receive operating current I_A at node N_A . Similarly, amplifiers A3 and A4 have their first electrodes connected together to receive operating current I_B at node N_B . A main current supply 34 connected between the V_{HH} and V_{LL} supplies provides oppositely directed currents I_A and I_B . Current supply 34 may be implemented using either of the circuits shown in Figs. 4a and 4b. Other embodiments described in U.S. Patent 4,555,673 may also be used.

Differential portions 30 and 32 function in a complementary manner. When V_{CM} is sufficiently high, portion 30 amplifies the voltage difference between input points P1 and P2 connected to the A1 and A2 control electrodes by dividing current I_A into amplified internal currents I_{D1} and I_{D2} supplied from the A1 and

A2 second electrodes. The difference between the currents I_{D1} and I_{D2} is representative of the voltage difference between points P1 and P2. When V_{CM} is sufficiently low, portion 32 amplifies the voltage difference between input points P3 and P4 connected to the A3 and A4 control electrodes by dividing current I_B into amplified internal currents I_{D3} and I_{D4} supplied from the A3 and A4 second electrode. The difference between currents I_{D3} and I_{D4} is representative of the voltage difference between points P3 and P4.

A summing circuit 36 connected between the V_{HH} and V_{LL} supplies suitably combines currents $I_{D1} - I_{D4}$ to produce complementary circuit output currents I_O and $\bar{I}_O$. Summing circuit 36 may be implemented in any of the ways shown in U.S. Patents 4,555,673 and 4,532,479. If desired, circuit 36 may provide only a single circuit output current.

A level-shift circuit consisting of a network of level-shift elements 38, 40, 42, and 44 and a level-shift supply circuit 46 selectively enables voltages V_{P1} and V_{P2} at points P1 and P2 to exceed voltages V_{I1} and V_{I2} by controllable level shifts V_{LS1} and V_{LS2} . The level-shift circuit likewise selectively enables voltages V_{P3} and V_{P4} at points P3 and P4 to be less than voltages V_{I1} and V_{I2} by controllable level shifts V_{LS3} and V_{LS4} . Level-shift elements 38 - 44, which are connected between terminals T1 and T2 and points P1 - P4 in the manner shown in Fig. 6, directly provide level-shift voltages $V_{LS1} - V_{LS4}$.

Level-shift current supply 46, which is connected between the V_{HH} and V_{LL} supplies, controls the operation of level shifts 38 - 44. Current supply 46 accomplishes the control by providing supply currents I_{S1} , I_{S2} , I_{S3} and I_{S4} along lines connected to points P1 - P4. Although not indicated in Fig. 6, supply 46 is typically connected to other points in the amplifier circuit. For example, supply 46 may provide current at terminals T1 and T2 in some embodiments of the invention.

As indicated in Fig. 6, level-shift currents I_{LS1} , I_{LS1} , I_{LS3} , and I_{LS4} actually flow through elements 38 - 44. Currents $I_{LS1} - I_{LS4}$ respectively differ from currents $I_{S1} - I_{S4}$ by the currents (if any) flowing through the respective control electrodes of amplifiers A1 - A4. The control-electrode current normally can be neglected. As a result, each level-shift current I_{LSi} is substantially equal to corresponding supply current I_{Si} (where i is 1, 2, 3, or 4).

To have a good common-mode rejection ratio, V_{LS1} and V_{LS2} are preferably equal. Consequently, I_{LS1} and I_{LS2} are preferably equal. Likewise, V_{LS3} and V_{LS4} are preferably equal so that I_{LS3} and I_{LS4} are also preferably equal.

It is desirable to avoid loading the circuitry that supplies circuit inputs V_{I1} and V_{I2} . Except for the situation in which other internal current of significant magnitude is supplied at terminals T1 and T2, this objective can usually be reached by setting I_{LS3} equal to I_{LS1} . Likewise, I_{LS4} is usually chosen to equal I_{LS2} . The

result is that currents I_{LS1} and I_{LS4} are typically all equal. Nonetheless, voltages V_{LS3} and V_{LS4} may still respectively differ from voltages V_{LS1} and V_{LS2} .

Current supply 46 utilizes currents $I_{S1} - I_{S4}$ to control the values of voltages $V_{LS1} - V_{LS4}$ in a way that reduces the minimum rail-to-rail V_{CM} level for the power supply voltage to a value lower than that which would be needed if (a) V_{P1} and V_{P3} always equalled V_{I1} and (b) V_{P2} and V_{P4} always equalled V_{I2} . An understanding of how the level-shift control is accomplished can be facilitated by first considering what would happen if components 38 - 46 were absent. In that case, the operation would proceed basically in the manner described above for the differential amplifier of Fig. 1. When power supply voltage V_{PS} drops below prior art value V_{PS0} , V_{CM} would pass through (at least part of) the dead zone in which neither of portions 30 and 32 is operatively conductive.

With the level-shift circuit present, the operation can still be described in terms of thresholds V_{TA} and V_{TB} shown in Fig. 2. However, V_{CM} in Eq. (1) must be replaced with the common-mode voltage V_{CMA} at points P1 and P2. Differential portion 30 is turned on when:

$$V_{CMA} - V_{LL} \geq V_{TA} \quad (3)$$

In view of Eq. (3), V_{LS1} and V_{LS2} must be related to V_{TA} as follows in order to make portion 30 operatively conductive if V_{CM} is not high enough in itself to turn portion 30 on:

$$V_{LS1}, V_{LS2} \geq V_{TA} - V_{CM} - V_{LL} \quad (4)$$

Because supply 46 operates from the V_{HH} supply, Eq. (4) is at least subject to the limitation that:

$$V_{LS1}, V_{LS2} < V_{HH} - V_{CM} \quad (5)$$

V_{CM} in Eq. (2) must similarly be replaced with the common-mode voltage V_{CMB} at points P3 and P4. Portion 32 is turned on when:

$$V_{HH} - V_{CMB} \geq V_{TB} \quad (6)$$

Accordingly, V_{LS3} and V_{LS4} must satisfy the following relationship with V_{TB} so as to make portion 32 operatively conductive if V_{CM} itself is not low enough to turn portion 32 on:

$$V_{LS3}, V_{LS4} \geq V_{TB} = V_{CM} - V_{HH} \quad (7)$$

Since supply 46 also operates from the V_{LL} supply, Eq. (7) is at least subject to the restriction that:

$$V_{LS3}, V_{LS4} < V_{CM} - V_{LL} \quad (8)$$

A level shift is usually not needed when V_{PS} is greater than V_{PS0} (since V_{CM} will be sufficient in itself to cause one or both of portions 30 and 32 to turn on). When V_{PS} is less than V_{PS0} so that a level shift is needed, thresholds V_{TA} and V_{TB} are preferably at their respective minimum values V_{MA} and V_{MB} . As a result, V_{MA} and V_{MB} can be respectively substituted for V_{TA} and V_{TB} in Eq. (4) and (7).

Let V_{SATH} be the minimum voltage spacing that supply 46 allows between V_{HH} and the highest of V_{P1} and V_{P2} . Likewise, let V_{SATL} be the minimum voltage spacing that supply 46 permits between V_{LL} and the lowest of V_{P3} and V_{P4} . When V_{CM} is not adequate by

itself to cause at least one of portions 30 and 32 to become conductive, supply 46 thereby normally provides currents $I_{S1} - I_{S4}$ at values that enable level shifts $V_{LS1} - V_{LS4}$ to satisfy the following relationships:

$$V_{HH} - V_{CM} - V_{SATH} \geq V_{LS1}, V_{LS2} \geq V_{MA} - V_{CM} + V_{LL} \quad (9)$$

$$V_{CM} - V_{LL} - V_{SATL} \geq V_{LS3}, V_{LS4} \geq V_{MB} + V_{CM} - V_{HH} \quad (10)$$

For the situation in which V_{TA} and V_{TB} vary in the manner indicated in Fig. 2, Figs. 7a and 7b show the operational regions that result from using the level-shift circuit. Fig. 7b is a 3X magnification of a lower portion of Fig. 7a encompassing the V_{MA} -to- V_{PS0} part of the V_{PS} range. Lines 18, 24, and 26 are the V_{HH} , V_{MA} , and V_{MB} lines as in Fig. 3. Lines 20A, 20B, and 22 of Fig. 7a have the same meaning for the invention that lines 20A, 20B, and 22 have in Fig. 3 for the prior art circuit of Fig. 1.

The point where the non-conductive region for portion 30 starts to overlap with the non-conductive region for portion 32 occurs when V_{PS} is at a value V_{PSF} as indicated in Fig. 7a. This is the lowest value of the power supply voltage at which the differential amplifier of Fig. 6 can achieve rail-to-rail input capability. Due to the level shift, V_{PSF} is less than V_{PS0} . For the usual case in which V_{PS0} equals $V_{MA} + V_{MB}$, V_{PSF} is thus less than $V_{MA} + V_{MB}$.

The lower limit for V_{PSF} is slightly greater than the larger of V_{MA} and V_{MB} in the normal situation. More specifically, V_{PSF} usually equals (a) $V_{MA} + V_{SATH}$ or (b) $V_{MB} + V_{SATL}$, whichever is larger.

Turning briefly to Fig. 7b, the three different zones of the triangular operational region formed by lines 22, 24 and 26 are labeled with reference numbers 48, 50, and 52. If V_{CM} is in zone 48, the level-shift circuit preferably adjusts V_{LS1} and V_{LS2} according to Eq. (9) so as to turn portion 30 on. If V_{CM} is in zone 50, the level-shift circuit preferably adjusts V_{LS3} and V_{LS4} according to Eq. (10) in order to turn portion 32 on. Finally, the level-shift circuit adjusts $V_{LS1} - V_{LS4}$ according to Eqs. (9) and (10) so as to turn on both of portions 30 and 32 when V_{CM} is in zone 52.

Fig. 8 illustrates in general functional embodiment for current supply 46 in Fig. 6. In this embodiment, a common-mode generator 54 responsive to circuit inputs V_{I1} and V_{I2} produces operating voltages V_{YA} and V_{YB} that bear specific relationships to V_{CM} . For example, each of voltages V_{YA} and V_{YB} may differ from V_{CM} by an amount that is largely constant at a given temperature. In response to signals V_{YA} and V_{YB} , a level-shift current control circuit 56 generates a pair of control voltages V_{CL} and V_{CH} that control the operation of a set of level-shift current sources 58 suitably connected between the V_{LL} and V_{HH} supplies. Sources 58 provide supply currents $I_{S1} - I_{S4}$.

Turning back to current control 56, it consists of voltage reference sources 60 and 62, differential amplifiers 64 and 66, and a linear AND/NAND generator

68. Reference sources 60 and 62 provide reference voltages V_{RA} and V_{RB} at values respectively "referenced" to low supply voltage V_{LL} and high supply voltage V_{HH} . In particular, V_{RA} typically exceeds V_{LL} by an amount V_{KA} that is largely constant at a given temperature. V_{RB} is likewise lower than V_{HH} by an amount V_{KB} that is largely constant at a given temperature.

Amplifier 64 amplifies the difference between voltages V_{YA} and V_{RA} to produce an amplified voltage V_{ZA} that gradually changes from high level V_{ZD} to low level V_{ZC} as V_{YA} passes V_{RA} . Amplifier 66 amplifies the difference between voltage V_{YB} and V_{RB} to produce an amplified voltage V_{ZB} that gradually changes from V_{ZC} to V_{ZD} as V_{YB} passes V_{RB} . Figs. 9a and 9b respectively show how voltages V_{ZA} and V_{ZB} basically vary. Transition zones 70 and 72 in Figs. 9a and 9b are typically 100 millivolts in width.

Generator 68 supplies (a) control voltage V_{CL} as the linear AND of voltages V_{ZA} and V_{ZB} and (b) control voltage V_{CH} as the linear NAND of voltages V_{ZA} and V_{ZB} . Referring to Fig. 10, the top curve depicts how voltage V_{CL} varies between low level V_{CLC} and high level V_{CLD} as a function of V_{CM} .

Transition zones 70 and 72 for V_{ZA} and V_{ZB} are reflected in V_{CL} as respective transition zones 74 and 76. The centres of zones 74 and 76 are respectively "referenced" to V_{LL} and V_{HH} . That is, the center of zone 74 is separated from V_{LL} by a voltage spacing V_{CLL} that is largely constant at a given temperature. The center of zone 76 is similarly separated from V_{HH} by a voltage spacing that is largely constant at a given temperature. As a consequence, the separation between zones 74 and 76 varies inversely with V_{PS} .

Fig. 10 indicates that the V_{CL} curve has a flat portion 78 situated between zones 74 and 76. It is usually preferably that zones 74 and 76 meet so that portion 78 compresses to a point. If zones 74 and 76 do so meet, an increase in V_{PS} causes zones 74 and 76 to merge into each other. High level V_{CLD} decreases in value. Typical level shift V_{LSI} vary when control voltage V_{CL} (or V_{CH}) has the indicated variation. Zones 74 and 76 are reflected directly in the I_{SI} and V_{LSI} curves. If a sufficient increase in V_{PS} causes zones 74 and 76 to merge, high levels I_{SM} and V_{LSM} for the I_{SI} and V_{LSI} curves usually decrease. In this way, the level-shift circuit gradually shuts off as V_{PS} rises.

Moving to Fig. 11, it shows an embodiment of Fig. 6 in which amplifiers A1 - A4 are formed with bipolar transistors Q1 - Q4 arranged the same as in Fig. 1. Level shifts 38 - 44 are embodied with resistors R1, R2, R3, and R4 in Fig. 11. Common-mode generator 54 of Fig. 8 is implemented with components 30, 32, 34, and R1 - R4 in Fig. 11. These components in combination with current supply 56 form a level-shift feedback control loop. Finally, current sources 58 of Fig. 8 are implemented with variable current sources S1, S2, S3, and S4 in Fig. 11. Signal V_{CH} controls current sources S1 and S2, while signal V_{CL} controls current

sources S3 and S4.

In Fig. 11, V_{MA} equals $V_{BE} + V_{SAT}$ when main supply 34 is implemented with the circuitry of Fig. 4a or 4b. For the optimum case in which V_{RP} equals $V_{HH} - V_{MB}$ in Fig. 4b, the same applies to V_{MB} . The minimum voltage across each of current sources S1 - S4 when they are fully conductive is $1V_{SAT}$. Since each spacing V_{SATL} or V_{SATH} thereby equals $1V_{SAT}$, V_{PSS} equals $V_{BE} + 2V_{SAT}$. Using the above values of 0.6 volt for V_{BE} and 0.1 volt for V_{SAT} , V_{PSF} is approximately 0.8 volt.

Fig. 12 depicts a preferred way for implementing current control 56 in Fig. 11. The circuitry in Fig. 12 differs from current control 56 in Fig. 8 in that the circuit of Fig. 12 employs a differential amplifier 78 to perform the functions of components 66 and 68 in Fig. 8. Amplifier 78 amplifies the difference between voltages V_{YB} and V_{RB} just as amplifier 66 does in Fig. 8. However, amplifier 78 has a gain control terminal that receives voltage V_{ZA} from amplifier 64. This allows amplifier 78 to produce control voltages V_{CL} and V_{CH} in much the same way as shown in Fig. 10.

Figs. 13a - 13c indicate the manner in which level-shift voltage V_{LSI} preferably varies as a function of V_{CM} for the differential amplifier of Fig. 11 when implemented with current control 56 of Fig. 8 or 12. For the case illustrated in Figs. 13a - 13c, resistors R1 - R4 all have the same resistance. Fig. 13a depicts the basic situation at standard temperature and 1.0-volt V_{PS} . Fig. 13b illustrates how the level-shift circuit gradually "turns off" as V_{PS} increases. No level shifting is needed when V_{PS} is at or above 1.4 volts. As indicated in Fig. 13c, the level-shift circuit also automatically increases V_{LSI} with decreasing temperature, and vice versa, to provide temperature compensation.

Figs. 14a and 14b graphically show the idealized operational regions that arise for the differential amplifier of Fig. 11 when main current supply 34 is respectively embodied with the circuitry of Figs. 4a and 4b. In Fig. 14a, the merged portion of lines 20A and 20B lying between V_{PSO} and V_{PSF} is equally separated from V_{LL} and V_{HH} . The same applies to the portion of line 20 located between V_{PFO} and V_{PSF} in Fig. 14b.

A preferred bipolar embodiment for the present differential amplifier is shown in Fig. 15. Subject to the following comments, the elements used in Fig. 15 to implement the components of the amplifier of Fig. 11 can be determined by inspection. Main supply 34 is implemented with the circuit of Fig. 4b. Consequently, the transconductance of the amplifier in Fig. 15 is largely constant. A voltage reference source 80 supplies reference voltage V_{RP} at a value lower than voltage V_{HH} by an amount V_{KP} that is largely constant at a given temperature. For supply 34 to operate optimally, V_{KP} equals $V_{BE} + V_{SAT}$. That is, V_{RP} equals $V_{HH} - V_{BE} - V_{SAT}$.

Current control 56 in Fig. 15 uses the arrangement shown in Fig. 12. Based on what has been said

above about Fig. 12, a detailed understanding of the various circuit elements in control 56 should be evident to a skilled artisan. Resistors R1 - R4 introduce an extra frequency pole. Capacitors C1, C2, C3, and C4 provide frequency compensation by introducing a frequency zero at approximately the same location as the extra pole.

Fig. 16 illustrates two ways for implementing voltage reference sources 60, 62, and 80. Using only the circuit elements shown in solid line, V_{RB} and V_{RP} are separated from V_{HH} by relatively constant amounts at a given temperature. However, it is usually desirable to employ portion 30 over more of the V_{PS} range than portion 32 because NPN transistors require less base current than PNP transistors. This objective can be reached by using the entire circuitry (both solid line and dashed line) shown in Fig. 16. The full circuitry in Fig. 16 also avoid Zener problems that NPN components 30 and 78 might otherwise encounter. In this case, Fig. 17 illustrates the resulting idealized operational regions. The level-shift circuit shuts off when V_{PS} goes above 1.6 volts.

As indicated above, the level-shift circuit normally shuts off when V_{PS} rises. Nonetheless, there may be some applications in which the level-shift circuit should remain fully on as V_{PS} is increased. Figs. 18a and 18b indicate how level shift V_{LS1} would vary with V_{CM} in such an application for the case in which main supply 34 is implemented with the circuit of Fig. 4a. The basic variation at a 1.0-volt V_{PS} is shown in Fig. 18a. Fig. 18b illustrates what happens as V_{PS} is raised. Fig. 19 shows the resulting idealized operational regions.

In the embodiments of the invention variously illustrated in Figs. 8 - 19, supply currents $I_{S1} - I_{S4}$ are all approximately equal. Consequently, portion 30 receives a level shift when portion 32 receives a level shift, and vice versa. The level shifts received by portions 30 and 32 are normally close to the same value.

Fig. 20 depicts an embodiment of Fig. 6 in which the level shifts supplied to portions 30 and 32 are largely independent of each other. This is achieved by using four additional variable current sources S5, S6, S7, and S8 arranged as indicated in Fig. 20. Sources S1, S2, S7, and S8 fix the level shift for portion 30. Sources S3 - S6 similarly fix the level shift for portion 32.

In addition to control voltages V_{CL} and V_{CH} , current control 56 in Fig. 20 supplies control voltages $V_{CL'}$ and $V_{CH'}$. Signals V_{CH} and $V_{CL'}$ are generated at complementary values to control the level shift for portion 30. Signals V_{CL} and $V_{CH'}$ are likewise supplied at complementary values to control the level shift for portion 32. However, signals V_{CL} and $V_{CH'}$ do not necessarily track signals V_{CH} and $V_{CL'}$.

While the invention has been described with reference to particular embodiments, this is solely for the purpose of illustration and is not to be construed

as limiting the scope of the invention claimed below. For example, the level shifts might be implemented with Schottky diodes to improve the noise behavior. Thus, various modifications and applications may be made by those skilled in the art without departing from the true scope of the invention as defined in the appended claims.

Claims

1. An electronic circuit for amplifying a circuit input signal differentially provided between first (T1) and second (T2) input terminals as respective first (V_{I1}) and second (V_{I2}) input voltages, the circuit comprising:

main supply means (34), coupled between respective sources of a high supply voltage V_{HH} and a low supply voltage V_{LL} whose difference is a power supply voltage V_{PS} that defines a power supply range, for providing opposite first (I_A) and second (I_B) operating currents;

first means (30) for amplifying the voltage difference between first (P1) and second (P2) input points by largely dividing the first operating current (I_A) into a pair of amplified first internal signals, the first (P1) and second (P2) input points being respectively coupled to the first (T1) and second (T2) input terminals, the first means (30) being operatively conductive to so produce the first internal signals when the common-mode voltage V_{CM} of the circuit input signal is in a portion of the supply range extending up to V_{HH} ;

second means (32) for amplifying the voltage difference between third (P3) and fourth (P4) input points by largely dividing the second operating current (I_B) into a pair of amplified second internal signals, the third (P3) and fourth (P4) input points being respectively coupled to the first (T1) and second (T2) input terminals, the second means (32) being operatively conductive to so produce the second internal signals when V_{CM} is in a portion of the supply range extending down to V_{LL} such that at least one of the differential means is operatively conductive as V_{CM} traverses substantially the entire supply range when V_{PS} is greater than or equal to a specified minimum level; and

summing means (36) for combining the internal signals to generate at least one circuit output signal (I_O); characterized in that the circuit further comprises:

level-shift means (38,40,42,44) for selectively causing the voltages at the first (P1) and second (P2) input points to be respectively higher than the first and second input voltages by respective first (38) and second (40) voltage level

above about Fig. 12, a detailed understanding of the various circuit elements in control 56 should be evident to a skilled artisan. Resistors R1 - R4 introduce an extra frequency pole. Capacitors C1, C2, C3, and C4 provide frequency compensation by introducing a frequency zero at approximately the same location as the extra pole.

Fig. 16 illustrates two ways for implementing voltage reference sources 60, 62, and 80. Using only the circuit elements shown in solid line, V_{RB} and V_{RP} are separated from V_{HH} by relatively constant amounts at a given temperature. However, it is usually desirable to employ portion 30 over more of the V_{PS} range than portion 32 because NPN transistors require less base current than PNP transistors. This objective can be reached by using the entire circuitry (both solid line and dashed line) shown in Fig. 16. The full circuitry in Fig. 16 also avoid Zener problems that NPN components 30 and 78 might otherwise encounter. In this case, Fig. 17 illustrates the resulting idealized operational regions. The level-shift circuit shuts off when V_{PS} goes above 1.6 volts.

As indicated above, the level-shift circuit normally shuts off when V_{PS} rises. Nonetheless, there may be some applications in which the level-shift circuit should remain fully on as V_{PS} is increased. Figs. 18a and 18b indicate how level shift V_{LSI} would vary with V_{CM} in such an application for the case in which main supply 34 is implemented with the circuit of Fig. 4a. The basic variation at a 1.0-volt V_{PS} is shown in Fig. 18a. Fig. 18b illustrates what happens as V_{PS} is raised. Fig. 19 shows the resulting idealized operational regions.

In the embodiments of the invention variously illustrated in Figs. 8 - 19, supply currents $I_{S1} - I_{S4}$ are all approximately equal. Consequently, portion 30 receives a level shift when portion 32 receives a level shift, and vice versa. The level shifts received by portions 30 and 32 are normally close to the same value.

Fig. 20 depicts an embodiment of Fig. 6 in which the level shifts supplied to portions 30 and 32 are largely independent of each other. This is achieved by using four additional variable current sources S5, S6, S7, and S8 arranged as indicated in Fig. 20. Sources S1, S2, S7, and S8 fix the level shift for portion 30. Sources S3 - S6 similarly fix the level shift for portion 32.

In addition to control voltages V_{CL} and V_{CH} , current control 56 in Fig. 20 supplies control voltages $V_{CL'}$ and $V_{CH'}$. Signals V_{CH} and $V_{CL'}$ are generated at complementary values to control the level shift for portion 30. Signals V_{CL} and $V_{CH'}$ are likewise supplied at complementary values to control the level shift for portion 32. However, signals V_{CL} and $V_{CH'}$ do not necessarily track signals V_{CH} and $V_{CL'}$.

While the invention has been described with reference to particular embodiments, this is solely for the purpose of illustration and is not to be construed

as limiting the scope of the invention claimed below. For example, the level shifts might be implemented with Schottky diodes to improve the noise behavior. Thus, various modifications and applications may be made by those skilled in the art without departing from the true scope of the invention as defined in the appended claims.

Claims

1. An electronic circuit for amplifying a circuit input signal differentially provided between first (T1) and second (T2) input terminals as respective first (V_{I1}) and second (V_{I2}) input voltages, the circuit comprising:

main supply means (34), coupled between respective sources of a high supply voltage V_{HH} and a low supply voltage V_{LL} whose difference is a power supply voltage V_{PS} that defines a power supply range, for providing opposite first (I_A) and second (I_B) operating currents;

first means (30) for amplifying the voltage difference between first (P1) and second (P2) input points by largely dividing the first operating current (I_A) into a pair of amplified first internal signals, the first (P1) and second (P2) input points being respectively coupled to the first (T1) and second (T2) input terminals, the first means (30) being operatively conductive to so produce the first internal signals when the common-mode voltage V_{CM} of the circuit input signal is in a portion of the supply range extending up to V_{HH} ;

second means (32) for amplifying the voltage difference between third (P3) and fourth (P4) input points by largely dividing the second operating current (I_B) into a pair of amplified second internal signals, the third (P3) and fourth (P4) input points being respectively coupled to the first (T1) and second (T2) input terminals, the second means (32) being operatively conductive to so produce the second internal signals when V_{CM} is in a portion of the supply range extending down to V_{LL} such that at least one of the differential means is operatively conductive as V_{CM} traverses substantially the entire supply range when V_{PS} is greater than or equal to a specified minimum level; and

summing means (36) for combining the internal signals to generate at least one circuit output signal (I_O);

characterized in that the circuit further comprises:

level-shift means (38,40,42,44) for selectively causing the voltages at the first (P1) and second (P2) input points to be respectively higher than the first and second input voltages by respective first (38) and second (40) voltage level



shifts and for selectively causing the voltages at the third (P3) and fourth (P4) input points to be respectively lower than the first and second input voltages by respective third (42) and fourth (44) voltage level shifts.

2. A circuit as claimed in Claim 1, characterized in that the level shifts (38,40,42,44) are provided at values adequate to reduce the specified minimum level of V_{PS} to a value below that which would occur if (a) the voltages at the first (P1) and third (P3) input points were always substantially equal to the first input voltage and (b) the voltages at the second (P2) and fourth (P4) input points were always substantially equal to the second input voltage.
3. A circuit as claimed in Claim 2, characterized in that the first means (30) is operatively conductive when the magnitude of the difference between V_{LL} and the common-mode portion V_{CMA} of the voltages at the first (P1) and second (P2) input points is greater than or equal to a first threshold voltage V_{TA} which can vary with V_{PS} ; and the second means (32) is operatively conductive when the magnitude of the difference between V_{HH} and the common-mode portion V_{CMB} of the voltages at the third (P3) and fourth (P4) input points is greater than or equal to a second threshold voltage V_{TB} which can vary with V_{PS} ; characterized in that (a) the first (38) and second (40) voltage level shifts are provided at values greater than or equal to $V_{TA} - V_{CM} + V_{LL}$ but less than $V_{HH} - V_{CM}$ and (b) the third (42) and fourth (44) voltage level shifts are provided at values greater than or equal to $V_{TB} + V_{CM} - V_{HH}$ but less than $V_{CM} - V_{LL}$.
4. A circuit as claimed in Claim 3, characterized in that V_{TA} and V_{TB} have respective minimum values V_{MA} and V_{MB} , characterized in that the value of the specified minimum level of V_{PS} is less than $V_{MA} + V_{MB}$.
5. A circuit as claimed in Claim 4, characterized in that the value of the specified minimum level for V_{PS} is greater than the larger of V_{MA} and V_{MB} .
6. A circuit as claimed in Claim 3, characterized in that (a) the first (38) and second (40) voltage level shifts are largely equal and (b) the third (42) and fourth (44) voltage level shifts are largely equal.
7. A circuit as claimed in any of the preceding Claims, characterized in that the level-shift means comprises:

network means, coupled between the input terminals (T1, T2) and the input points, (P1,P2,P3,P4) for providing the level shifts; and

level-shift supply means (46) for providing current to the network means to control the values of the level shifts.

8. A circuit as claimed in Claim 7, characterized in that the network means comprises a first level-shift element (R1) coupled between the first input terminal (T1) and the first input point (P1), a second level-shift element (R2) coupled between the second input terminal (T2) and the second input point (P2), a third level-shift element (R3) coupled between the first input terminal (T1) and the third input point (P3), and a fourth level-shift element (R4) coupled between the second input terminal (T2) and the fourth input point (P4).
9. A circuit as claimed in Claim 8, characterized in that each level-shift element comprises a resistor.
10. A circuit as claimed in Claim 8, characterized in that the level-shift supply means comprises a first current source (S1) coupled between the first input point (P1) and the V_{HH} source, a second current source (S2) coupled between the second input point (P2) and the V_{HH} source, a third current source (S3) coupled between the third input point (P3) and the V_{LL} source, a fourth current source (S4) coupled between the fourth input point (P4) and the V_{LL} source, and control means (56) for controlling conduction of the current sources.
11. A circuit as claimed in Claim 10, characterized in that the level-shift supply means (46) further includes a fifth current source (S5) coupled between the first input terminal (T1) and the V_{HH} source, a sixth current source (S6) coupled between the second input terminal (T2) and the V_{HH} source, a seventh current source (S7) coupled between the first input terminal (T1) and the V_{LL} source, and an eighth current source (S8) coupled between the second input terminal (T2) and the V_{LL} source.
12. A circuit as claimed in Claim 10 or 11, characterized in that each current source (S1...S8) provides progressively less current as the power supply voltage V_{PS} rises so as to gradually turn off the level-shift means.
13. A circuit as claimed in Claim 10, characterized in that the control means (56) provides at least part of the current sources with a control signal (V_{CH}, V_{CL}) that, as a function of V_{CH} when V_{PS} is sufficiently low, gradually changes (a) from a first control level to a second control level in a first voltage transition zone referenced to V_{HH} and (b)



from the second control level back to the first control level in a second voltage transition zone referenced to V_{LL} .

14. A circuit as claimed in Claim 13, characterized in that the voltage transition zones meet each other. 5
15. A circuit as claimed in Claim 14, characterized in that the voltage transition zones shrink in size as V_{PS} increases so that the difference between the two control levels decreases. 10
16. A circuit as claimed in Claim 13, characterized in that the control means (56) (a) supplies the first control signal (V_{CH}) to the first (S1) and second (S2) current sources, (b) generates a second control (V_{CL}) signal having largely the opposite variation as the first control signal, and (c) supplies the second control signal to the third (S3) and fourth (S4) current sources. 15
17. A circuit as claimed in Claim 13, characterized in that the control means (56) comprises:
generating means (54) responsive to the input voltages for producing first and second operating voltages that bear specific relationships to V_{CM} ; 20
first reference means (62) for supplying a first reference voltage that is referenced to V_{LL} at least when V_{PS} is sufficiently small; 25
second reference means (64) for supplying a second reference voltage that is referenced to V_{HH} at least when V_{PS} is sufficiently small; and
linear means (64,66) responsive to the operating voltages and the reference voltages for producing the first control signal. 30
18. A circuit as claimed in Claim 17, characterized in that the linear means (64,66) comprises:
a first amplifying section (66) for amplifying the difference between the first operating voltage and the first reference voltage to produce a first amplified voltage; 35
a second amplifying section (64) for amplifying the difference between the second operating voltage and the second reference voltage to produce a second amplified voltage; and
AND/NAND means (68) for generating the first control signal largely as either the linear AND of the amplified voltages or the linear NAND of the amplified voltages. 40
19. A circuit as claimed in Claim 17, characterized in that the linear means comprises:
a first amplifying section (64) for amplifying the difference between the first operating voltage and the first reference voltage to produce a first amplified voltage; and 45

a second amplifying section (78) having a gain control terminal responsive to the first amplified voltage for amplifying the difference between the second operating voltage and the second reference voltage to produce the first control signal.

20. A circuit as claimed in Claim 17, characterized in that the generating means (54) comprises the level-shift elements, both differential means (30,32), and the main supply means (34). 50
21. A circuit as claimed in Claim 20, characterized in that the first and second operating voltages are largely the voltages at which the first and second operating currents are respectively supplied. 55
22. A circuit as claimed in any preceding Claim, characterized in that the first internal signals are differentially representative of the circuit input signal when the first means (30) is operatively conductive; and the second internal signals are differentially representative of the circuit input signal when the second means (32) is operatively conductive. 60
23. A circuit as claimed in any preceding Claim, characterized in that each of the first and second (30,32) means comprises a pair of like-configured amplifiers, each amplifier having a first flow electrode, a second flow electrode, and a control electrode for regulating current transmission between the flow electrodes, the amplifiers (Q1,Q2) in the first means (30) having (a) their control electrodes respectively coupled to the first (P1) and second (P2) input points, (b) their first electrodes coupled together to receive the first operating current (I_A), and (c) their second electrodes respectively coupled to the summing means (36) to supply the first internal currents, the amplifiers (Q3,Q4) in the second means (32) having (a) their control electrodes respectively coupled to the third (P3) and fourth (P4) input points (b) their first electrodes coupled together to receive the second operating current (I_B), and (c) their second electrodes coupled to the summing means (36) to supply the second internal current, the amplifiers (Q3,Q4) in the second means (32) being complementary to the amplifiers (Q1,Q2) in the first means (30). 65
24. A circuit as in Claim 23, characterized in that charge carriers that move between the flow electrodes of each amplifier originate at its first electrode and terminate at its second electrode. 70
25. A circuit as in Claim 24, characterized in that each amplifier is a bipolar transistor having an emitter, 75



a collector, and a base respectively coupled to the first, second, and control electrodes of that amplifier.

Patentansprüche

1. Elektronische Schaltung zur Verstärkung eines Schaltungs-Eingangssignals, das differentiell zwischen einem ersten (T1) und einem zweiten Eingangsanschluß (T2) als erste (V_{11}) bzw. als zweite Eingangsspannung (V_{12}) anliegt, wobei die Schaltung folgendes enthält:

eine Hauptstromversorgung (34), die zwischen die jeweiligen Quellen einer hohen Versorgungsspannung V_{HH} und einer niedrigen Versorgungsspannung V_{LL} geschaltet ist, deren Differenz eine Versorgungsspannung V_{PS} ist, die einen Versorgungsspannungsbereich definiert, um einen ersten (I_A) und einen zweiten Arbeitsstrom (I_B) zu liefern, die einander entgegengesetzt sind;

erste Mittel (30) zum Verstärken der Spannungsdifferenz zwischen dem ersten (P1) und dem zweiten Eingangspunkt (P2) durch weitgehendes Aufteilen des ersten Arbeitsstroms (I_A) in ein Paar verstärkter erster interner Signale, wobei der erste (P1) und der zweite Eingangspunkt (P2) mit einem ersten (T1) bzw. mit einem zweiten Eingangsanschluß (T2) verbunden sind, und wobei die ersten Mittel (30) im Betrieb leitend sind, um somit die ersten internen Eingangssignale zu erzeugen, wenn die Gleichtaktspannung V_{CM} des Schaltungs-Eingangssignals in einem Teil des Versorgungsbereiches liegt, der sich bis V_{HH} erstreckt;

zweite Mittel (32) zum Verstärken der Spannungsdifferenz zwischen dem dritten (P3) und dem vierten Eingangspunkt (P4) durch weitgehendes Aufteilen des zweiten Arbeitsstroms (I_B) in ein Paar verstärkter zweiter interner Signale, wobei der dritte (P3) und der vierte Eingangspunkt (P4) mit dem ersten (T1) bzw. mit dem zweiten Eingangsanschluß (T2) verbunden sind, und wobei die zweiten Mittel (32) im Betrieb leitend sind, um somit die zweiten internen Signale zu erzeugen, wenn V_{CM} in einem Teil des Versorgungsbereiches liegt, der sich bis V_{LL} erstreckt, so daß mindestens eines der differentiellen Mittel im Betrieb leitend ist, wenn V_{CM} im wesentlichen den gesamten Versorgungsbereich durchquert, wenn V_{PS} größer oder gleich einem spezifizierten Mindestpegel ist; und

Summiermittel (36) zum Kombinieren der internen Signale, um mindestens ein Schaltungs-Ausgangssignal (I_O) zu erzeugen; dadurch gekennzeichnet, daß die Schaltung weiterhin folgendes umfaßt:

Pegelverschiebungsmittel (38, 40, 42, 44),

um selektiv dafür zu sorgen, daß die Spannungen an dem ersten (P1) und an dem zweiten Eingangspunkt (P2) höher als die erste bzw. die zweite Eingangsspannung sind, und zwar durch entsprechende Pegelverschiebungen der ersten (38) und der zweiten Spannung (40), und um selektiv dafür zu sorgen, daß die Spannungen an dem dritten (P3) und an dem vierten Eingangspunkt (P4) niedriger als die erste bzw. die zweite Eingangsspannung sind, und zwar durch entsprechende Pegelverschiebungen der dritten (42) und der vierten Spannung (44).

2. Schaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Pegelverschiebungen (38, 40, 42, 44) mit Werten geschaffen werden, die geeignet sind, um den minimalen Pegel von V_{PS} auf einen Wert zu reduzieren, der kleiner ist als derjenige, welcher vorliegen würde, wenn (a) die Spannungen an dem ersten (P1) und an dem dritten Eingangspunkt (P3) immer im wesentlichen gleich der ersten Eingangsspannung wären und wenn (b) die Spannungen an dem zweiten (P2) und an dem vierten Eingangspunkt (P4) immer im wesentlichen gleich der zweiten Eingangsspannung wären.
3. Schaltung nach Anspruch 2, dadurch gekennzeichnet, daß das erste Mittel (30) im Betrieb leitend ist, wenn die Größe der Differenz zwischen V_{LL} und dem Gleichtaktanteil V_{CMA} der Spannungen an dem ersten (P1) und an dem zweiten Eingangspunkt (P2) größer oder gleich einer ersten Schwellenspannung V_{TA} ist, die mit V_{PS} schwanken kann; und daß das zweite Mittel (32) im Betrieb leitend ist, wenn die Größe der Differenz zwischen V_{HH} und dem Gleichtaktanteil V_{CMB} der Spannungen an dem dritten (P3) und an dem vierten Eingangspunkt (P4) größer oder gleich einer zweiten Schwellenspannung V_{TB} ist, die mit V_{PS} schwanken kann; dadurch gekennzeichnet, daß (a) die erste (38) und die zweite Spannungspegelverschiebung (40) mit Werten geschaffen werden, die größer oder gleich $V_{TA} - V_{CM} + V_{LL}$ sind, aber kleiner als $V_{HH} - V_{CM}$ und daß (b) die dritte (42) und die vierte Spannungspegelverschiebung (44) mit Werten geschaffen werden, die größer oder gleich $V_{TB} + V_{CM} - V_{HH}$ sind, aber kleiner als $V_{CM} - V_{LL}$.
4. Schaltung nach Anspruch 3, dadurch gekennzeichnet, daß V_{TA} und V_{TB} die Mindestwerte V_{MA} bzw. V_{MB} haben, die dadurch gekennzeichnet sind, daß der Wert des spezifizierten Mindestpegels von V_{PS} kleiner ist als $V_{MA} + V_{MB}$.
5. Schaltung nach Anspruch 4, dadurch gekennzeichnet, daß der Wert des spezifizierten Min-



destpegels für V_{PS} größer ist als der größere der Werte V_{MA} und V_{MB} .

6. Schaltung nach Anspruch 3, dadurch gekennzeichnet, daß (a) die erste (38) und die zweite Spannungspegelverschiebung (40) weitgehend gleich sind und daß (b) die dritte (42) und die vierte Spannungspegelverschiebung (44) weitgehend gleich sind.
7. Schaltung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß das Pegelverschiebungsmittel folgendes enthält:
Netzwerkmittel, das zwischen die Eingangsanschlüsse (T1, T2) und die Eingangspunkte (P1, P2, P3, P4) geschaltet ist, um für die Pegelverschiebungen zu sorgen; und
Pegelverschiebungs-Versorgungsmittel (46) zum Liefern des Stroms an das Netzwerkmittel, um die Werte der Pegelverschiebungen zu steuern.
8. Schaltung nach Anspruch 7, dadurch gekennzeichnet, daß das Netzwerkmittel ein erstes Pegelverschiebungselement (R1) enthält, das zwischen den ersten Eingangsanschluß (T1) und den ersten Eingangspunkt (P1) geschaltet ist, ein zweites Pegelverschiebungselement (R2), das zwischen den zweiten Eingangsanschluß (T2) und den zweiten Eingangspunkt (P2) geschaltet ist, ein drittes Pegelverschiebungselement (R3), das zwischen den ersten Eingangsanschluß (T1) und den dritten Eingangspunkt (P3) geschaltet ist, und ein viertes Pegelverschiebungselement (R4), das zwischen den zweiten Eingangsanschluß (T2) und den vierten Eingangspunkt (P4) geschaltet ist.
9. Schaltung nach Anspruch 8, dadurch gekennzeichnet, daß jedes Pegelverschiebungselement einen Widerstand enthält.
10. Schaltung nach Anspruch 8, dadurch gekennzeichnet, daß das Pegelverschiebungs-Versorgungsmittel eine erste Stromquelle (S1) enthält, die zwischen den ersten Eingangspunkt (P1) und die V_{HH} -Quelle geschaltet ist, eine zweite Stromquelle (S2), die zwischen den zweiten Eingangspunkt (P2) und die V_{HH} -Quelle geschaltet ist, eine dritte Stromquelle (S3), die zwischen den dritten Eingangspunkt (P3) und die V_{LL} -Quelle geschaltet ist, eine vierte Stromquelle (S4), die zwischen den vierten Eingangspunkt (P4) und die V_{LL} -Quelle geschaltet ist, und ein Steuermittel (56) zum Steuern der Leitung der Stromquellen.
11. Schaltung nach Anspruch 10, dadurch gekennzeichnet, daß das Pegelverschiebungs-

Versorgungsmittel (46) weiterhin eine fünfte Stromquelle (S5) enthält, die zwischen den ersten Eingangsanschluß (T1) und die V_{HH} -Quelle geschaltet ist, eine sechste Stromquelle (S6), die zwischen den zweiten Eingangsanschluß (T2) und die V_{HH} -Quelle geschaltet ist, eine siebente Stromquelle (S7), die zwischen den ersten Eingangsanschluß (T1) und die V_{LL} -Quelle geschaltet ist, und eine achte Stromquelle (S8), die zwischen den zweiten Eingangspunkt (T2) und die V_{LL} -Quelle geschaltet ist.

12. Schaltung nach Anspruch 10 oder 11, dadurch gekennzeichnet, daß jede Stromquelle (S1 ... S8) immer weniger Strom liefert, wenn die Versorgungsspannung V_{PS} ansteigt, um somit die Pegelverschiebungsmittel nach und nach auszu-schalten.

13. Schaltung nach Anspruch 10, dadurch gekennzeichnet, daß das Steuermittel (56) zumindest einen Teil der Stromquellen mit einem Steuersignal (V_{CM} , V_{CL}) versorgt, das in Abhängigkeit von V_{CM} , wenn V_{PS} genügend niedrig ist, allmählich (a) von einem ersten Steuerpegel auf einen zweiten Steuerpegel in einer ersten Spannungs-Übergangszone wechselt, die auf V_{HH} bezogen ist, und (b) von einem zweiten Steuerpegel zurück zu dem ersten Steuerpegel in einer zweiten Spannungs-Übergangszone wechselt, die auf V_{LL} bezogen ist.

14. Schaltung nach Anspruch 13, dadurch gekennzeichnet, daß die Spannungs-Übergangszonen einander berühren.

15. Schaltung nach Anspruch 14, dadurch gekennzeichnet, daß die Größe der Spannungs-Übergangszonen abnimmt, wenn V_{PS} ansteigt, so daß die Differenz zwischen den beiden Steuerpegeln kleiner wird.

16. Schaltung nach Anspruch 13, dadurch gekennzeichnet, daß das Steuermittel (56) (a) das erste Steuersignal (V_{CM}) der ersten (S1) und der zweiten Stromquelle (S2) zuführt, (b) ein zweites Steuersignal (V_{CL}) erzeugt, das weitgehend entgegengesetzt zum ersten Steuersignal schwankt, und (d) das zweite Steuersignal der dritten (S3) und der vierten Stromquelle (S4) zuführt.

17. Schaltung nach Anspruch 13, dadurch gekennzeichnet, daß das Steuermittel (56) folgendes umfaßt:

Erzeugungsmittel (54), die auf die Eingangsspannungen reagieren, um eine erste und eine zweite Arbeitsspannung zu erzeugen, die in



einem bestimmten Zusammenhang mit V_{CM} stehen;

erste Referenzmittel (62) zum Liefern einer ersten Referenzspannung, die auf V_{LL} bezogen ist, zumindest wenn V_{PS} ausreichend klein ist;

zweite Referenzmittel (64) zum Liefern einer zweiten Referenzspannung, die auf V_{HH} bezogen ist, zumindest wenn V_{PS} ausreichend klein ist;

lineare Mittel (64, 66), das auf die Arbeitsspannungen und die Referenzspannungen reagiert, um das erste Steuersignal zu erzeugen.

18. Schaltung nach Anspruch 17, dadurch gekennzeichnet, daß das lineare Mittel (64, 66) folgendes enthält:

einen ersten verstärkenden Teil (66) zur Verstärkung der Differenz zwischen der ersten Arbeitsspannung und der ersten Referenzspannung, um eine erste verstärkte Spannung zu erzeugen;

einen zweiten verstärkenden Teil (64) zur Verstärkung der Differenz zwischen der zweiten Arbeitsspannung und der zweiten Referenzspannung, um eine zweite verstärkte Spannung zu erzeugen; und

UND/NICHT-UND-Mittel (68) zum Erzeugen des ersten Steuersignals im wesentlichen entweder als lineare UND-Verknüpfung der verstärkten Spannungen oder als lineare NICHT-UND-Verknüpfung der verstärkten Spannungen.

19. Schaltung nach Anspruch 17, dadurch gekennzeichnet, daß das lineare Mittel folgendes enthält:

einen ersten verstärkenden Teil (64) zur Verstärkung der Differenz zwischen der ersten Arbeitsspannung und der ersten Referenzspannung, um eine erste verstärkte Spannung zu erzeugen; und

einen zweiten verstärkenden Teil (78) mit einem Verstärkungs-Steueranschluß, der auf die erste verstärkte Spannung reagiert, zur Verstärkung der Differenz zwischen der zweiten Arbeitsspannung und der zweiten Referenzspannung, um das erste Steuersignal zu erzeugen.

20. Schaltung nach Anspruch 17, dadurch gekennzeichnet, daß das Erzeugungsmittel (54) die Pegelverschiebungselemente, beide differentiellen Mittel (30, 32) und das Hauptversorgungsmittel (34) enthält.

21. Schaltung nach Anspruch 20, dadurch gekennzeichnet, daß die erste und die zweite Arbeitsspannung im wesentlichen die Spannungen sind, bei denen der erste bzw. der zweite Arbeitsstrom

geliefert werden.

22. Schaltung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die ersten internen Signale differentiell für das Schaltungs-Eingangssignal repräsentativ sind, wenn das erste Mittel (30) im Betrieb leitend ist; und daß die zweiten internen Signale differentiell für das Schaltungs-Eingangssignal repräsentativ sind, wenn das zweite Mittel (32) im Betrieb leitend ist.

23. Schaltung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß jedes von dem ersten und dem zweiten Mittel (30, 32) ein Paar gleich konfigurierte Verstärker enthält, wobei jeder Verstärker eine erste Leitungselektrode, eine zweite Leitungselektrode und eine Steuerelektrode zur Regulierung der Stromübertragung zwischen den Leitungselektroden besitzt, (a) die Steuerelektroden der Verstärker (Q1, Q2) in dem ersten Mittel (30) mit dem ersten (P1) bzw. mit dem zweiten Eingangspunkt (P2) verbunden sind, (b) die ersten Elektroden dieser Verstärker (Q1, Q2) miteinander verbunden sind, um den ersten Arbeitsstrom (I_A) zu erhalten, und (c) die zweiten Elektroden dieser Verstärker (Q1, Q2) mit dem Summierungsmittel (36) verbunden sind, um die ersten internen Ströme zu liefern, und wobei (a) die Steuerelektroden der Verstärker (Q3, Q4) in dem zweiten Mittel (32) mit dem dritten (P3) bzw. mit dem vierten Eingangspunkt (P4) verbunden sind, (b) die ersten Elektroden dieser Verstärker (Q3, Q4) miteinander verbunden sind, um den zweiten Arbeitsstrom (I_B) zu erhalten, und (c) die zweiten Elektroden dieser Verstärker (Q3, Q4) mit dem Summierungsmittel (36) verbunden sind, um den zweiten internen Strom zu liefern, wobei die Verstärker (Q3, Q4) in dem zweiten Mittel (32) komplementär zu den Verstärkern (Q1, Q2) in dem ersten Mittel (30) sind.

24. Schaltung nach Anspruch 23, dadurch gekennzeichnet, daß Ladungsträger, die sich zwischen den Leitungselektroden jedes Verstärkers bewegen, ihren Ursprung bei seiner ersten Leitungselektrode haben und ihr Ziel bei seiner zweiten Leitungselektrode erreichen.

25. Schaltung nach Anspruch 24, dadurch gekennzeichnet, daß jeder Verstärker ein Bipolartransistor mit einem Emitter, einem Kollektor und einer Basis ist, die mit der ersten und der zweiten Leitungselektrode bzw. mit der Steuerelektrode dieses Verstärkers verbunden sind.



Revendications

1. Circuit électronique pour l'amplification d'un signal d'entrée fourni de manière différentielle entre une première (T1) et une seconde (T2) borne d'entrée, respectivement, comme première (V_{11}) et seconde (V_{12}) tension d'entrée, le circuit comprenant :
 - une alimentation principale (34), couplée entre des sources respectives d'une tension haute V_{HH} et d'une tension basse V_{LL} , dont la différence est une tension d'alimentation V_{PS} qui définit une plage de tensions d'alimentation, pour la fourniture d'un premier (I_A) et d'un second (I_B) courant de fonctionnement opposés;
 - un premier moyen (30) pour l'amplification de la différence de tension entre un premier (P1) et un second (P2) point d'entrée par division approximative du premier courant de fonctionnement (I_A) en une paire de premiers signaux internes amplifiés, le premier (P1) et le second (P2) point d'entrée étant couplés, respectivement, à la première (T1) et à la seconde (T2) borne d'entrée, le premier moyen (30) étant opérationnellement conducteur afin de produire ainsi les premiers signaux internes lorsque la tension de mode commun V_{CM} du signal d'entrée du circuit est dans une partie de la plage d'alimentation s'étendant jusqu'à V_{HH} ;
 - un second moyen (32) pour l'amplification de la différence de tension entre un troisième (P3) et un quatrième (P4) point d'entrée par division approximative du second courant de fonctionnement (I_B) en une paire de seconds signaux internes amplifiés, le troisième (P3) et le quatrième (P4) point d'entrée étant couplés, respectivement, à la première (T1) et à la seconde (T2) borne d'entrée, le second moyen (32) étant opérationnellement conducteur afin de produire ainsi les seconds signaux internes lorsque V_{CM} est dans une partie de la plage d'alimentation s'étendant vers le bas jusqu'à V_{LL} telle qu'au moins un des moyens différentiels est opérationnellement conducteur pendant que V_{CM} traverse pratiquement la plage d'alimentation entière lorsque V_{PS} est supérieure ou égale à un niveau minimum spécifié; et
 - un moyen de sommation (36) pour la combinaison des signaux internes afin de générer au moins un signal de sortie (I_O) du circuit, caractérisé en ce que le circuit comprend en plus :
 - des moyens de décalage de niveau (38, 40, 42, 44) ayant pour effet, de manière sélective, que les tensions du premier (P1) et du second (P2) point d'entrée soient supérieures, respectivement, à la première et à la seconde tension d'entrée, respectivement, d'un premier (38) et d'un second (40) décalage de niveau de tension

et ayant pour effet, de manière sélective, que les tensions du troisième (P3) et du quatrième (P4) point d'entrée soient supérieures, respectivement, à la première et à la seconde tension d'entrée, respectivement, d'un troisième (42) et d'un quatrième (44) décalage de niveau de tension.

2. Circuit suivant la revendication 1, caractérisé en ce que les décalages de niveau (38, 40, 42, 44) sont fournis à des valeurs appropriées pour réduire le niveau minimum spécifié de V_{PS} à une valeur inférieure à celle qui se produirait si (a) les tensions au premier (P1) et au second (P2) point d'entrée étaient toujours pratiquement égales à la première tension d'entrée et (b) les tensions au troisième (P3) et au quatrième (P4) point d'entrée étaient toujours pratiquement égales à la seconde tension d'entrée.
3. Circuit suivant la revendication 2, caractérisé en ce que le premier moyen (30) est opérationnellement conducteur lorsque l'amplitude de la différence entre V_{LL} et la partie de mode commun V_{CMA} des tensions au premier (P1) et au second (P2) point d'entrée est supérieure ou égale à une première tension de seuil V_{TA} , qui peut varier avec V_{PS} ; et le second moyen (32) est opérationnellement conducteur lorsque l'amplitude de la différence entre V_{HH} et la partie de mode commun V_{CMB} des tensions au troisième (P3) et au quatrième (P4) point d'entrée est supérieure ou égale à une seconde tension de seuil V_{TB} , qui peut varier avec V_{PS} , caractérisé en ce que (a) le premier (38) et le second (40) décalage de niveau de tension sont fournis à des valeurs supérieures ou égales à $V_{TA} - V_{CM} + V_{LL}$, mais inférieures à $V_{HH} - V_{CM}$ et (b) le troisième (42) et le quatrième (44) décalage de niveau de tension sont fournis à des valeurs supérieures ou égales à $V_{TB} + V_{CM} - V_{HH}$, mais $V_{CM} - V_{LL}$.
4. Circuit suivant la revendication 3, caractérisé en ce que V_{TA} et V_{TB} ont des valeurs minimums respectives V_{MA} et V_{MB} , caractérisé en ce que la valeur du niveau minimum spécifié pour V_{PS} est inférieure à $V_{MA} + V_{MB}$.
5. Circuit suivant la revendication 4, caractérisé en ce que la valeur du niveau minimum spécifié pour V_{PS} est supérieure ou égale à V_{MA} et V_{MB} .
6. Circuit suivant la revendication 3, caractérisé en ce que (a) le premier (38) et le second (40) décalage de niveau de tension sont essentiellement égaux et (b) le troisième (42) et le quatrième (44) décalage de niveau de tension sont essentiellement égaux.



7. Circuit suivant l'une quelconque des revendications précédentes, caractérisé en ce que le moyen de décalage de niveau comprend :
- un moyen de secteur, couplé entre les bornes d'entrée (T1, T2) et les points d'entrée (P1, P2, P3, P4) afin de fournir les décalages de niveau; et
 - un moyen d'alimentation (46) de décalage de niveau pour fournir le courant au moyen de secteur afin de commander les valeurs des décalages de niveau.
8. Circuit suivant la revendication 7, caractérisé en ce que le moyen de secteur comprend un premier élément de décalage de niveau (R1) couplé entre la première borne d'entrée (T1) et le premier point d'entrée (P1), un second élément de décalage de niveau (R2) couplé entre la seconde borne d'entrée (T2) et le second point d'entrée (P2), un troisième élément de décalage de niveau (R3) couplé entre la première borne d'entrée (T1) et le troisième point d'entrée (P3), et un quatrième élément de décalage de niveau (R4) couplé entre la deuxième borne d'entrée (T2) et le quatrième point d'entrée (P4).
9. Circuit suivant la revendication 8, caractérisé en ce que chaque élément de décalage de niveau comprend une résistance.
10. Circuit suivant la revendication 8, caractérisé en ce que le moyen d'alimentation de décalage de niveau comprend une première source de courant (S1) couplée entre le premier point d'entrée (P1) et la source V_{HH} , une seconde source de courant (S2) couplée entre le second point d'entrée (P2) et la source V_{HH} , une troisième source de courant (S3) couplée entre le troisième point d'entrée (P3) et la source V_{LL} , une quatrième source de courant (S4) couplée entre le quatrième point d'entrée (P4) et la source V_{LL} , et un moyen de commande (56) pour commander la conduction des sources de courant.
11. Circuit suivant la revendication 10, caractérisé en ce que le moyen d'alimentation de décalage de niveau (46) comprend en plus une cinquième source de courant (S5) couplée entre la première borne d'entrée (T1) et la source V_{HH} , une sixième source de courant (S6) couplée entre la seconde borne d'entrée (T2) et la source V_{HH} , une septième source de courant (S7) couplée entre la première borne d'entrée (T1) et la source V_{LL} , et une huitième source de courant (S8) couplée entre la seconde borne d'entrée (T2) et la source V_{LL} .
12. Circuit suivant la revendication 10 ou 11, caractérisé en ce que chaque source de courant (S1, ..., S8) fournit progressivement moins de courant lorsque la tension d'alimentation V_{PS} augmente, de façon à mettre graduellement hors service les moyens de décalage de niveau.
13. Circuit suivant la revendication 10, caractérisé en ce que le moyen de commande (56) fournit au moins à une partie des sources de courant un signal de commande (V_{CH} , V_{CL}) qui, lorsque V_{PS} est suffisamment basse, change graduellement en fonction de V_{CM} (a) d'un premier niveau de commande vers un second niveau de commande dans une première zone de transition de tension référencée par rapport à V_{HH} et (b) du second niveau de commande en retour vers le premier niveau de commande dans une seconde zone de transition de tension référencée par rapport à V_{LL} .
14. Circuit suivant la revendication 13, caractérisé en ce que les zones de transition de tension se touchent mutuellement.
15. Circuit suivant la revendication 14, caractérisé en ce que les zones de transition de tension diminuent de taille lorsque V_{PS} augmente de sorte que la différence entre les deux niveaux de commande diminue.
16. Circuit suivant la revendication 13, caractérisé en ce que le moyen de commande (56) (a) fournit le premier signal de commande (V_{CH}) à la première (S1) et à la seconde (S2) source de courant, (b) génère un second signal de commande (V_{CL}) variant essentiellement de manière opposée au premier signal de commande, et (c) fournit le second signal de commande à la troisième (S3) et à la quatrième (S4) source de courant.
17. Circuit suivant la revendication 13, caractérisé en ce que le moyen de commande (56) comprend :
- un moyen de génération (54) sensible aux tensions d'entrée afin de produire la première et la seconde tension de fonctionnement en relation spécifique par rapport à V_{CM} ;
 - un premier moyen de référence (62) pour fournir une première tension de référence qui est référencée par rapport à V_{LL} au moins lorsque V_{PS} est suffisamment petite;
 - un second moyen de référence (64) pour fournir une seconde tension de référence qui est référencée par rapport à V_{HH} au moins lorsque V_{PS} est suffisamment petite; et
 - un moyen linéaire (64, 66) sensible aux tensions de fonctionnement et aux tensions de référence afin de produire le premier signal de commande.



18. Circuit suivant la revendication 17, caractérisé en ce que le moyen linéaire (64, 66) comprend :
- une première section d'amplification (66) pour amplifier la différence entre la première tension de fonctionnement et la première tension de référence afin de produire une première tension amplifiée;
 - une seconde section d'amplification (64) pour amplifier la différence entre la seconde tension de fonctionnement et la seconde tension de référence afin de produire une seconde tension amplifiée; et
 - un moyen ET/NON-ET (68) afin de générer le premier signal de commande essentiellement, soit comme ET linéaire des tensions amplifiées, soit comme NON-ET linéaire des tensions amplifiées.
19. Circuit suivant la revendication 17, caractérisé en ce que le moyen linéaire comprend :
- une première section d'amplification (64) pour amplifier la différence entre la première tension de fonctionnement et la première tension de référence afin de produire une première tension amplifiée; et
 - une seconde section d'amplification (78) ayant une borne de commande de gain sensible à la première tension amplifiée afin d'amplifier la différence entre la seconde tension de fonctionnement et la seconde tension de référence afin de produire le premier signal de commande.
20. Circuit suivant la revendication 17, caractérisé en ce que le moyen de génération (54) comprend les éléments de décalage de niveau, les deux moyens différentiels (30, 32), et l'alimentation principale (34).
21. Circuit suivant la revendication 20, caractérisé en ce que la première et la seconde tension de fonctionnement sont essentiellement les tensions auxquelles le premier et le second courant de fonctionnement sont, respectivement, fournis.
22. Circuit suivant l'une quelconque des revendications précédentes, caractérisé en ce que les premiers signaux internes sont représentatifs de manière différentielle du signal d'entrée de circuit lorsque le premier moyen (30) est opérationnellement conducteur; et les seconds signaux internes sont représentatifs de manière différentielle du signal d'entrée de circuit lorsque le second moyen (32) est opérationnellement conducteur.
23. Circuit suivant l'une quelconque des revendications précédentes, caractérisé en ce que chacun des premier et second moyens (30, 32) comprend
- une paire d'amplificateurs de même configuration, chaque amplificateur ayant une première électrode de courant, une seconde électrode de courant, et une électrode de commande pour réguler la transmission du courant entre les électrodes de courant, les amplificateurs (Q1, Q2) du premier moyen (30) ayant (a) leurs électrodes de commande respectivement couplées au premier (P1) et au second (P2) point d'entrée, (b) leurs premières électrodes couplées entre elles afin de recevoir le premier courant de fonctionnement (I_A), et (c) leurs secondes électrodes respectivement couplées au moyen d'addition (36) afin de fournir les premiers courants internes, les amplificateurs (Q3, Q4) du second moyen (32) ayant (a) leurs électrodes de commande respectivement couplées au troisième (P3) et au quatrième (P4) point d'entrée, (b) leurs premières électrodes couplées entre elles afin de recevoir le second courant de fonctionnement (I_B), et (c) leurs secondes électrodes couplées au moyen d'addition (36) afin de fournir les seconds courants internes, les amplificateurs (Q3, Q4) du second moyen (32) étant complémentaires des amplificateurs (Q1, Q2) du premier moyen (30).
24. Circuit suivant la revendication 23, caractérisé en ce que les porteurs de charge qui se déplacent entre les électrodes de courant de chaque amplificateur proviennent de sa première électrode et aboutissent à sa seconde électrode.
25. Circuit suivant la revendication 24, caractérisé en ce que chaque amplificateur est un transistor bipolaire ayant un émetteur, un collecteur et une base respectivement connectés à la première électrode, à la seconde électrode et à l'électrode de commande de cet amplificateur.

