signal indicates a difference between the desired output frequency and the determined output frequency;

a loop selector circuit configured to receive the error signal from the frequency-locked loop circuit and the error signal from the phase-locked loop circuit, select one of the error signals and output the selected error signal, wherein the loop selector circuit enables the phase-locked loop circuit when the difference indicated by the error signal received from the frequency–locked loop circuit is less than a threshold and enables the frequency-locked loop circuit when the difference indicated by the error signal received from the phase-locked loop circuit is greater than the threshold; and

a controller configured to receive the selected error signal from the loop selector circuit and converts the error signal to the control signal for the oscillator circuit, wherein the oscillator circuit, the frequency-locked loop circuit, the phase-locked loop circuit and the loop selector circuit are implemented in the digital domain without the use of capacitors and inductors.

12. The programmable clock generator of claim 11 wherein the oscillator circuit is implemented by a ring oscillator.

13. The programmable clock generator of claim 11 wherein the oscillator circuit is implemented with CMOS transistors, each transistor having a channel length ten times the minimum length for CMOS technology.

14. The programmable clock generator of claim 11 wherein the frequency-locked loop circuit oversamples the output signal from the oscillator circuit and determines the frequency of the output signal from the oversampled signal.