provided in the probe card 20.

The probe card 20 includes the plurality of probe electrodes 21. Each of the plurality of probe electrodes 21 is electrically coupled to each of memory controllers (hereinafter, referred to as “NAND controller chips”, which are not illustrated in the drawings) mounted on the probe card 20 and provided in units of chips.

The control unit 30 includes, for example, a temperature control system 31, a drive control system 32, and an interface control system 33, and controls the entire operation of the prober 3.

The temperature control system 31 controls a temperature environment to which the probe card 20 and the storage wafer 10 or the cleaning wafer 10c are exposed in the prober 3. In the present embodiment, for example, the temperature control system 31 performs control such that the temperatures of the probe card 20 and the storage wafer 10 or the cleaning wafer 10c do not change from the predetermined temperatures.

The drive control system 32 has a mechanism capable of three-dimensionally and freely displacing the storage wafer 10 with respect to the probe card 20. In addition, the drive control system 32 has a function of contacting the plurality of pad electrodes 11 on the storage wafer 10 and the plurality of probe electrodes 21 on the corresponding probe card 20 by controlling the mechanism.

the NAND controller chip 200.

The peripheral circuit 120 includes an I/F circuit 121, a command register 126, an address register 127, a data register 128, a driver 129, a row decoder 130, a sense amplifier module 131, and a sequencer 132.

The I/F circuit 121 is a circuit group that mainly manages an interface between the pad electrodes 11 and other portions in the peripheral circuit 120 in the NAND chip unit 100, and includes an input/output circuit 122, a logic control circuit 123, a timing adjustment circuit 124, and an ECC circuit 125.

The input/output circuit 122 transmits and receives the signal I/O to and from the NAND controller chip 200. When the signal I/O is received from the NAND controller chip 200, the input/output circuit 122 distributes the signal I/O to the command CMD, the address ADD, and the data DAT based on information from the logic control circuit 123. The input/output circuit 122 transfers the command CMD to the command register 126 and transfers the address ADD to the address register 127. Further, the input/output circuit 122 transmits and receives the write data and read data DAT to and from the data register 128.

The logic control circuit 123 receives the signals CEn, CLE, ALE, WEn, and REn from the NAND controller chip 200, and sends information for identifying the command CMD, the address ADD, and the data DAT in the signal I/O to the input/output circuit 122. Further, the logic

in FIG. 15. Steps ST11 to ST19 in FIG. 15 are an example illustrating details of step ST10 in FIG. 14.

As illustrated in FIG. 15, in step ST11, the prober 3 selects the storage wafer 10 to be accessed based on a request from the host device 2. In the following description, the storage wafer 10 selected in step ST11 is also referred to as the “selected storage wafer 10”.

In step ST12, the prober 3 initializes a variable i to “1” ($1 \leq i \leq n$).

In step ST13, the prober 3 refers to the probe management table 335 and determines whether or not the defect flag corresponding to the pad group PdGi of the selected storage wafer 10 is “False”. When the corresponding defect flag is not “False” (step ST13; no), the prober 3 determines that the pad group PdGi cannot be used, and the processing proceeds to step ST14. When the corresponding defect flag is “False” (step ST13; yes), the prober 3 determines that the pad group PdGi can be used, and the processing proceeds to step ST15.

In step ST14, the prober 3 increments the variable i and returns the processing to step ST13. As a result, steps ST13 and ST14 are repeated until it is determined that the pad group PdGi can be used.

In step ST15, the prober 3 selects the pad group PdGi as the pad group PdG to be brought into contact with the probe electrode 21.

In step ST16, the prober 3 confirms, for example,

coupling the pad region and the peripheral circuit region. Specifically, for example, as illustrated in FIGS. 18 and 19, after the pad group PdG1 is selected, the pad group PdG2 closer to the conductor 75 than the pad group PdG1 is desirably selected. As a result, it is possible to suppress the presence of a defective pad electrode in a conductive path between the probe electrode 21 and the conductor 75. Therefore, it is possible to suppress communication between the NAND controller chip 200 and the NAND chip unit 100 from being inhibited by the defective pad electrode.

1.2.4.2 Read processing

Next, as an example of further data communication processing, a case of read processing will be described using a flowchart illustrated in FIG. 20. Similarly to FIG. 17, FIG. 20 illustrates an example of a flow of the read processing after the alignment processing and the touchdown processing are executed following the wafer conveyance processing and the prober 3 and the storage wafer 10 are electrically coupled.

As illustrated in FIG. 20, in step ST51, the NAND controller chip 200 in the prober 3 issues a read command CMD based on a data read request from the host device 2. In addition, the NAND controller chip 200 sends a read command set including the read command CMD and the address ADD to the NAND chip unit 100. The processing of the prober 3 proceeds to step ST55.

C L A I M S

1. A storage system comprising:

a first memory chip unit including a first pad electrode including a first portion and a second portion electrically coupled to each other, and a first memory cell array electrically coupled to the first pad electrode; and

a prober that is able to hold the first memory chip unit and executes reading and writing on the first memory cell array of the held first memory chip unit, wherein

the prober includes

a probe card including a first probe electrode that is able to be in contact with the first pad electrode of the held first memory chip unit, and a first memory controller that is able to be electrically coupled to the first probe electrode and execute reading and writing on the first memory cell array via the first probe electrode, and

a movement mechanism that moves the probe card or the held first memory chip unit to bring the first pad electrode of the held first memory chip unit into contact with the first probe electrode, and

the movement mechanism executes a first operation that brings the first probe electrode into contact with the first portion of the first pad electrode and does not bring the first probe electrode into contact with the second portion of the first pad electrode, and a second operation that does not bring

the first probe electrode into contact with the first portion of the first pad electrode and brings the first probe electrode into contact with the second portion of the first pad electrode.

2. The storage system according to claim 1, further comprising:

a first wafer including the first memory chip unit, wherein

the prober is able to hold the first wafer, and holds the first memory chip unit by holding the first wafer, and

the movement mechanism moves the first memory chip unit by moving the first wafer.

3. The storage system according to claim 1, wherein

the movement mechanism is configured to

execute the first operation when a first condition is not satisfied, and

execute the second operation when the first condition is satisfied.

4. The storage system according to claim 3, wherein

the first condition includes that the number of times of contact between the first probe electrode and the first portion of the first pad electrode is equal to or larger than a first threshold.

5. The storage system according to claim 3, wherein

the first condition includes that the first memory controller has failed in error correction processing of data from the first memory chip unit.

6. The storage system according to claim 3, wherein

the first condition includes that the first memory chip unit has failed in error correction processing of data from the first memory controller.

7. The storage system according to claim 1, wherein

the first memory chip unit includes a latch circuit that is commonly coupled to the first portion and the second portion of the first pad electrode.

8. The storage system according to claim 4, further comprising:

a first wafer including the first memory chip unit; and

a second wafer, wherein

the prober is able to hold the first wafer, and holds the first memory chip unit by holding the first wafer,

the movement mechanism moves the first memory chip unit by moving the first wafer, and

the movement mechanism is further able to execute a third operation that brings the first probe electrode into contact with the second wafer.

9. The storage system according to claim 8, wherein

the movement mechanism is configured to execute the first operation or the second operation after executing the third operation, when a second condition is satisfied.

10. The storage system according to claim 9, wherein

the second condition includes that the number of times of contact between the first probe electrode and the first wafer is equal to or larger than a second threshold larger than the first threshold.

11. The storage system according to claim 2, wherein

the first wafer further includes a second memory chip unit including a second pad electrode including a first portion and a second portion electrically coupled to each other, and a second memory cell array electrically coupled to the second pad electrode,

the probe card further includes a second probe electrode electrically coupled to the first memory controller,

the first operation further includes bringing the second probe electrode into contact with the first portion of the second pad electrode, and

the second operation further includes bringing the second probe electrode into contact with the second portion of the second pad electrode.

12. The storage system according to claim 2, wherein

the first wafer further includes a third memory chip unit including a third pad electrode including a first portion and a second portion electrically coupled to each other, and a third memory cell array electrically coupled to the third pad electrode,

the probe card further includes a third probe electrode and a second memory controller electrically coupled to the third probe electrode,

the first operation further includes bringing the third probe electrode into contact with the first portion of the third pad electrode, and

the second operation further includes bringing the third probe electrode into contact with the second portion of the third pad electrode.

13. The storage system according to claim 2, wherein

the first pad electrode has a convex shape from the first wafer toward the probe card in a state where the first wafer is placed in the prober, and

a portion of the first probe electrode facing the first wafer placed in the prober has a flat plate shape.

14. A memory chip unit, comprising:

a memory structure including a plurality of first

conductor layers stacked in a first direction above a substrate, a first semiconductor layer extending in the first direction in the plurality of first conductor layers, and a first charge storage layer provided between the plurality of first conductor layers and the first semiconductor layer;

a first interconnect layer and a second interconnect layer provided above the memory structure so as to be electrically insulated from each other;

a second conductor layer provided on a top surface of a first portion of the first interconnect layer;

a third conductor layer provided on a top surface of a second portion of the first interconnect layer;

a fourth conductor layer provided on a top surface of the first portion of the second interconnect layer; and

a fifth conductor layer provided on a top surface of a second portion of the second interconnect layer, wherein

the second conductor layer, the third conductor layer, the fourth conductor layer, and the fifth conductor layer include aluminum (Al), and

a relative position of the fourth conductor layer with respect to the second conductor layer is matched with a relative position of the fifth conductor layer with respect to the third conductor layer in a plane parallel to the substrate.

15. The memory chip unit according to claim 14, wherein

a direction in which the second conductor layer and the

third conductor layer are arranged is parallel to a direction in which the fourth conductor layer and the fifth conductor layer are arranged, and

a direction in which the second conductor layer and the fourth conductor layer are arranged is parallel to a direction in which the third conductor layer and the fifth conductor layer are arranged.

16. The memory chip unit according to claim 14, further comprising:

a sixth conductor layer provided on a top surface of the second conductor layer; and

a seventh conductor layer provided on a top surface of the third conductor layer, wherein

the sixth conductor layer and the seventh conductor layer include a metal different from a metal of the second conductor layer and the third conductor layer.

17. The memory chip unit according to claim 16, wherein

the sixth conductor layer and the seventh conductor layer include at least one metal selected from nickel (Ni), gold (Au), cobalt (Co), palladium (Pd), copper (Cu), and silver (Ag).

18. The memory chip unit according to claim 16, wherein

a top surface of the sixth conductor layer and a top surface of the seventh conductor layer are located above a top

surface of an insulator layer between the sixth conductor layer and the seventh conductor layer.

19. The memory chip unit according to claim 14, further comprising

a dicing line provided between the second conductor layer and the third conductor layer.

20. A wafer comprising:

a memory structure including a plurality of first conductor layers stacked in a first direction above a substrate, a first semiconductor layer extending in the first direction in the plurality of first conductor layers, and a first charge storage layer provided between the plurality of first conductor layers and the first semiconductor layer;

a second conductor layer provided above the memory structure;

a third conductor layer provided above the second conductor layer;

a fourth conductor layer electrically coupling the second conductor layer and the third conductor layer; and

an insulator layer provided between the second conductor layer and the third conductor layer and including polyimide, wherein

in plan view,

the fourth conductor layer crosses a dicing line, and

the second conductor layer and the third conductor layer sandwich the dicing line.

21. The wafer according to claim 20, wherein

the second conductor layer includes aluminum (Al), and

the fourth conductor layer includes copper (Cu).

22. The wafer according to claim 21, further comprising:

a fifth conductor layer adjacent to the second conductor layer in a first plane parallel to the substrate; and

a sixth conductor layer adjacent to the third conductor layer in a second plane parallel to the substrate, wherein

a distance between the third conductor layer and the sixth conductor layer is longer than a distance between the second conductor layer and the fifth conductor layer.

23. The wafer according to claim 22, further comprising:

a seventh conductor layer electrically coupled to the sixth conductor layer in the first plane, wherein

a distance between the third conductor layer and the sixth conductor layer is shorter than a distance between the second conductor layer and the seventh conductor layer.

24. The wafer according to claim 22, wherein

a direction in which the second conductor layer and the fifth conductor layer are arranged is different from a

direction in which the third conductor layer and the sixth conductor layer are arranged.

25. The wafer according to claim 21, wherein

an area of the third conductor layer is larger than an area of the second conductor layer in plan view.

26. The wafer according to claim 21, further comprising:

an eighth conductor layer electrically coupled to the third conductor layer via the second conductor layer and including aluminum (Al).

27. The wafer according to claim 21, further comprising:

a ninth conductor layer electrically coupled to the third conductor layer without going through the second conductor layer and including aluminum (Al).

28. The wafer according to claim 21, further comprising:

a tenth conductor layer electrically coupled to the third conductor layer without going through the second conductor layer and the fourth conductor layer and including aluminum (Al).

29. The wafer according to claim 21, wherein

the third conductor layer includes gold (Au) or nickel (Ni).