

ABSTRACT

A semiconductor package and a method manufacturing the same are disclosed. At least one semiconductor chip is mounted on a package substrate. An insulative mold layer is formed at sides of the semiconductor chip having at least one recess in a region in which conductive connection members are formed, the recess defining one or more protrusions within the mold layer. An interposer is positioned on the protrusions with the conductive connection members connecting and providing electrical connections between conductive pads on the upper surface of the package and conductive pads on the lower surface of the package substrate. The protrusions may position the interposer in the vertical direction by defining the vertical spacing between the lower surface of the interposer and the upper surface of the package substrate. The protrusions may also position the interposer in one or more horizontal directions and/or prevent substantial movement during connecting of the interposer to the package substrate. An under-fill resin layer may be injected into remaining space between the interposer and the package substrate.

FIG. 2