Description

Cross reference to related applications

1. European Patent Application No. 81903037.0 (WO—A—82/02299, published 8.7.82) entitled "Horizontal Oscillator",

2. European Patent Application No. 81903038.8 (WO—A—82/02309, published 8.7.82) entitled "Horizontal Phase Detector Gain Control",

3. European Patent Application No. 81903039.6 (WO—A—82/02311, published 8.7.82) entitled "Large Scale, Single Chip Integrated Circuit Television Receiver Subsystem",

4. European Patent Application No. 81902999.2 (WO—A—82/02302, published 8.7.82) entitled "Variable Capacitance Circuit",

5. European Patent Application No. 81902937.2 (WO—A—82/02293, published 8.7.82) entitled "Linear Full Wave Rectifier Circuit",

Background of the invention

Field of the invention

This invention relates generally to television receiver systems and, more particularly, to an improved horizontal phase lock loop which employs an oscillator which oscillates at twice line frequency, provides an accurate fifty percent duty cycle horizontal output drive waveform and provides an accurate fifty percent duty cycle phase detector switching waveform to assure symmetrical pull-in performance.

Description of the prior art

In most modern television receivers, a phase lock loop is employed to lock the horizontal oscillator in the horizontal sweep section of the receiver to the incoming separated horizontal synchronization pulses to establish the phase relationship between the incoming synchronization pulses and the horizontal flyback pulse thus fixing the television picture on the raster. In the prior art single loop system, the horizontal oscillator operates at line frequency (15.75 KHz in the United States) and its output is a ramp signal. This ramp signal is then shaped to form a square wave drive signal to the horizontal output stage which in turn produces flyback pulses approximately microseconds wide and approximately 63 microseconds apart. The flyback pulses are then processed by external wave shaping circuitry to produce a ramp signal which is applied to one input of a horizontal phase detector. The phase detector has a second input coupled to a bias voltage. The incoming horizontal synchronization pulse gates the phase detector which generates a d.c. output for controlling the horizontal frequency.

This system suffers from several disadvantages. First, many external components are required to shape the flyback pulse stream into a ramp for the phase detector. Second, the pull-in symmetry of the loop depends on the shaped ramp and the flyback signal which may vary with signal conditions and loading. Third, the loop's response time or bandwidth is a compromise between a requirement for good low signal operation (low bandwidth and slow response time) and variations in loop delay in the horizontal output stage which requires a fast loop response to avoid horizontal displacement or portions of the picture on the raster. Finally, this system does not provide a clock signal at twice line frequency for a vertical countdown section. If the vertical deflection signal is derived from the horizontal oscillator by countdown, then the twice line frequency clock is required at the counter input to provide for proper vertical interlacing.

To reduce the effects of the first three, disadvantages described above, two loop systems have been employed, e.g. the TBA920/TDA2590 2-loop system by Philips. This system suffers, however, from the disadvantage that the duty cycle of the horizontal output stage drive signal varies as the second loop corrects for changes in loop delays. Furthermore, this system does not employ a 31.5 KHz oscillator necessary for vertical countdown; i.e. twice U.S. line frequency. From US—A—4214260 there is known a horizontal phase lock loop for use in a television receiver of the type which receives horizontal synchronization pulses at the picture line frequency and which includes a horizontal output stage for generating flyback pulses; a first loop including a first phase detector, an oscillator and a first divide by two circuit; and a second loop including a second phase detector; said first phase detector having a first input coupled to receive said synchronization pulses, and a second input; said oscillator having an input coupled to an output of said first phase detector for generating a ramp waveform, said output of said first phase detector altering the frequency of said oscillator; said first divide by two circuit having an input coupled to said ramp waveform for producing a switching waveform, said second input of said first phase detector receiving said switching waveform; said first loop locking said oscillator to said horizontal synchronization pulses; said horizontal phase lock loop.

Summary of the invention

It is an object of the present invention to provide an improved horizontal phase lock loop for a television receiver.

It is a further object of the invention to provide a phase lock loop for a television receiver which provides a clock signal at twice the line frequency to a vertical countdown counter to achieve proper vertical interlacing.

It is a still further object of the invention to provide a horizontal phase lock loop for a television receiver which provides a horizontal output drive signal and a phase detector switching signal each of which have an accurate fifty percent duty cycle.

According to a first aspect of the present invention a horizontal phase lock loop of the above known kind is characterized by said ramp waveform having a frequency substantially equal to twice said line frequency; said second loop

locking said flyback pulses to said switching waveform, said second loop further including first means and a second divide by two circuit; said second phase detector having a first input coupled to said switching waveform and a second input coupled to receive said flyback pulses; said first means having a first input coupled to said ramp waveform and a second input coupled to an output of said second phase detector for slicing said ramp waveform and producing an output having a frequency substantially equal to said ramp waveform; said second divide by two circuit having an input coupled to the output of said first means and an output coupled to said horizontal output stage for producing a fifty percent duty cycle drive waveform having a frequency substantially equal to said line frequency.

According to a second aspect of the present invention there is provided a method for locking the horizontal oscillator of a television receiver to the line frequency horizontal synchronization pulses received by said television receiver, the method comprising:

receiving said horizontal synchronisation pulses in a first phase detector and producing an output therefrom,

controlling the oscillator frequency in accordance with said first phase detector output,

generating from said first phase detector output a ramp waveform,

generating from said ramp waveform in a first divide by two circuit a switching waveform, and

applying said switching waveform to said first phase detector so as to lock said oscillator to said horizontal synchronisation pulses, and

generating from said oscillator output flyback pulses,

characterised by

said ramp waveform having a frequency substantially equal to twice said line frequency, and

locking said flyback pulses in a second phase detector and producing an output therefrom, slicing said ramp waveform in dependence on said second phase detector output to produce a sliced signal having a frequency substantially equal to said ramp waveform, generating from said sliced signal in a second divide by two circuit a fifty percent duty cycle waveform having a frequency substantially equal to said line frequency, and using said fifty percent duty cycle waveform in generating said flyback pulses.

The above and other objects, features and advantages of the invention will be better understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

Brief description of the drawings

Figures 1 and 2 illustrate the composite video signal received by a television receiver;

Figure 3 is a block diagram of a basic prior art television receiver;

Figure 4 is a block diagram of the inventive horizontal phase lock loop; and

Figures 5A, 5B and 5C illustrate waveforms appearing at certain points in Figure 1.

Description of the preferred embodiment

Before embarking on a detailed discussion of the invention, it may be helpful to briefly review basic television principles. A complete TV picture appears on the TV screen thirty times per second. Between each picture, there is an interval during which the screen is dark. Each TV frame, however, is not projected as a complete picture but is created in sections by varying the brightness of a moving spot of light. That is, the picture tube contains an electron gun which generates an electron beam which moves very rapidly across a phosphor coated screen and, by changing its strength, different amounts of light are produced in different places. More exactly, the electron beam is focused into a fine point that moves from the upper left-hand corner in a straight horizontal line to the right side of the screen. After each movement from left to right, the beam intensity is reduced so that no light is produced during the return motion from right to left. After each line is painted, the beam is moved down a little on the tube face. While the motion of the electron beam is called "scanning", the electronic actions involved are generally referred to a "sweeping" and we speak of a horizontal sweep frequency of approximately 15,750 cycles per second.

It should be obvious that there must be some synchronization between the image seen by a remote television camera and that which is ultimately shown on the TV screen. If, for example, the receiver scans a picture in more or less than one-thirtieth of a second, the picture will appear to roll vertically. Thus, great care is taken to synchronize accurately the scanning of each line and frame. To achieve this, synchronizing signals are transmitted to the receiver with the sound and video information. In addition to providing signals which control the starting of each line, the edges of the picture must be blanked out to avoid any appearance of ragged edges, and the electron beam must turned off during the time in which it returns to its starting place. This return time is often referred to as the retrace or flyback period and is approximately 9 microseconds long for each line (the horizontal flyback), but is considerably longer for the period when the beam returns from the bottom to the top of the screen (the vertical flyback period).

Figure 1 illustrates a black and white video signal including the horizontal synchronization pulses 2 and the horizontal blanking or flyback pulse 4. Interposed between successsive flyback pulses is the actual black and white video signal 6 corresponding to one picture line. As can be seen, the horizontal flyback pulse 4 extends into the black region so that the edges of the picture are completely black avoiding the appearance of ragged edges.

Referring to Figure 2, the start of each field of vertical scanning is dictated by a vertical syn-

chronization pulse which lasts much longer than the horizontal synchronization pulses. To avoid losing horizontal synchronization during the vertical flyback or blanking period, the horizontal synchronization pulses are superimposed on the vertical blanking pulse. The first six pulses are very narrow and are referred to as equalizing pulses. Next, there are periods of six wide pulses which comprise the actual vertical synchronization pulse serrated by the horizontal synchronization period. This is followed by an additional six equalizing pulses and then four regular horizontal synchronizing pulses that start the top of the picture. Note that the vertical blanking period extends through this time and darkens the screen while the beam moves from bottom to top and covers the first four lines of the picture.

Figure 3 is a block diagram of a basic black and white TV receiver. From the antenna, a transmission line 8 brings all signals received by the antenna to tuner 10 whose function it is to select the desired band of frequencies and reject all others. The tuner passes only the desired intermediate frequency to the IF amplifiers 12.

Television IF amplifiers 12 include a plurality of IF stages which amplify the IF signals. To prevent over-loading and to minimize picture changes during fading, automatic gain control is used to control the amplification of the IF signal.

The output of IF amplifiers 12 is applied to a detector 14 which removes the amplitude modulated video signal and applies it to video amplifier 16. The sound signal is removed, amplified, clipped, and limited in audio section 18. The output of audio detector 18 is applied to audio amplifier 20 which is similar to audio amplifiers found in radio receivers. The output of the audio amplifier is applied to the speaker.

Video amplifier 16 requires more bandwidth than audio amplifier 20. This is accomplished using special peaking circuits for the high and low frequency response. The output of video amplifier 16 is applied to the picture tube and to a sync separator 22 which is unique to television receivers. As described earlier, the horizontal and vertical synchronization pulses appear on top of their respective blanking signals which are sandwiched in between lines of picture signal. The sync separator clips the syncrhonization pulses off the composite video signal after the signal has been amplified in video amplifier 16. Two separate filters may be employed to separate the vertical from the horizontal synchronization pulses. For example, a high pass filter would permit only the horizontal synchronization pulses to reach horizontal sweep section 24 while the vertical pulses could be passed through a low pass filter to the vertical sweep section 26.

The vertical sweep section generates the actual signals which pass through the deflection yoke of the picture tube to move the electron beam up and down. Similarly, the horizontal sweep section is responsible for moving the electron beam across the tube. In order to obtain the large current of short duration required in the horizontal deflection coils, a transformer is generally used. Furthermore, a flyback transformer is generally considered part of the horizontal sweep section. This transformer generates a high voltage during the time in which the electron beam returns from right to left.

Co-pending Patent Application WO—A—82/02311, pub. 8.7.82 entitled "Large Scale, Single Chip Integrated Circuit Television Receiver Subsystem" and filed of even data herewith describes a VLSI single chip television receiver into which the inventive horizontal phase lock loop may be incorporated. Fig. 4 is a block diagram of the inventive two loop horizontal phase lock loop. The first loop consists of a first phase detector 30, a first low pass filter 32, a horizontal oscillator 34, a comparator slicer 36 and a divide-by-two circuit 38. Phase detector 30 has a first input coupled to the horizontal synchronization pulse stream and a second input coupled to the output of the divide-by-two circuit 38. Horizontal oscillator 34 generates asymmetrical ramp signal of the type shown in Fig. 5A at a frequency of 31.5 KHz (twice the line frequency in the U.S.). The ramp signal has a ramp up time of t1=20 microseconds and a ramp down time of t2=12 microseconds. The output of the oscillator is applied to a first input of comparator slicer 36, and a bias voltage is applied to its second input. The DC bias voltage is shown as line 50 in Fig. 5A. The output of comparator slicer 36 is shown in Fig. 5B.

It is important to note that since the horizontal oscillator is implemented on chip, the ramp signal is less likely to be subject to unwanted veriations. However, even if such unwanted variations should occur, the divide-by-two circuit is implemented so as to trigger off the trailing edge of the waveform appearing at the output of comparator slicer 36. This assures a fifty percent duty cycle signal appearing at the output of divide-by-two circuit 38 as is shown in Fig. 5C. The output of divide-by-two circuit 38 is fed back to a second input of phase detector 30 and is used to gate the phase detector. The output of phase detector 30 is filtered in low pass filter 32 the output of which represents a DC control voltage for altering the frequency of horizontal oscillator 34. Thus, the output of divide-by-two circuit 38 is used to gate phase detector 30 thus locking the horizontal oscillator to the horizontal synchronization pulses. Circuits which are suitable for use as phase detector 30 are well known and a further discussion of them is not deemed necessary. One suitable phase detector circuit is shown in co-pending Patent Application WO—A—82/02309 pub. 8.7.82 entitled "Horizontal Phase Detector Gain Control" filed of even date herewith. Further, a suitable oscillator for use as horizontal oscillator 34 is shown and described in co-pending Patent Application WO—A—82/02299 pub. 8.7.82 entitled "Horizontal Oscillator" and filed of even date herewith.

The second loop comprises a second phase detector 40, a second low pass filter 42, phase shift slicer 44, a second divide-by-two circuit 46

and horizontal output circuit 48. The output of divide-by-two circuit 38 is applied to the second phase detector 40 and serves as a switching signal which is gated directly by the flyback pulse coming from horizontal output 48 and applied to a second input of phase detector 40. The output of phase detector 40 is filtered in low pass filter 42 which in turn generates an output which is applied to phase shift slicer 44 for controlling its slicing level. The output of horizontal oscillator 34 is applied to a second input of phase shift slicer 44. The output of phase shift slicer 44, as shown in Fig. 5B, is applied to a divide-by-two circuit 46 which in turn generates a signal similar to that shown in Fig. 5C. The divide-by-two circuit 46 triggers on a single edge of the slicer output as to assure a fifty percent duty cycle signal. The output of divide-by-two circuit 46 is applied as a drive signal to the horizontal output circuit 48 which in turn generates the flyback drive signal to the horizontal output circuit 48 which in turn generates the flyback pulses which are fed back to the second phase detector 40. Thus, by controlling the slicing level in phase shift slicer 44, the phasing of the horizontal drive output can be controlled such that the flyback waveform is centered on the switching waveform applied from divide-by-two circuit 38 to phase detector 40.

The above described approach overcomes loop ambiguities and provides accurate fifty percent duty cycle switching waveforms to both phase detectors and to the horizontal output resulting in symmetrical pull-in. The phase relationship between the first and second loops may be adjusted by designing in a predetermined offset in the second loop phase detector. Further, since horizontal oscillator 34 is operating at twice the line frequency it is suitable for use with a vertical countdown system.

Claims

1. A horizontal phase lock loop for use in a television receiver of the type which receives horizontal synchronization pulses at the picture line frequency and which includes a horizontal output (48) stage for generating flyback pulses; a first loop including a first phase detector (30), an oscillator (34) and a first divide by two circuit (38); and a second loop including a second phase detector (40); said first phase detector (30) having a first input coupled to receive said synchronization pulses, and a second input; said oscillator (34) having an input coupled to an output of said first phase detector (30) for generating a ramp waveform, said output of said first phase detector altering the frequency of said oscillator; said first divide by two circuit (38) having an input coupled to said ramp waveform for producing a switching waveform, said second input of said first phase detector receiving said switching waveform; said first loop locking said oscillator to said horizontal synchronization pulses; said horizontal phase lock loop being characterized by said ramp waveform having a frequency substantially equal to twice said line frequency; said second loop locking said flyback pulses to said switching waveform, said second loop further including first means (44) and a second divide by two circuit (46); said second phase detector (40) having a first input coupled to said switching waveform a second input coupled to receive said flyback pulses; said first means (44) having a first input coupled to said ramp waveform and a second input coupled to an output of said second phase detector (40) for slicing said ramp waveform and producing an output having a frequency substantially equal to said ramp waveform; said second divide by two circuit (46) having an input coupled to the output of said first means (44) and an output coupled to said horizontal output stage (48) for producing a fifty percent duty cycle drive waveform having a frequency substantially equal to said line frequency.

2. The horizontal phase lock loop according to claim 1 further characterized by said synchronization pulses being locked to a point on said ramp signal.

3. The horizontal phase lock loop according to claim 1 or 2 further characterized by said first loop further including a comparator circuit (36) coupled between said oscillator (34) and said first divide by two circuit (38) for generating a first signal having a frequency substantially equal to that of said oscillator.

4. A method for locking the horizontal oscillator of a television receiver to the line frequency horizontal synchronization pulses received by said television receiver, the method comprising:

receiving said horizontal synchronisation pulses in a first phase detector (30) and producing an output therefrom,

controlling the oscillator (34) frequency in accordance with said first phase detector output.

generating from said first phase detector output a ramp waveform,

generating from said ramp waveform in a first divide by two circuit (38) a switching waveform, and

applying said switching waveform to said first phase detector so as to lock said oscillator to said horizontal synchronisation pulses, and

generating from said oscillator output flyback pulses.

characterised by

said ramp waveform having a frequency substantially equal to twice said line frequency, and

locking said flyback pulses in a second phase detector (40) and producing an output therefrom, slicing said ramp waveform in dependence on said second phase detector output to produce a sliced signal having a frequency substantially equal to said ramp waveform, generating from said sliced signal in a second divide by two circuit (46) a fifty percent duty cycle waveform having a frequency substantially equal to said line frequency, and using said fifty percent duty cycle waveform in generating said flyback pulses.

and horizontal output circuit 48. The output of divide-by-two circuit 38 is applied to the second phase detector 40 and serves as a switching signal which is gated directly by the flyback pulse coming from horizontal output 48 and applied to a second input of phase detector 40. The output of phase detector 40 is filtered in low pass filter 42 which in turn generates an output which is applied to phase shift slicer 44 for controlling its slicing level. The output of horizontal oscillator 34 is applied to a second input of phase shift slicer 44. The output of phase shift slicer 44, as shown in Fig. 5B, is applied to a divide-by-two circuit 46 which in turn generates a signal similar to that shown in Fig. 5C. The divide-by-two circuit 46 triggers on a single edge of the slicer output as to assure a fifty percent duty cycle signal. The output of divide-by-two circuit 46 is applied as a drive signal to the horizontal output circuit 48 which in turn generates the flyback drive signal to the horizontal output circuit 48 which in turn generates the flyback pulses which are fed back to the second phase detector 40. Thus, by controlling the slicing level in phase shift slicer 44, the phasing of the horizontal drive output can be controlled such that the flyback waveform is centered on the switching waveform applied from divide-by-two circuit 38 to phase detector 40.

The above described approach overcomes loop ambiguities and provides accurate fifty percent duty cycle switching waveforms to both phase detectors and to the horizontal output resulting in symmetrical pull-in. The phase relationship between the first and second loops may be adjusted by designing in a predetermined offset in the second loop phase detector. Further, since horizontal oscillator 34 is operating at twice the line frequency it is suitable for use with a vertical countdown system.

Claims

1. A horizontal phase lock loop for use in a television receiver of the type which receives horizontal synchronization pulses at the picture line frequency and which includes a horizontal output (48) stage for generating flyback pulses; a first loop including a first phase detector (30), an oscillator (34) and a first divide by two circuit (38); and a second loop including a second phase detector (40); said first phase detector (30) having a first input coupled to receive said synchronization pulses, and a second input; said oscillator (34) having an input coupled to an output of said first phase detector (30) for generating a ramp waveform, said output of said first phase detector altering the frequency of said oscillator; said first divide by two circuit (38) having an input coupled to said ramp waveform for producing a switching waveform, said second input of said first phase detector receiving said switching waveform; said first loop locking said oscillator to said horizontal synchronization pulses; said horizontal phase lock loop being characterized by said ramp waveform having a frequency substantially equal to twice said line frequency; said second loop locking said flyback pulses to said switching waveform, said second loop further including first means (44) and a second divide by two circuit (46); said second phase detector (40) having a first input coupled to said switching waveform a second input coupled to receive said flyback pulses; said first means (44) having a first input coupled to said ramp waveform and a second input coupled to an output of said second phase detector (40) for slicing said ramp waveform and producing an output having a frequency substantially equal to said ramp waveform; said second divide by two circuit (46) having an input coupled to the output of said first means (44) and an output coupled to said horizontal output stage (48) for producing a fifty percent duty cycle drive waveform having a frequency substantially equal to said line frequency.

2. The horizontal phase lock loop according to claim 1 further characterized by said synchronization pulses being locked to a point on said ramp signal.

3. The horizontal phase lock loop according to claim 1 or 2 further characterized by said first loop further including a comparator circuit (36) coupled between said oscillator (34) and said first divide by two circuit (38) for generating a first signal having a frequency substantially equal to that of said oscillator.

4. A method for locking the horizontal oscillator of a television receiver to the line frequency horizontal synchronization pulses received by said television receiver, the method comprising:

receiving said horizontal synchronisation pulses in a first phase detector (30) and producing an output therefrom,

controlling the oscillator (34) frequency in accordance with said first phase detector output.

generating from said first phase detector output a ramp waveform,

generating from said ramp waveform in a first divide by two circuit (38) a switching waveform, and

applying said switching waveform to said first phase detector so as to lock said oscillator to said horizontal synchronisation pulses, and

generating from said oscillator output flyback pulses.

characterised by

said ramp waveform having a frequency substantially equal to twice said line frequency, and

locking said flyback pulses in a second phase detector (40) and producing an output therefrom, slicing said ramp waveform in dependence on said second phase detector output to produce a sliced signal having a frequency substantially equal to said ramp waveform, generating from said sliced signal in a second divide by two circuit (46) a fifty percent duty cycle waveform having a frequency substantially equal to said line frequency, and using said fifty percent duty cycle waveform in generating said flyback pulses.

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Patentansprüche

1. Horizontal-Phasenverriegelungsschleife zur Verwendung in einem Fernsehempfänger, die Horizontalsynchronimpulse der Bildzeilenfrequenz empfängt und die eine Horizontalausgangsstufe (48) zur Erzeugung von Zeilenrücklaufimpulsen enthält;

mit einer ersten Schleife, die einen ersten Phasendetektor (30), einen Oszillator (34) und eine erste durch zwei teilende Schaltung (38) enthält; und einer zweiten Schleife, die einen zweten Phasendetktor (40) enthält; wobei der erste Phasendetektor (30) einen ersten Eingang, der die Synchronisationsimpulse empfängt und einen zweiten Eingang aufweist; der Oszillator (34) einen ersten Eingang aufweist, der mit einem Ausgang des ersten Phasendetektors (30) verbunden ist, um eine Rampenwellenform zu erzeugen, wobei der Ausgang des ersten Phasendetektors die Frequenz des Oszillators verändert; die erste durch zwei teilende Schaltung (38) einen Eingang aufweist, der mit der Rampenwellenform verbunden ist, um eine schaltende Wellenform zu erzeugen, wobei der zweite Eingang des ersten Phasendetektors diese schaltende Wellenform empfängt; die erste Schleife den Oszillator auf die Horizontalsynchronimpulse verriegelt; wobei die horizontale Phasenverriegelungsschleife dadurch gekennzeichnet ist, daß die Rampenwellenform eine Frequenz aufweist, die im wesentlichen gleich dem Doppelten der Zeilenfrequenz ist; die zweite Schleife die Zeilenrücklaufimpulse auf die Schaltende Wellenform verriegelt, die zweite Schleife weiterhin eine erste Einrichtung (44) und eine zweite durch zwei teilende Schaltung (46) enthält; der zweite Phasendetektor (40) einen ersten Eingang, der mit der schaltenden Wellenform verbunden ist, und einen zweiten Eingang, der die Zeilenrücklaufimpulse empfängt, aufweist; die erste einrichtung (44) einen ersten Eingang, der mit der Rampenwellenform verbunden ist und einen zweiten Eingang, der mit einem Ausgang des zweiten Phasendetectors (40) verbunden ist, aufweist, um die Rampenwellenform zu zerschneiden und einen Ausgang zu erzeugen, der eine Frequenz aufweist, die im wesentlichen gleich der der Rampenwellenform ist; die zweite durch zwei teilende Schaltung (46) einen Eingang aufweist, der mit dem Ausgang der ersten Einrichtung (44) verbunden ist, und einen Ausgang aufweist, der mit der Horizontalausgangsstufe (48) zur Erzeugung einer Treiberwellenform mit einem Tastverhältnis von 50%, deren Frequenz im wesentlichen gleich der der Zeilenfrequenz ist, verbunden ist.

2. Horizontal-Phasenverriegelungsschleife nach Anspurch 1, weiterhin dadurch gekennzeichnet, daß die Synchronisationsimpulse auf einen Punkt auf dem genannten Rampensignal verriegelt sind.

3. Horizontal-Phasenverriegelungsschleife nach Anspruch 1 oder 2, weiterhin dadurch gekennzeichnet, daß die erste Schleife weiterhin eine Komparatorschaltung (36) aufweist, die zwischen den Oszillator (34) und die erste, durch zwei teilende Schaltung (38) geschaltet ist, um ein erstes Signal zu erzeugen, das eine Frequenz hat, die im wesentlichen gleich der des Oszillators ist.

4. Verfahren zum Verriegeln des Horizontaloszillators eines Fernsehempfängers auf die Zeilenfrequenz-Horizontalsynchronimpulse, die von dem Fernsehempfänger empfangen werden, enthaltend:

Empfangen der Horizontalsynchronimpulse in einem ersten Phasendetektor (30) und erzeugen eines Ausgangs davon,

Regeln der Oszillatorfrequenz (34) in übereinstimmung mit dem Ausgang des ersten Phasendetektors,

Erzeugen einer Rampenwellenform aus dem Ausgang des ersten Phasendetektors,

Erzeugen einer Schaltenden Wellenform aus der genannten Rampenwellenform in einer ersten durch zwei teilenden Schaltung (38), und

Anlegen der schaltenden Wellenform an den ersten Phasendetektor, um den Oszillator auf die Horizontalsynchronimpulse zu verriegeln und

Erzeugen von Zeilenrücklaufimpulsen aus dem Oszillatorausgang,

dadurch gekennzeichnet,

daß die Rampenwellenform eine Frequenz hat, die im wesentlichen gleich dem Zweifachen der Zeilenfrequenz ist und

Verriegeln der Zeilenrücklaufimpulse in einem zweiten Phasendetektor (40) und Erzeugen eines Ausgangs daraus, Zerschneiden der Rampenwellenform im Abhängigkeit vom Ausgang des zweiten Phasendetektors, um ein zerschnittenes Signal zu erzeugen, das eine Frequenz hat, die im wesentlichen gleich der der Rampenwellenform ist, Erzeugen aus dem zerschnittenen Signal in einer zweiten durch zwei teilenden Schaltung (46) eine Wellenform mit 50% Tastverhältnis, die eine Frequenz aufweist, die im wesentlichen gleich der Zeilenfrequenz ist, und Verwenden der genannten Wellenform mit 50% Tastverhältnis bei der Erzeugung der Zeilenrücklaufimpulse.

Revendications

1. Boucle à verrouillage de phase horizontale destinée à un récepteur de télévision du type qui reçoit des impulsions de synchronisation horizontale à la fréquence des lignes d'image et qui comporte un étage de sortie horizontal (48) pour produire des impulsions de retour; une première boucle comportant un premier détecteur de phase (30), un oscillateur (34) et un premier circuit diviseur par deux (38); et une seconde boucle comportant un second détecteur de phase (40); ledit premier détecteur de phase (30) ayant une première entrée couplée pour recevoir lesdites impulsions de synchronisation et une seconde entrée; ledit oscillateur (34) ayant une première entrée couplée avec une sortie dudit premier détecteur de phase (30) pour produire une forme d'onde en dent de scie, ladite sortie dudit premier détecteur de phase modifiant la fréquence dudit oscillateur; ledit premier circuit diviseur par deux (38) ayant une entrée couplée avec ladite forme

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d'onde en dent de scie pour produire une forme d'onde de commutation, ladite second entrée dudit premier détecteur de phase recevant ladite forme d'onde de commutation; ladite première boucle verrouillant ledit oscillateur sur lesdites impulsions de synchronisation horizontale; ladite boucle à verrouillage de phase horizontale étant caractérisée par le fait que ladit forme d'onde en dent de scie a une fréquence pratiquement égale au double de ladite fréquence de ligne; que ladite second boucle verrouille lesdites impulsions de retour sur ladite forme d'onde de commutation, ladite seconde boucle comportant en outre un premier dispositif (44) et un second circuit diviseur par deux (46); ledit second détecteur de phase (40) ayant une première entrée couplée avec ladite forme d'onde de commutation et une seconde entrée couplée pour recevoir lesdites impulsions de retour; ledit premier dispositif (44) ayant une première entrée couplée avec ladite forme d'onde en dent de scie et une seconde entrée couplée avec une sortie dudit second détecteur de phase (40) pour limiter ladite forme d'onde en dent de scie et produire une sortie ayant une fréquence pratiquement étale à ladite forme d'onde en dent de scie; le second circuit diviseur par deux (46) ayant une entrée couplée avec la sortie dudit premier dispositif (44) et une sortie couplée avec ledit étage de sortie horizontale (48) pour produire une forme d'onde d'attaque à rapport d'impulsions de cinquante pourcent ayant une fréquence pratiquement égale à ladite fréquence de ligne.

2. Boucle à verrouillage de phase horizontale selon la revendication 1, caractérisée en outre en ce que les impulsions de synchronisation sont verrouillées sur un point dudit signal en dent de scie.

3. Boucle à verrouillage de phase horizontale selon la revendication 1 ou 2, caractérisée en outre en ce que ladite première boucle comporte en outre un circuit comparateur (36) couplé entre ledit oscillateur (34) et ledit premier circuit diviseur par deux (38) pour produire un premier signal ayant une fréquence pratiquement égale à celle dudit oscillateur.

4. Procédé de verrouillage de l'oscillateur horizontal d'un récepteur de télévision sur les impulsions de synchronisation horizontale à la fréquence de ligne reçues par ledit récepteur de télévision, le procédé consistant:

à recevoir lesdites impulsions de synchronisation horizontale dans un premier détecteur de phase (30) et à produire une sortie à partir de ces dernières,

à commander la fréquence de l'oscillateur (34) en fonction de la sortie dudit premier détecteur de phase,

à produire, à partir de la sortie dudit premier détecteur de phase, une forme d'onde en dent de scie,

à produire, à partie de ladite forme d'onde en dent de scie et dans un premier diviseur par deux (38) une forme d'onde de commutation, et

à appliquer ladite forme d'onde de commutation audit premier détecteur de phase de manière à verrouiller ledit oscillateur sur lesdites impulsions de synchronisation horizontale, et

à produire à partir de la sortie dudit oscillateur des impulsions de retour,

caractérisée en ce que ladite forme d'onde en dent de scie a une fréquence pratiquement égale au double de ladite fréquence de ligne, et

en ce qu'il consiste à verrouiller lesdites impulsions de retour dans un second détecteur de phase (40) et à produire une sortie à partir d'elles, à limiter ladite forme d'onde en dent de scie en fonction de la sortie dudit second detecteur de phase pour produire un signal limité ayant une fréquence pratiquement égale à ladite forme d'onde en dent de scie, à produire à partir dudit signal limité, dans un second crcuit diviseur par deux (46) une forme d'onde à rapport d'impulsions de cinquante pour-cent ayant une fréquence pratiquement égale à ladite fréquence de ligne et à utiliser ladite forme d'onde à rapport d'impulsions de cinquante pourcent pour produire lesdites impulsions de retour.

* C L M S *