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METHOD AND APPARATUS FOR PERFORMING A FAST HADAMARD TRANSFORM

BACKGROUND OF THE INVENTION

I. Field of the Invention

The present invention relates to digital signal processing. More particularly, the present invention relates to a novel and improved method and apparatus for performing fast Hadamard transformations.

II. Description of the Related Art

Waveform coding procedures transform a waveform set into an improved waveform set. The improved waveform set can then be used to provide improved probability of bit error P_B compared to the original set upon communication. In the improved waveform set the signals are as unlike as possible. Another way of viewing this is to render the cross-correlation between any two waveforms i and j (denoted z_{ij}) as small as possible.

The cross correlation (z_{ij}) is defined as:

$$z_{ij} = \frac{1}{E}\int_0^T s_i(t)s_j(t)dt, \qquad i \neq j \tag{1}$$

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$$\text{and } E = \int_0^T (s_i)^2(t)dt, \qquad \forall\, i.$$

where $s_i(t)$ and $s_j(t)$ are two waveform functions. In a waveform set comprised of bipolar pulses (+1,-1), the definition of the cross-correlation (z_{ij}) can be simplified to:

$$z_{ij} = \frac{\text{number of agreements} - \text{number of disagreements}}{\text{total number of digits}} \tag{2}$$

The smallest possible value of the cross-correlation occurs when the signals are anticorrelated (z_{ij}= -1); however, this can only be achieved when the number of waveforms in the set are two and the waveforms are antipodal. In general, the best achievable waveform set has all the cross-

correlation values equal to zero. The set is then said to be orthogonal. The most popular waveform codes used for communication purposes are orthogonal codes.

One method by which a data set can be transformed into an orthogonal data set is by means of a Hadamard transformation. A Hadamard transformation is characterized by a Hadamard matrix, in which each row of the Hadamard matrix is orthogonal to every other row of the matrix, that is in accordance with equation 2, the number of agreements equals the number of disagreements for each pair of rows. Each row of the Hadamard matrix can be referred to as a Walsh sequence.

A Hadamard matrix of order n can be defined recursively as follows:

$$H_{2n} = \begin{bmatrix} H_n & H_n \\ H_n & H'_n \end{bmatrix} \tag{3}$$

where H_1 is defined as:

$$H_1 = [1] \tag{4}$$

and $H'_i = -H_i$.

Thus,

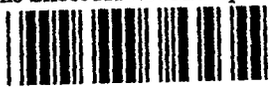
$$H_2 = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}. \tag{5}$$

Similarly, by application of equation 3, H_4 is found to be:

$$H_4 = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \tag{6}$$

and H_8 is found to be:

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$$H_8 = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 & 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 \\ 1 & -1 & 1 & -1 & -1 & 1 & -1 & 1 \\ 1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 \end{bmatrix} \quad (7)$$

Fast algorithms have been developed to increase the efficiency of in the performance of Hadamard transformations. These implementations exploit the fact that Hadamard matrices are real, symmetric and row-wise orthogonal. Since the Hadamard matrices contain only ±1 values, no multiplications are required in the transform calculations. Moreover the number of additions and subtractions required can be reduced from n^2 to $n \bullet \log_2 n$, due to the fact that a Hadamard matrix of order n (H_n) can be written as a product of n sparse matrices, that is,

$$H_n = \tilde{H}_n^{\log_2(n)} \quad (8)$$

where

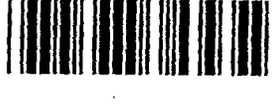
$$\tilde{H}_n = \begin{bmatrix} 1 & 1 & 0 & 0 & .. & .. & .. & .. \\ 0 & 0 & 1 & 1 & .. & .. & .. & .. \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & .. & .. & .. & .. & 1 & 1 \\ 1 & -1 & 0 & 0 & .. & .. & .. & .. \\ 0 & 0 & 1 & -1 & .. & .. & .. & .. \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ .. & .. & .. & .. & .. & .. & 1 & -1 \end{bmatrix} \quad (9)$$

(n columns; n rows)

Noting that the top n/2 rows and the bottom n/2 rows contain only two nonzero terms per row, the transformation

$$v = \tilde{H}_n^{\log_2(n)} = \tilde{H}_n \cdot \tilde{H}_n \ldots \tilde{H}_n \cdot u \quad (10)$$

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can be accomplished by operating $\tilde{H}_n$ $\log_2 n$ times on u. Due to the structure of $\tilde{H}_n$ only n additions and subtractions are required each time $\tilde{H}_n$ operates on a vector, giving a total of $n \cdot \log_2(n)$ additions and subtractions.

The problem associated in the implementation of the fast Hadamard transformation described above is the burden on memory resources. In addition, the method described above does not lend itself to serial processing. Accordingly, there is a need for an improved method and apparatus for performing fast Hadamard transforms that lessen the burden on memory resources and lends itself to serial processing. Such a method is the subject of the present invention.

SUMMARY OF THE INVENTION

The present invention is a novel and improved method and apparatus for performing a fast Hadamard transform. A Hadamard transform of order 2 can be performed by an element that receives two input values a and b, and in response outputs two values (a+b) and (a-b). This element can be realized in hardware with one adder and one subtractor, two multiplexers, and a memory element.

The element described above can be achieved by providing the inputs serially to a subtracting input of the subtractor to a summing input of the adder, and to the B input of the first multiplexer. The output of the subtractor is provided to the A input of the first multiplexer, and the output of the adder is provided to the A input of the second multiplexer. The output of the first multiplexer is provided to the input of the memory element. The output of the memory element is then coupled to the summing input of the subtractor, to the second summing input of the adder, and to the B input of the second multiplexer. The output is then provided serially at the output of the second multiplexer.

Now in order to provide a means for performing a Hadamard transform of order 4. The fundamental element described above is placed in series with another such element slightly modified. The second element in the series is modified by having a second memory element placed in series with the first memory element, such that the output from the first multiplexer would first be stored in the first memory element, then at the next clock cycle the data stored in the first memory element would be shifted to the second memory element before being provided to the

summing inputs of the subtractor and adder and the B input of the second multiplexer on the next clock cycle.

By extension a Hadamard transformation of order 8 could be provided by adding on a third modified element, this time with four memory elements in series, and so on. The number of memory elements of the last Hadamard element will have a number of memory elements equal to half the order of the Hadamard order. It is important to note that the memory requirements of these memory elements are not the same. This is because the sum of two m bit numbers is an m+1 bit number. So the memory elements at each successive element stage is required to hold a number of accuracy one bit greater than the memory elements of the preceding element.

In order to provide savings in the memory necessary to perform this operation, as a further improvement on the previously described means the order of the elements can be reversed. For example, in the case of the Hadamard transform of order 8, the first element can have four memory elements, with memory element (m+1) bits wide where m is the number of bits in the input. The next element will have two (m+2) wide memory elements and the final element in the series will have a single (m+3) wide memory element.

It is therefore an objective of the present invention to provide a means for performing the Hadamard transformations using simplified hardware. By using single bit adders with a carry resource, a Hadamard transformation can be performed where the inputs are serialized to the transformer one bit at a time.

It is a further objective of the present invention to provide method and means for an additional savings in memory achieved through efficient truncation of values stored in the memory elements described above.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, objects, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

Figure 1 is a block diagram of the Hadamard transformation apparatus for performing a Hadamard transform of order 4;

Figure 2 is a block diagram of the Hadamard transformation apparatus for performing a Hadamard transform of order 64;

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Figure 3 is a block diagram of an improved implementation of Hadamard transformation apparatus for performing a Hadamard transform of order 64; and

Figure 4 is block diagram of a serial input FHT stage.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is a method and apparatus for performing a Fast Hadamard Transform (FHT). In Figure 1, an exemplary embodiment of the present invention is illustrated for the purpose of performing a Hadamard transform of order 4. For example, if a block of four digital samples (a_1, a_2, a_3, a_4) constitute an input symbol, the apparatus shown in Figure 3 performs an FHT on the input symbol to provide an FHT encoded symbol in accordance with Equation 11 below:

$$\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \times \begin{bmatrix} a1 \\ a2 \\ a3 \\ a4 \end{bmatrix} =$$

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$$[(a1+a2+a3+a4),(a1-a2+a3-a4),(a1+a2-a3-a4),(a1-a2-a3+a4)] \quad (11)$$

It should be noted that the dimension of four used in the exemplary embodiment is for exemplary representation and that the method and apparatus of the present invention is equally applicable to fast Hadamard transformations (FHT) of all defined dimension.

In the exemplary embodiment each of the digital samples (a_1, a_2, a_3, and a_4) are 8 bit representations, though any other bit length is equally applicable to the present invention. The first input sample a_1 is provided on the input signal line. Input sample a_1 is provided to the subtracting input of subtractor 2 (an adder configured for subtraction), the first input of summer 6, and input B of multiplexer 4. Multiplexer 4 provides to its output either the signal on the input signal line or the output from subtractor 2. On the first input cycle, multiplexer 4 output provides the signal on the input signal line. On the second input cycle, multiplexer 4 output provides the signal from subtractor 2 output to its output, and alternates in this fashion each input cycle. Thus for the first input cycle,

multiplexer 4 provides sample a_1 at its output, which is received at and stored in memory element 10.

On the second input cycle, the next input sample a_2 is provided to the subtracting input of the subtractor 2, the first input of summer 6, and input B of multiplexer 4. The stored value in memory element 10, a_1, is provided to the adding input of subtractor 2, to the second input of summer 6, and to input B of multiplexer 8. In response subtractor 2 provides the value of (a_1-a_2) at its output, which is also presented at the output of multiplexer 4 and stored in memory element 10. Summer 6 provides the value of (a_1+a_2) at its output. Multiplexer 8 provides at its output either the output from summer 6 or the output from memory element 10. On the second input cycle multiplexer 8 provides the output from summer 6 at its output, on the third input cycle it provides the output from memory element 10 at its output and alternates between providing these signals to its outputs each input cycle. Thus for the second input cycle, multiplexer 8 provides at its output the value output from summer 6, (a_1+a_2).

The output of multiplexer 8, (a_1+a_2), is provided to the subtracting input of subtractor 12, the first input of summer 16, and the B input to multiplexer 14. Multiplexer 14 provides at its output the signal from the output of multiplexer 8 for the second and third input cycles, then it provides the output from summer 12 for the fourth and fifth input cycles, and alternates every two cycles thereforth. Thus for the second input cycle, multiplexer 14 provides the signal output from multiplexer 8, (a_1+a_2), to memory element 20 where it is stored.

During the third input cycle the sample a_3 is provided to the subtracting input of subtractor 2, the first input of summer 6, and input B of multiplexer 4. Memory element 10 provides its stored value (a_1-a_2) to the adding input of subtractor 2, to the second input of summer 6, and to the B input of multiplexer 8. Multiplexer 4 provides the value from the input signal line, a_3, to memory element 10 where it is stored. Multiplexer 8 provides the signal on its B input (a_1-a_2) at its output.

The value output by multiplexer 8, (a_1-a_2), is provided to the subtracting input of subtractor 12, the first input of summer 16, and the B input to multiplexer 14. Memory element 20 transfers its contents (a_1+a_2) to memory element 22. Multiplexer 14 provides the output signal from multiplexer 8, (a_1-a_2), to memory element 20.

In the forth cycle, the next input sample a_4 is provided to the subtracting input of subtractor 2, the first input of summer 6, and input B of multiplexer 4. Memory element 10 provides its stored value, a_3, to the

adding input of subtractor 2, to the second input of summer 6, and to the B input of multiplexer 8. Summer 2 provides (a_3-a_4) to the A input of multiplexer 4. Multiplexer 4 provides the output from subtractor 2, (a_3-a_4), to memory element 10 where it is stored. Summer 6 provides the sum (a_3+a_4) to the A input of Multiplexer 8. Multiplexer 8 provides the signal output from summer 6, (a_3+a_4), at its output.

The value output by multiplexer 8, (a_3+a_4), is provided to the subtracting input of subtractor 12, the first input of summer 16, and the B input to multiplexer 14. Memory element 22 then provides its contents, (a_1+a_2), to the adding input of subtractor 12, the second input of summer 16 and the B input of multiplexer 18. Memory element 20 transfers its contents, (a_1+a_2), to memory element 22. Summer 12 in response provides the sum of its inputs (a_1+a_2)-(a_3+a_4) to the A input of multiplexer 14. Multiplexer 14 provides the value output by subtractor 12, (a_1+a_2)-(a_3+a_4), to memory element 20 where it is stored. Summer 16 then provides the sum of its two inputs (a_1+a_2)+(a_3+a_4), to the A input of multiplexer 18. Multiplexer 18 provides the signal output by summer 16 for input cycles 4 and 5, then provides the output from memory element 22 as output for input cycles 6 and 7, and alternates every two cycles thereforth. Multiplexer 18 provides the desired sum (a_1+a_2+a_3+a_4) as the first output of the second stage of the FHT apparatus.

In the fifth input cycle, the next input sample a_5 is provided to the subtracting input of the subtractor 2, the first input of summer 6, and input B of multiplexer 4. Memory element 10 provides its stored value (a_3-a_4) to the adding input of summer 2, to the second input of summer 6, and to the B input of multiplexer 8. Multiplexer 4 provides the value on the input signal line, a_5, to memory element 10 where it is stored. Multiplexer 8, provides the signal, output from memory element 10, (a_3-a_4), at its output.

The value at the output of multiplexer 8, (a_3-a_4), is provided to the subtracting input of summer 12, the first input of summer 16, and the B input to multiplexer 14. Memory element 22 provides its contents, (a_1-a_2), to the adding input of subtractor 12, the second input of summer 16 and the B input of multiplexer 18. Memory element 20 transfers its contents, (a_1+a_2)-(a_3+a_4), to memory element 22. Subtractor 12 provides (a_1-a_2)-(a_3-a_4) to the first input of multiplexer 14 which provides this value to memory element 20. Likewise summer 16 provides (a_1-a_2)+(a_3-a_4), or (a_1-a_2+a_3-a_4), to the first input of multiplexer 18, which provides this value at its output.

In the sixth input cycle, the next input sample a_6 is provided to the subtracting input of the subtractor 2, the first input of summer 6, and input

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B of multiplexer 4. Memory element 10 provides its stored value, a_5, to the adding input of subtractor 2, to the second input of summer 6, and to the B input of multiplexer 8. Subtractor 2 provides (a_5-a_6) to the A input of multiplexer 4. Multiplexer 4 provides the value on its A input, (a_5-a_6), to memory element 10 where it is stored. Summer 6 provides (a_5+a_6) to the A input of Multiplexer 8. Multiplexer 8 provides the signal on its A input, (a_5+a_6), at its output.

The output from multiplexer 8, (a_5+a_6), is provided to the subtracting input of subtractor 12, the first input of summer 16, and the B input to multiplexer 14. Memory element 22 then provides its contents, $(a_1+a_2)-(a_3+a_4)$, to the adding input of subtractor 12, the second input of summer 16 and the B input of multiplexer 18. Memory element 20 transfers its contents, $(a_1-a_2)-(a_3-a_4)$, to memory element 22. Multiplexer 14 provides its B input signal (a_5+a_6) to memory element 20 where it is stored. Multiplexer 18 provides the value of the B input signal, $(a_1+a_2)-(a_3+a_4)=(a_1+a_2-a_3-a_4)$, at its output.

In the seventh input cycle, the next input sample a_7 is provided to the subtracting input of subtractor 2, the first input of summer 6, and input B of multiplexer 4. Memory element 10 provides its stored value, (a_5-a_6), to the adding input of summer 2, to the second input of summer 6, and to the B input of multiplexer 8. Multiplexer 4 provides the value on the B input, a_7, to memory element 10 where it is stored. Multiplexer 8 provides the signal on its B input, (a_5-a_6), at its output

The output of multiplexer 8, (a_5-a_6), is provided to the subtracting input of subtractor 12, the first input of summer 16, and the B input to multiplexer 14. Memory element 22 then provides its contents, $(a_1-a_2)-(a_3-a_4)$, to the adding input of subtractor 12, the second input of summer 16 and the B input of multiplexer 18. Memory element 20 transfers its contents, (a_5+a_6), to memory element 22. Multiplexer 14 provides its B input signal, (a_5-a_6), to memory element 20 where it is stored. Multiplexer 18 provides the value of the B input signal, $(a_1-a_2)-(a_3-a_4)=(a_1-a_2-a_3+a_4)$, at its output.

Note that the FHT of the input sequence (a_1,a_2,a_3,a_4), $(a_1+a_2+a_3+a_4, a_1-a_2+a_3-a_4, a_1+a_2-a_3-a_4, a_1+a_2-a_3-a_4)$ has been successfully output by the apparatus. By inputting the next in the series to the apparatus, a_8, the first element of the FHT of input sequence (a_5,a_6,a_7,a_8), which is $a_5+a_6+a_7+a_8$ appears at the output of the apparatus. The process can be continued indefinitely.

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The fundamental element of the FHT apparatus is the shown in the dashed lines of block 24. Block 24 is composed of one subtractor 12, one summer 16 and two multiplexers (multiplexers 14 and 18), this subsystem is referred to as the FHT engine. Note that the subtractor is a summer with an inverting input. In combination with the memory devices or memory elements they makeup a complete FHT stage. Additional stages can be added on by providing an output of a previous stage to an added stage. The only difference between a stage and its previous stage is the number of memory elements doubles (also the number of bits in a given memory element must increase by one) and the timing of the memory elements changes switching only half as often as the previous stage.

In Figure 2, a block diagram of an FHT an apparatus for performing an FHT of order 64 is illustrated. The FHT engines 30, 34, 38, 42, 46 and 50 are all identical to the FHT engine illustrated in detail in block 24 of Figure 1, and memory devices 32, 36, 40, 44, 48 and 52 are a plurality of interconnected memory elements or data latches, such as formed by a shift register, also as described in Figure 1. In the exemplary embodiment, the data input into FHT engine 30 is comprised of eight bit numbers, though the present invention is equally applicable to data of any bit length.

Since in this exemplary embodiment the input data stream is comprised of 8 bit/sample data, the memory element in memory device 32 must be able to hold nine bits to accommodate the possible outputs of FHT engine 30 without truncation, since the sum of two n-bit numbers is an (n+1)-bit number. Similarly, the memory elements of memory device 36 must be able to store 10 bits. The memory elements of memory device 40 must be able to store 11 bits; those of memory device 44 must be able to store 12 bits; those of memory device 48 must be able to store 13 bits and the memory elements of memory device 52 must be able to store 14 bits.

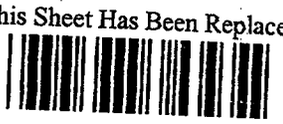
Figure 3 illustrates an improved embodiment of the present invention. The apparatus shown in Figure 3 performs a fast Hadamard transform of order 64. The FHT engines 90, 94, 98, 102, 106 and 110 are identical in construction to the FHT engine 24 shown in detail in Figure 1. The only difference that occurs in the operation of the FHT engines in Figure 3 as opposed to those shown in Figure 2 occurs in the switching of the multiplexers (not shown) of FHT engines 90, 94, 98, 102, 106 and 110. The multiplexers of the first stage FHT engine 90 switch only every 32 input cycles. The multiplexers of FHT of the second stage FHT engine 94 switch every 16 input cycles. The multiplexers of the last stage FHT engine 110 switch every input cycle.

The significant difference between the improved embodiment illustrated in Figure 3 and the embodiment illustrated in Figure 2 is the savings in total memory used. Recalling the exemplary embodiment for processing data of bit length eight, the first memory device had to be capable of storing a nine bit number the next, whereas the memory devices of the next stage would need to store a ten bit number. Therefore, in this improved embodiment the stages where the memory devices are required to store the lowest number of bits are used to store the largest number of values. Memory device 92 stores thirty-two 9-bit numbers, device 96 sixteen 10-bit numbers, device 100 eight 11-bit numbers, device 104 four 12-bit numbers, device 108 two 13-bit numbers and device 112 one 14-bit number. The number of bits of memory saved using this improved embodiment can be calculated by the formula below:

$$\begin{aligned} \#\text{ of bits saved} &= \sum_{i=1}^{\log_2(n)} (m+i)2^{i-1} - (m+i)\cdot 2^{\log_2 n - i} \\ &= \sum_{i=1}^{\log_2(n)} (m+i)\cdot (2^{\log_2(n)-i} - 2^{i-1}). \end{aligned} \tag{12}$$

where n is the order of the FHT being performed and m is the number of bits per input.

In Figure 4, an alternative implementation of the present invention is illustrated for receiving samples as a serial bit stream. In this implementation the bits that comprise the input samples are provided to the FHT apparatus serially. For each input sample, the bits of the sample are provided to the FHT engine least significant bit (LSB) to most significant bit (MSB). An input bit is provided to the first subtracting input of subtractor 120, a B input of multiplexer 124, and the first adding input of adder 128. In addition, the output data from the memory element 126 is provided to the adding input of subtractor 120. The last input to subtractor 120, a second subtracting input, is the borrow bit from the previous operation, which is provided by delay 122. Delay elements 122 and 130 provide a delay equal to a single bit period in duration. Subtractor 120 then subtracts the delayed borrow bit and the current subtracting input bit from the adding bit. This operation provides two bits of output data, including a borrow bit which is provided to delay 122, and a difference bit which is provided to the A input of multiplexer 124.



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Multiplexer 124 selects the data on one of its two inputs for providing to its output. The switching cycles of the multiplexers 124 and 132 are the same as described previously noting of course that an input cycle is defined as the time period required to provide all bits comprising an input sample. As previously mentioned the input bit is provided to the first adding input of adder 128. The output of the memory element 126 is also provided to a second adding input of adder 128. In addition, a delayed carry bit from the previous summing operation of adder 128 is provided by delay 130 to the third adding input of adder 128. The sum of the three inputs (the delayed carry, the input bit and the output bit from the memory element) are summed to provide two bits of data. The first bit, the carry bit, is provided to delay element 130 and the sum bit is provided to the A input of multiplexer 132. Multiplexer 132 also receives at its B input the output bit of memory element 126. Multiplexer 132 then selects the data on one of its two inputs to provide at its output as a bit of one of the FHT coefficients in accordance with the switching operation described above.

A final method that can be used alone or in combination with the above mentioned improvements is by means of truncation. When the data is provided in a parallel fashion to the FHT apparatus, truncation can be achieved by simply providing only a predetermined number of most significant bits of data to the memory elements. In the case where the data provided to the FHT apparatus is a serial stream, the bits provided least significant bit first to a memory element are shifted into and eventually out of the first memory element behaving as a serially loaded parallel output shift register. When only the most significant bits remain in the memory element, truncation is achieved, and these bits can then be parallel shifted to the next memory element.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

I CLAIM:

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CLAIMS

1. An apparatus for performing a Hadamard transform operation comprising:

plurality of successively coupled FHT engine means for receiving a corresponding input symbol and a corresponding delayed processed symbol, subtracting said input from said delayed processed symbol to provide a difference symbol, selecting a processed symbol from said difference symbol and said input symbol according to a predetermined selection format, summing said delayed processed symbol with said previous FHT engine means output symbol to provide a sum symbol, and selecting and providing an input symbol to a subsequent FHT engine means from said delayed processed symbol and said sum symbol with a last FHT engine means providing an output symbol; and

plurality of delay means coupled to a corresponding one of said plurality of FHT engine means for receiving said processed symbol and delaying said processed symbol by a corresponding predetermined delay format to provide said delayed processed symbol.

2. The apparatus of Claim 1 wherein each of said plurality of FHT engine means comprises:

difference means for receiving said input symbol and said delayed processed symbol and for subtracting said input symbol from said delayed processed symbol to provide said difference symbol;

first multiplexer means for receiving said difference symbol and said input symbol and providing one of said difference symbol and said input symbol as said processed symbol in accordance with a first predetermined selection format;

summing means for receiving and summing said input symbol and said delayed processed symbol to provide said sum symbol; and

multiplexer means for receiving said sum symbol and said delayed processed symbol and providing one of said sum symbol and said delayed processed symbol in accordance with a second predetermined selection format.

3. The apparatus of Claim 1 wherein each delay means of said plurality of delay means delays said processed symbol by a delay duration twice the delay duration of the delay means coupled to the previous FHT engine.

4. The apparatus of Claim 1 wherein each delay means of said plurality of delay means delays said processed symbol by a delay duration half the delay duration of the delay means coupled to the previous FHT engine.

5. The apparatus of Claim 1 wherein said input symbol is provided serially and wherein each of said plurality of FHT engines comprises:

difference means for receiving a delayed borrow signal, said delayed processed symbol, and said input symbol and subtracting said delayed borrow symbol and said input symbol from a bit of said delayed processed symbol to provide said difference symbol and a borrow symbol;

first delay means for receiving said borrow symbol and delaying said borrow symbol according to a predetermined duration to provide said delayed borrow symbol;

first multiplexer means for receiving said input symbol and said difference symbol and providing one of said input symbol and said difference symbol as said processed symbol according to a predetermined selection format;

summing means for receiving ad summing said input symbol, said delayed processed symbol and a delayed carry symbol to provide said sum symbol and a carry symbol;

second delay means for receiving said carry symbol and delaying said carry symbol by a predetermined duration to provide said delayed carry symbol; and

second multiplexer means for receiving said delayed processed symbol and said sum symbol and providing one of said sum symbol and said delayed processed symbol as said input symbol for a subsequent stage.

6. A method for performing a Hadamard transformation comprising the repeated steps of:

receiving an input symbol;

subtracting said input symbol from a delayed processed symbol to provide a difference symbol;

selecting a processed symbol from said difference and said input symbol in accordance with a predetermined selection format;

delaying said processed symbol by a predetermined duration to provide said delayed processed symbol;

summing said processed symbol with said input symbol to provide a sum symbol; and

selecting an output symbol from said sum and said delayed processed symbol in accordance with a second predetermined selection format.

7. The method of Claim 6 wherein said step of delaying said processed symbol comprises the steps of:

shifting a plurality of stored processed symbols into arrays with different indices;

storing said processed symbol into an array of an initial index; and

wherein the stored processed symbol stored in an array with a final index is provided as said delayed processed symbol.

8. The method of Claim 6 wherein said step of receiving said input symbol comprises receiving the bits of said input symbol serially;

wherein said step of subtracting said input symbol from a delayed processed symbol further comprises subtracting a borrow symbol from said delayed processed symbol and further comprises providing said borrow symbol in accordance with said step of subtracting; and

wherein said step of summing said processed symbol with said input symbol further comprise summing a carry symbol with said processed symbol and said input symbol to further provide carry symbol.

9. An apparatus for performing a Hadamard transform operation comprising:

a plurality of FHT engine means with a first FHT engine means having two inputs with a first input for receiving an input symbol and having two outputs with a first output for providing a processed symbol and a plurality of additional FHT engine means successively coupled having two inputs with a first input coupled to a second output of a previous FHT engine; and

a plurality of delay means with a first delay means having an input coupled to a second output of said first FHT engine and having an output coupled to a second input of said first FHT engine means and a plurality of additional delay means having an input coupled to a second output of a corresponding additional FHT engine and having an output coupled to a second input of a corresponding additional FHT engine.

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10. The apparatus of Claim 9 wherein each of said plurality of FHT engine means comprises:

a difference means having two inputs with a first input for receiving said input symbol and having an output;

a first multiplexer means having two inputs and an output with a first input for receiving said input symbol and a second input coupled to said difference means output;

a summing means having two inputs with a first input for receiving said input symbol and having an output; and

a second multiplexer means having a first input coupled to said summing means output.

11. The apparatus of Claim 10 wherein said difference means further comprises a third input and a second output and wherein said summing means further comprises a third input and a second output, said apparatus further comprising:

a third delay means having an input coupled to said difference means second output and having an output coupled to said difference means third input; and

a fourth delay means having an input coupled to said summing means second output and having an output coupled to said summing means third input.

12. An circuit for performing a Hadamard transform operation comprising:

a plurality of successively coupled FHT engine circuits for receiving a corresponding input symbol and a corresponding delayed processed symbol, subtracting said input from said delayed processed symbol to provide a difference symbol, selecting a processed symbol from said difference symbol and said input symbol according to a predetermined selection format, summing said delayed processed symbol with said previous FHT engine circuit output symbol to provide a sum symbol, and selecting and providing an input symbol to a subsequent FHT engine circuit from said delayed processed symbol and said sum symbol with a last FHT engine circuit providing an output symbol; and

a plurality of delay circuits coupled to a corresponding one of said plurality of FHT engine circuits for receiving said processed symbol and delaying said processed symbol by a corresponding predetermined delay format to provide said delayed processed symbol.

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13. The circuit of Claim 12 wherein each of said plurality of FHT engine circuit comprises:

a difference circuit for receiving said input symbol and said delayed processed symbol and for subtracting said input symbol from said delayed processed symbol to provide said difference symbol;

a first multiplexer circuit for receiving said difference symbol and said input symbol and providing one of said difference symbol and said input symbol as said processed symbol in accordance with a first predetermined selection format;

a summing circuit for receiving and summing said input symbol and said delayed processed symbol to provide said sum symbol; and

a multiplexer circuit for receiving said sum symbol and said delayed processed symbol and providing one of said sum symbol and said delayed processed symbol in accordance with a second predetermined selection format.

14. The circuit of Claim 12 wherein each delay circuit of said plurality of delay circuit delays said processed symbol by a delay duration twice the delay duration of the delay circuit coupled to the previous FHT engine.

15. The circuit of Claim 12 wherein each delay circuit of said plurality of delay circuit delays said processed symbol by a delay duration half the delay duration of the delay circuit coupled to the previous FHT engine.

16. The circuit of Claim 12 wherein said input symbol is provided serially and wherein each of said plurality of FHT engines comprises:

a difference circuit for receiving a delayed borrow signal, said delayed processed symbol, and said input symbol and subtracting said delayed borrow symbol and said input symbol from a bit of said delayed processed symbol to provide said difference symbol and a borrow symbol;

a first delay circuit for receiving said borrow symbol and delaying said borrow symbol according to a predetermined duration to provide said delayed borrow symbol;

a first multiplexer circuit for receiving said input symbol and said difference symbol and providing one of said input symbol and said

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difference symbol as said processed symbol according to a predetermined selection format;

a summing circuit for receiving ad summing said input symbol, said delayed processed symbol and a delayed carry symbol to provide said sum symbol and a carry symbol;

a second delay circuit for receiving said carry symbol and delaying said carry symbol by a predetermined duration to provide said delayed carry symbol; and

a second multiplexer circuit for receiving said delayed processed symbol and said sum symbol and providing one of said sum symbol and said delayed processed symbol as said input symbol for a subsequent stage.

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