METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES



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TECHNICAL FIELD OF THE INVENTION

The present invention relates to flash memory devices, and more particularly to NAND-type flash memory devices.

BACKGROUND OF THE INVENTION

Semiconductor flash memory devices include NAND-type flash memory devices. Such memory devices typically comprise a high density core region and a low density peripheral region on a single substrate. The memory cells within the core region are coupled together in a NAND-type circuit configuration, as illustrated in Figures 1A and 1B. Figure 1A illustrates a circuit schematic diagram of the core region 11 while Figure 1B illustrates a plan view of the core region 11. The core region 11 includes a memory cell region 22 which is bounded on one side by a drain select transistor portion 24 and bounded on another side by a source select transistor portion 26. Each of the select transistor portions 24 and 26 contain select gate transistors 24a-24c and 26a-26c, respectively, which operate to selectively activate a desired bit line.

Figure 1C illustrates a cross-section of conventional stack structures of a select transistor 100 and a memory cell 150 in the core region 11. The stack structure 150 of the memory cell includes a tunnel oxide 104 on a substrate 102 and a floating gate 106 composed of polysilicon on the tunnel oxide 104. The control gate comprises a polysilicon layer 110 and a tungsten silicide layer 112 on the polysilicon layer 110. A dielectric layer 108 insulates the floating gate 106 from the control gate 110 and 112. The control gate 110 and 112 is coupled to a word line. A cap layer 114 composed of silicon oxynitride resides on the control gate 110 and 112 and provides an anti-reflective coating at masking.

The stack structure 100 of the select transistor comprises a select gate oxide 116 on the substrate 102. A select gate 118 is on the select gate oxide 116. Like the memory cell stack structure 150, the control gate of the select transistor includes a polysilicon layer 122 and a tungsten silicide layer 124. A dielectric layer 120 insulates the select gate 118 from the control gate 122 and 124.



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The stack structure 100 is topped by a silicon oxynitride layer 126.

Typically, the floating gate 106 of the memory cell stack structure 150 and the select gate 118 of the select transistor stack structure 100 are formed from a single in-situ doped polysilicon layer. Subsequent masking and etching provides the resulting floating gate 106 and the select gate 118. In order to properly perform the programming and erasure of the memory cell, this single polysilicon layer must be conductive. It may be rendered conductive by using doped amorphous silicon for the single polysilicon layer. The dopant level of the single polysilicon layer is critical in the performance of the memory cell and thus the semiconductor device as a whole.

However, there are two conflicting factors in determining the level of dopant for the single polysilicon layer. If the dopant level is too low, this will cause the control gate contact resistance of the select transistor to become too high since the select gate 118 is connected to the control gate 122 and 124 via an interconnect (not shown). This causes the select transistor word line resistance to also become too high, resulting in a slower circuit performance. If the dopant level is too high, some of the dopant will contaminate the tunnel oxide 104 of the memory cell, which causes the surface of the floating gate 106 and tunnel oxide 104 interface to be rough. The rough interface leads to a high local electric field and a lower oxide dielectric strength. This causes reliability problems and a charge gain/loss problem in the programming and erasure of the memory cell.

EP-A-0,663,695 discloses a method of forming a NAND-type EEPROM in which a doped polysilicon layer is formed over a gate oxide layer, an ONO insulating layer is formed over the doped polysilicon layer, and a polysilicon film is deposited over the insulating layer to form a control gate layer, the doped polysilicon, the ONO layer and the control gate layer being etched to form gate portions of a memory cell and a select transistor. The polysilicon layer is doped with $5x10^{19} - 2x10^{20}$ of P or As.

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US-A-5,511,020 discloses a method of forming a pseudo-nonvolatile (PNUM) transistor in which a floating gate layer is deposited over a tunnelling oxide layer, the floating gate layer consisting of doped polysilicon or amorphous silicon deposited by CVD.

According to one aspect of the present invention there is provided a method for providing a NAND-type flash memory device, comprising:

(a) forming a select gate oxide layer in a select transistor area of a substrate and a tunnel oxide layer in a memory cell area of the substrate;

(b) forming a polysilicon layer on the select gate oxide layer and the tunnel oxide layer;

(c) forming an insulating layer on the polysilicon layer;

(d) forming a control gate layer on the insulating layer; and

(e) etching at least the doped polysilicon, the insulating layer, and the control gate layer to form at least one memory cell stack structure and at least one select transistor stack structure

characterised in that the gate oxide layer of the select transistor is thicker than the tunnel oxide layer of the memory cell, and the polysilicon layer consists of a doped amorphous silicon layer having a dopant level of between 5×10^{18} and 8×10^{19} ions/cm^3 of phosphorus.

With this dopant level, the contact resistance of the select transistor's control gate is low, thus keeping the word line resistivity of the device low. Simultaneously, contamination of the tunnel oxide of the flash memory cell by the dopant is limited, allowing for a smooth interface between the floating gate and the tunnel oxide, which prevents charge gain/loss problems. Thus, the reliability of the device is increased.

In the accompanying drawings, by way of example only:

FIGS. 1A-1B illustrate conventional memory cells within the core region in a NAND-type circuit configuration.

FIG. 1C illustrates a cross-section of conventional stack structures of a select transistor and a memory cell in the core region.

FIG. 2 is a flow chart illustrating a method of providing a NAND-type flash memory device in accordance with the present invention.

FIGS. 3A-3I illustrate cross-sections of a portion of a memory device core region along a bit line in demonstration of a preferred embodiment of the method for providing a NAND-type memory device in accordance with the present invention.

The present invention provides a method and NAND-type flash memory device for providing a polysilicon dopant level which avoids both the select transistor word line high resistance and the charge gain/loss problems. The

present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

The method in accordance with the present invention avoids the select transistor word line high resistance and the charge gain/loss problems by providing a polysilicon layer dopant level between approximately 5 x 10^{18} and 8 x 10^{19} ions/cm^3 of phosphorus. Preferably, the select transistor word line resistance is no greater than approximately 1500 ohm/sq. To more particularly describe the features of the present invention, please refer to Figures 2 through 3I in conjunction with the discussion below.

Figure 2 is a flow chart illustrating a method of providing a NAND-type flash memory device in accordance with the present invention. First, a select gate oxide layer in a select transistor area of a substrate and a tunnel oxide layer in a memory cell area of the substrate is formed, via step 202. Next, a doped amorphous silicon layer is formed on the select gate oxide layer and the tunnel oxide layer, via step 204. The doped amorphous silicon layer has a dopant level which simultaneously avoids the select transistor word line high resistance and the charge gain/loss problems. In the preferred embodiment, the dopant level is between 5 x 10^{18} and 8 x 10^{19} ions/cm^3 of phosphorus. Then, an insulating layer is formed on the doped amorphous silicon layer, via step 206, and a control gate layer is formed on the insulating layer, via step 208. To form the memory cell and select transistor stack structures, at least the doped amorphous silicon layer, the insulating layer, and the control gate layer is etched, via step 210.

With the method of providing a NAND-type flash memory device in accordance with the present invention, both the floating gate of the memory cell and the select gate of the select transistor are formed with the same doped amorphous silicon layer. With a dopant level between approximately 5 x 10^{18} and 8 x 10^{19} ions/cm^3 of phosphorus, the contact resistance of the select transistor's control gate is low, thus keeping the select transistor word line resistivity of the device low. Simultaneously, contamination of the tunnel oxide of the flash memory cell by the dopant is limited, allowing for the interface between the floating gate and the tunnel oxide to be smooth, which prevents charge gain/loss problems.

Although the present invention is described with the use of phosphorus ions, one of ordinary skill in the art will understand that other ions may be used, such as arsenic ions, without departing from the spirit and scope of the present invention.

Figures 3A-3I illustrate cross-sections of a portion of a memory device core region along a bit line in demonstration of a preferred embodiment of the method for providing a NAND-type memory device in accordance with the present invention. Although only cross-sections of a portion of the core region is illustrated, one of ordinary skill in the art will understand that a plurality of select transistors and memory cells may be fabricated in a similar manner.

Figures 3A-3D illustrate the formation of the select gate layer and the tunnel oxide layer, via step 202. First, as illustrated in Figure 3A, a first oxide layer 304 is grown on at least part of the substrate 302. The substrate 302 has a select transistor area and a memory cell area. Oxide grown in the select transistor area will eventually become the select gate oxide of the select transistor while oxide formed in the memory cell area will eventually become the tunnel oxide of the memory cell. In the preferred embodiment, approximately 148 Å of the first oxide layer 304 is grown on the substrate 302 using dry oxidation at about 900°C with an atmosphere of about 1.33 liters of O_2, 70 cc of HCl, and 12.6 liters of Ar.

Next, as illustrated in Figure 3B, a mask 306 is placed over a part of the first oxide layer 304. In the preferred embodiment, the mask 306 is placed over the first oxide layer in the select transistor area, leaving the first oxide layer in the memory cell area exposed. An etch is then performed, removing the unmasked portion of the first oxide layer 304. The mask 306 is then removed. As illustrated in Figure 3C, the result is the first oxide layer 308 in the select transistor area while the memory cell area has bare silicon substrate.

Next, a second oxide layer is grown on the first oxide layer 308 and the substrate 302, as illustrated in Figure 3D. In the preferred embodiment, dry oxidation techniques are used at about 1050°C with an atmosphere of about 1.33 liters of O_2, 70 cc of HCl, and 12.6 liters of Ar. The result is a combined oxide layer 310 which comprises a thin layer of oxide, the tunnel oxide layer, in the memory cell area of approximately 87Å, and a thicker layer of oxide, the select gate layer, in the

select transistor area of approximately 168Å.

Figure 3E illustrates the forming of a doped amorphous silicon layer, via step 204. In this step, a doped amorphous silicon layer 312 is deposited on the select oxide layer 310. In the preferred embodiment, approximately 700Å of the doped amorphous silicon layer 312 is deposited using low pressure chemical vapor deposition (LPCVD) techniques at about 450-580°C, preferably 530°C, and 300-550 mT, preferably 400mT, with about 1200-3000 sccm of SiH_4, preferably 2000 sccm, and 15-30 sccm of a mixture of 1% by weight of PH_3 in He, preferably 22 sccm. The amorphous silicon layer 312 is doped in-situ, i.e., doped during its formation, with a dopant level between 5×10^{18} and 8×10^{19} ions/cm^3 of phosphorus. The dopant level of the amorphous silicon layer 312 is a critical factor in the functioning of the device.

At this point, portions of the doped amorphous silicon layer 312 is etched away to define the floating gates of the memory cells. The etch is performed at about 125mT and 120W with about 30 sccm of Cl_2, and 70 sccm of HBr. The result is an isolation of portions of the doped amorphous silicon layer 312 along the bit line, defining floating gates for the memory cells along the bit lines. Figure 3F illustrates a cross-section along the word line illustrating the floating gates 324.

Figure 3G illustrates the formation of the insulating layer, via step 206, on the first doped amorphous silicon layer 312. In the preferred embodiment, the insulating layer 314 is a dielectric layer comprised of two oxide layers with a layer of nitride sandwiched in-between, called an ONO layer. Approximately 50Å of the first of the two oxide layers is first deposited on the doped amorphous silicon layer 312 at about 750°C and 600mT with about 20cc of SiH_4, and 1.2 liters of N_2O. Then approximately 80Å of the nitride layer is deposited at about 760°C and 330mT with about 600cc of NH_3, and 100cc of SiH_2Cl_2. The second of the two oxide layers of the dielectric layer 314 is formed using a nitride oxidation technique at about 950°C with about 5 liters of O_2, and 9 liters of H_2 for about 40 minutes, which grows approximately 50Å of oxide. The result is approximately 135Å of dielectric layer 314.

Figure 3H illustrates the formation of the control gate layer, via step 208. First, a polysilicon layer 316 is deposited on the dielectric layer 314. The polysilicon layer 316 may be comprised of

doped amorphous silicon. Then, a tungsten silicide layer 318 is deposited on the polysilicon layer 316, and a silicon oxynitride layer 320 is deposited on the tungsten silicide layer 318. In the preferred embodiment, approximately 1200Å of the polysilicon layer 316 is deposited. With a polysilicon layer comprised of doped amorphous silicon, the layer 316 is deposited using LPCVD techniques at about 530°C and 400mT with about 2000 sccm of SiH_4, and 75 sccm of a mixture of 1% by weight of PH_3 in He. Approximately 1500Å of the tungsten silicide layer 318 is deposited at about 360°C and 200mT with about 500 sccm of SiH_4, and 50 sccm of Ar. Approximately 1000Å of the silicon oxynitride layer 320 is deposited at about 400°C, 300-340W, and 3.5mT with about 90-110 sccm of SiH_4, 450-550 sccm of N_2, and 35-45 sccm of N_2O. A silicon oxynitride layer 320 with a reflectivity index between 2.0 and 2.34 is desirable. The silicon oxynitride layer 320 may also be bombarded with N_2O to promote the ease of removal of any subsequent photoresist during photolithography.

Then, a series of masking and etching steps are performed to form the stacked structures 300 and 350 of the select transistor and memory cell respectively, via step 210, illustrated in Figure 3I. The resulting memory cell stack structure 350 in accordance with the present invention comprises a tunnel oxide 322, formed from the oxide layer 310; a floating gate 324 with a dopant level between approximately 5×10^{18} and 8×10^{19} ions/cm^3 of phosphorus, formed from the doped amorphous silicon layer 312; an insulating layer 326; a polysilicon layer 328; a tungsten silicide layer 330; and a silicon oxynitride layer 332.

The resulting select transistor stack structure 350 in accordance with the present invention comprises a select gate oxide layer 334 formed from the oxide layer 310; a select gate 336 with a dopant level between approximately 5×10^{18} and 8×10^{19} ions/cm^3 of phosphorus, formed from the doped amorphous silicon layer 312; an insulating layer 338; a polysilicon layer 340; a tungsten silicide layer 342; and a silicon oxynitride layer 344.

Both the floating gate 324 and the select gate 336 are formed from the same doped amorphous silicon layer 312, which has a dopant level between approximately 5×10^{18} and 8×10^{19} ions/cm^3 of phosphorus. With this dopant level, both word line high resistance and charge gain/loss problems are avoided.

A NAND-type flash memory device and a method for providing such a device has been disclosed. A preferred embodiment of the polysilicon layer which forms both the floating gate of the flash memory cell and the select gate of the select transistor of the device is doped with between approximately 5×10^{18} and 8×10^{19} ions/cm^3 of phosphorus. With this dopant level, the contact resistance of the select transistor's control gate is low, thus keeping the word line resistivity of the device low. Simultaneously, contamination of the tunnel oxide of the flash memory cell by the dopant is limited, allowing for the interface between the floating gate and the tunnel oxide to be smooth, which prevents charge gain/loss problems. Thus, the reliability of the device is increased.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.

CLAIMS:

1. A method for providing a NAND-type flash memory device, comprising:

(a) forming a select gate oxide layer (334) in a select transistor area of a substrate and a tunnel oxide layer (322) in a memory cell area of the substrate;

(b) forming a polysilicon layer (312) on the select gate oxide layer and the tunnel oxide layer;

(c) forming an insulating layer (326, 338) on the polysilicon layer;

(d) forming a control gate layer (328, 330; 340, 342) on the insulating layer; and

(e) etching at least the doped polysilicon, the insulating layer, and the control gate layer to form at least one memory cell stack structure (350) and at least one select transistor stack structure (300);

characterised in that the gate oxide layer (334) of the select transistor is thicker than the tunnel oxide layer (322) of the memory cell, and the polysilicon layer (312) consists of a doped amorphous silicon layer having a dopant level of between 5×10^{18} and 8×10^{19} ions/cm^3 of phosphorus.

2. A method as claimed in claim 1, wherein the forming step (a) comprises:

(a1) growing a first oxide layer (304) in the select transistor area and the memory cell area;

(a2) removing the first oxide layer (304) in the memory cell area; and

(a3) growing a second oxide layer on the first oxide layer in the select transistor area and on the substrate in the memory cell area.

3. A method as claimed in claim 2, wherein the removing step (a2) comprises:

(a2i) placing a mask (306) on the first oxide layer (304) in the select transistor area;

(a2ii) etching the first oxide layer in the memory cell area; and

(a2iii) removing the mask.

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4. A method as claimed in any one of the preceding claims, wherein the doped amorphous silicon layer is formed using low pressure chemical vapor deposition techniques at about 450-580°C and 300-550mT with about 1200-3000 sccm of SiH_4 and 15-30 sccm of a mixture of 1% by weight of PH_3 in He.

5. A method as claimed in any one of the preceding claims, wherein the forming step (c) comprises:

(c1) depositing a first dielectric oxide layer on the doped amorphous silicon layer;

(c2) depositing a nitride layer on the first dielectric oxide layer; and

(c3) growing a second dielectric oxide layer on the nitride layer.

6. A method as claimed in any one of the preceding claims, wherein the forming step (d) comprises:

(d1) growing a second doped amorphous silicon layer (316) on the insulating layer (314); and

(d2) growing a tungsten silicide layer (318) on the second doped amorphous silicon layer.

7. A NAND-type flash memory device, comprising:

a substrate (302); at least one memory cell stack structure (350) on the substrate, comprising:

a tunnel oxide layer (322), a floating gate (324) on the tunnel oxide layer comprising doped amorphous silicon, the doped amorphous silicon having a dopant level of between 5×10^{18} and 8×10^{19} ions/cm^3 of phosphorus;

a first insulating layer (326) on the floating gate, and a first control gate layer (328, 330) on the first insulating layer;

and at least one select transistor stack structure (300) on the substrate (302), comprising:

a select gate oxide layer (334) on the substrate, the thickness of the select gate oxide layer (336) being greater than the thickness of the tunnel oxide layer (322);

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a select gate (336) on the select gate oxide layer comprising the doped amorphous silicon,

a second insulating layer (338) on the select gate, and

a second control gate layer (340, 342) on the second insulating layer.

8. A device as claimed in claim 7, wherein the doped amorphous silicon is formed using low chemical vapor deposition techniques at about 450-580°C and 300-550mT with about 1200-3000 sccm of SiH_4 and 15-30 sccm of a mixture of 1% by weight of PH_3 in He.

9. A device as claimed in claim 7 and claim 8, wherein the first insulating layer (326) comprises:

a first dielectric oxide layer on the floating gate;

a nitride layer on the first dielectric oxide layer; and

a second dielectric oxide layer on the nitride layer.

10. A device as claimed in any one of the claims 7-9, wherein the second insulating layer (338) comprises:

a first dielectric oxide layer on the select gate;

a nitride layer on the first dielectric oxide layer; and

a second dielectric oxide layer on the nitride layer.

11. A device as claimed in any one of the claims 7-10, wherein the first control gate layer comprises:

a polysilicon layer (328) on the first insulating layer (326); and

a tungsten silicide layer (330) on the polysilicon layer (328).

12. A device as claimed in any one of the claims 7-11, wherein the second control gate layer comprises:

a polysilicon layer (340) on the second insulating layer (338); and

a tungsten silicide layer (342) on the polysilicon layer (340).

13. A device as claimed in any one of the claims 7-12, wherein the at least one memory cell stack structure (350) further comprises:

a silicon oxynitride layer (332) on the first control gate layer.

14. A device as claimed in any one of the claims 7-13, wherein the at least one select transistor stack structure (300) further comprises:

a silicon oxynitride layer (344) on the second control gate layer.