ABSTRACT OF THE DISCLOSURE

A flexible, reconfigurable processing system architecture allows for the implementation of a variety of processing system configurations to be implemented on a single device, which is preferably a PCI bus add-in extension board (100) with an attached daughter card (D) attached and electrically connected thereto through a PCI Mezzanine type connector (36), and which is plugged into a personal computer PCI expansion slot. The architecture uses the PCI bus (26), for example, as the local CPU bus for an embedded processor, which not only allows for flexibility in system configuration but also allows PCI devices to be hidden from the host CPU to allow for proper system startup. The architecture further permits an embedded processing CPU (20) to be re-booted when the secondary PCI bus host bus bridge (25) fails to respond without affecting host CPU or other secondary PCI bus (27) peripheral devices. The architecture provides a method of loading an embedded system CPU's local memory with operating system and diagnostic code without the use of ROM or FLASH memory. A system and method of reserving memory is also disclosed which utilizes a dummy or surrogate board (210) with little of no functionality but which has a class code (208) of a common device such as an Ethernet card. The primary system BIOS will read the class code and reserve memory based on the surrogate card. The driver of the non-standard card such as an embedded processor, can then use the memory space allocated to the surrogate card (210) by the BIOS.



162162



G00002