

CLAIMS:

1. A semiconductor processing chamber comprising:
a gasbox;
a substrate support;
5 a blocker plate positioned between the gasbox and the substrate support,
wherein the blocker plate defines a plurality of apertures through the blocker plate; and
a faceplate positioned between the blocker plate and the substrate support,
wherein the faceplate is characterized by a first surface facing the blocker plate and a second
surface opposite the first surface, wherein the second surface of the faceplate and the
10 substrate support at least partially define a processing region within the semiconductor
processing chamber, wherein the faceplate is characterized by a central axis, wherein the
faceplate defines a plurality of apertures through the faceplate, wherein the faceplate defines
a plurality of recesses extending about and radially outward of the plurality of apertures, and
wherein each recess of the plurality of recesses extends from the second surface of the
15 faceplate to a depth less than a thickness of the faceplate.
2. The semiconductor processing chamber of claim 1, wherein the
faceplate is substantially planar across the first surface of the faceplate in an annular region
extending radially outward of the plurality of apertures.
3. The semiconductor processing chamber of claim 1, further comprising
20 an electrical source configured to strike a plasma within the processing region of the
semiconductor processing chamber.
4. The semiconductor processing chamber of claim 1, wherein each
aperture of the plurality of apertures comprises an aperture profile characterized by a first
section extending from the first surface of the faceplate partially through the faceplate, and
25 further characterized by a second section extending from a position partially through the
faceplate to the second surface of the faceplate.
5. The semiconductor processing chamber of claim 4, wherein the first
section is characterized by a substantially cylindrical profile.
6. The semiconductor processing chamber of claim 4, wherein the second
30 section comprises a conical or countersunk profile.

7. The semiconductor processing chamber of claim 6, wherein each recess of the plurality of recesses is characterized by a similar profile as the second section of the aperture profile of each aperture of the plurality of apertures.

8. The semiconductor processing chamber of claim 1, wherein each
5 recess of the plurality of recesses extends less than halfway through a thickness of the faceplate from the second surface of the faceplate.

9. A semiconductor processing chamber faceplate, comprising:
a first surface and a second surface opposite the first surface, wherein:
the faceplate is characterized by a central axis extending through the first
10 surface and the second surface,
the faceplate defines a plurality of apertures through the faceplate,
the faceplate defines a plurality of recesses extending about and radially
outward of the plurality of apertures, and
each recess of the plurality of recesses extends from the second surface of the
15 faceplate to a depth less than a thickness of the faceplate.

10. The semiconductor processing chamber faceplate of claim 9, wherein
the plurality of recesses are distributed as a set of rings extending outward from a central
axis, wherein a first subset of the set of rings is characterized by a number of apertures within
each corresponding ring according to the equation: XR , where X is a base number of
20 apertures, and R is the corresponding ring number, wherein a second subset of the set of rings
radially inward of the first subset of the set of rings is characterized by a number of apertures
within the ring according to the equation: $(XR) + N$, where N is an additional number of
apertures, and wherein a third subset of the set of rings radially outward of the first subset of
the set of rings is characterized by a number of apertures within the ring according to the
25 equation: $(XR) - N$, where N is an additional number of apertures.

11. The semiconductor processing chamber faceplate of claim 9, wherein
each aperture of the plurality of apertures extends from the first surface of the faceplate to the
second surface of the faceplate, and wherein a profile of each aperture includes a taper
extending from the second surface of the faceplate.

12. The semiconductor processing chamber faceplate of claim 11, wherein the taper extends to a depth partway through a depth of the faceplate, and wherein the profile of each aperture transitions to a choke from the taper.

13. The semiconductor processing chamber faceplate of claim 12, wherein
5 the profile of each aperture transitions from the choke to a substantially cylindrical profile extending to the first surface of the faceplate.

14. The semiconductor processing chamber faceplate of claim 12, wherein each recess of the plurality of recesses is characterized by a profile identical to the taper of the profile of each aperture of the plurality of apertures.

10 15. The semiconductor processing chamber faceplate of claim 14, wherein a profile for each recess of the plurality of recesses transitions to a substantially cylindrical profile extending to a location less than the thickness of the faceplate.

16. The semiconductor processing chamber faceplate of claim 15, wherein
15 each recess of the plurality of recesses is blocked from providing fluid access through the faceplate at the first surface of the faceplate.

17. The semiconductor processing chamber faceplate of claim 9, wherein each recess of the plurality of recesses extends less than halfway through a thickness of the faceplate from the second surface of the faceplate.

18. A method of semiconductor processing comprising:
20 flowing a precursor into a processing chamber, wherein the processing chamber comprises a faceplate and a substrate support on which a substrate is disposed, wherein a processing region of the processing chamber is at least partially defined between the faceplate and the substrate support, wherein the faceplate defines a plurality of apertures through which the precursor flows, wherein the faceplate defines a plurality of recesses
25 extending about and radially outward of the plurality of apertures, and wherein each recess of the plurality of recesses extends from a surface of the faceplate facing the substrate support to a depth less than a thickness of the faceplate;

generating a plasma of the precursor within the processing region of the processing chamber; and

depositing a material on the substrate.

19. The method of semiconductor processing of claim 18, wherein the material deposited is characterized by a thickness proximate an edge of the substrate less than 5% greater than a thickness proximate a center of the substrate.

5 20. The method of semiconductor processing of claim 18, wherein each recess of the plurality of recesses is characterized by a conical or countersunk profile.