NARROW-BODY DAMASCENE TRI-GATE FINFET HAVING THINNED BODY

TECHNICAL FIELD

The present invention relates generally to transistors and, more particularly, to fin field effect transistors (FinFETs).

BACKGROUND ART

The escalating demands for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

For example, when the gate length of conventional planar metal oxide semiconductor field effect transistors (MOSFETs) is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are, therefore, being explored to improve FET performance and allow further device scaling.

Double-gate MOSFETs represent structures that have been considered as candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, two gates may be used to control short channel effects. A FinFET is a recent double-gate structure that exhibits good short channel behavior. A FinFET includes a channel formed in a vertical fin. The FinFET structure may be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

DISCLOSURE OF THE INVENTION

Implementations consistent with the present invention provide a narrow-body tri-gate FinFET formed using, for example, a damascene process. A tri-gate FinFET will have better short-channel control than double-gate and single-gate devices, and will have higher drive current than a double-gate finFET for the same area. Local thinning of the fin channel minimizes source/drain series resistance while keeping the short-channel effect under control. The metal tri-gate, formed in a damascene process consistent with the invention, may be used to reduce gate resistance and eliminate poly depletion effects.

Additional advantages and other features of the invention will be set forth in part in the description which follows and, in part, will become apparent to those having ordinary skill in the art upon examination of the following, or may be learned from the practice of the invention. The advantages and features of the invention may be realized and obtained as particularly pointed out in the appended claims.

According to the present invention, the foregoing and other advantages are achieved in part by a method of forming a fin field effect transistor that includes forming a fin and forming a source region on a first end of the fin and a drain region on a second end of the fin. The method further includes forming a dummy gate, with a first crystalline material, in a first pattern over the fin and forming a dielectric layer around the dummy gate. The method also includes removing the first crystalline material to leave a trench in the dielectric layer corresponding to the first pattern, thinning a portion of the fin exposed within the trench, and forming a metal gate within the trench.

According to another aspect of the invention, a tri-gate fin field effect transistor is provided. The tri-gate fin field effect transistor includes a fin that further includes multiple surfaces and has a source region and a drain region formed adjacent each end of the fin. The tri-gate fin field effect transistor further includes a metal gate formed on three surfaces of the multiple surfaces, wherein the fin has been locally thinned prior to formation of the metal gate.

Other advantages and features of the present invention will become readily apparent to those skilled in this art from the following detailed description. The embodiments shown and described provide illustration of the best mode contemplated for carrying out the invention. The invention is capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference is made to the attached drawings, wherein elements having the same reference number designation may represent like elements throughout.

FIG. 1 illustrates exemplary layers of a silicon-on-insulator (SOI) wafer that may be used for forming a fin of a FinFET consistent with the present invention;

FIG. 2A illustrates an exemplary fin consistent with the invention;

FIGS. 2B and 2C illustrate source and drain regions formed adjacent the fin of FIG. 2A consistent with the invention;

FIG. 2D illustrates a cross-sectional view of the exemplary fin of FIG. 2A consistent with the invention;

FIG. 3A illustrates a cross-sectional view of a layer of sacrificial oxide formed on the fin of FIG. 2A consistent with the invention;

FIG. 3B illustrates a cross-sectional view of the removal of the sacrificial oxide of FIG. 3A consistent with the invention;

FIGS. 4A and 4B illustrate cross-sectional views of dummy oxide and a polysilicon layer formed on the fin of FIG. 3B consistent with the invention;

FIGS. 5A and 5B illustrate the formation of a dummy gate from the polysilicon layer of FIG. 4B consistent with the invention;

FIG. 6 illustrates the formation of a dielectric layer adjacent the dummy gate of FIGS. 5A and 5B consistent with the present invention; and

FIG. 7 illustrates the removal of the dummy gate of FIGS. 5A and 5B to form a gate trench consistent with the present invention;

FIG. 8 illustrates thinning of the fin exposed within the gate trench of FIG. 7 consistent with the present invention;

FIG. 9 illustrates formation of gate insulation within the gate trench of FIG. 7 consistent with the present invention;

FIGS. 10A, 10B and 10C illustrate formation of a metal tri-gate within the gate trench of FIG. 9 consistent with the present invention;

FIG. 11 illustrates formation of moly spacers adjacent a fin consistent with another embodiment of the invention; and

FIG. 12 illustrates nitrogen implantation within the moly spacers of FIG. 11 to form asymmetrically doped FinFET gates consistent with another embodiment of the invention.

BEST MODE FOR CARRYING OUT THE INVENTION

The following detailed description of the invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims.

Consistent with the present invention, an exemplary damascene process for forming a narrow-body tri-gate FinFET is provided. In the exemplary damascene process, a dummy gate may be formed from a layer of crystalline material, such as, for example, polysilicon, that has been formed over a fin. A dielectric layer may then be formed around the dummy gate and over the FinFET fin, source and drain regions. The dummy gate may then be removed to create a gate trench in the dielectric layer. The exposed portions of the FinFET fin within the gate trench may then be locally thinned to reduce source/drain series resistance. A metal gate that contacts three surfaces of the fin may then be formed in the created gate trench to complete the damascene process.

FIG. 1 illustrates a cross-section of a silicon on insulator (SOI) wafer 100 formed in accordance with an exemplary embodiment of the present invention. SOI wafer 100, consistent with the present invention, may include a buried oxide layer 110 formed on a substrate 115. A fin channel layer 105 may further be formed on buried oxide layer 110. The thickness of fin channel layer 105 may range, for example, from about 500Å to about 2000Å and the thickness of buried oxide layer 110 may range, for example, from about 1000Å to about 3000Å. Fin channel layer 105 and substate 115 may include, for example, silicon, though other semi-conducting materials, such as germanium, may be used.

As shown in FIGS. 2A through 2D, a vertical fin 205 may be formed from fin channel layer 105. Fin 205 may be formed, for example, with a width (w) in a range of 10-100 nm. Fin 205 may be formed from fin layer 105 using any conventional process, including, but not limited to, existing photolithographic and etching processes.

Subsequent to formation of fin 205, source 210 and drain 215 regions may be formed adjacent respective ends of fin 205, as shown in FIGS. 2B and 2C. Source 210 and drain 215 regions may be formed by, for example, deposition of a layer of semi-conducting material over fin 205. The source 210 and drain 215 regions may be formed from the layer of semi-conducting material using, for example, conventional photolithographic and etching processes. One skilled in the art will recognize, however, that other existing techniques may be used for forming source 210 and drain 215 regions. For example, source 210 and drain 215 regions may be formed by patterning and etching fin layer 105. Source 210 and drain 215 regions may include a material such as, for example, silicon, germanium, or silicon-germanium (Si-Ge). In one implementation, $Si_xGe_{(1-x)}$, with x approximately equal to 0.7 may be used. A cap 220 may then be formed on upper surfaces of fin 205, source 210 and drain 215, as illustrated in FIG. 2D. Cap 220 may include an oxide,

such as, for example, silicon oxide, and may range, for example, from about 150 Å to about 700 Å in thickness.

As shown in FIG. 3A, after formation of source 210 and drain 215 regions, a sacrificial oxide layer 305 may be formed on fin 205 and source 210 (not shown) and drain 215 (not shown). Sacrificial oxide layer 305 may be formed on fin 205, source 210 and drain 215 using any conventional process. In some exemplary embodiments, for example, sacrificial oxide layer 305 may be thermally grown on fin 205, source 210 and drain 215. As shown in FIG. 3B, cap 220 and sacrificial oxide layer 305 may be removed using a conventional process, such as, for example, a conventional etching process to remove defects from sidewalls of fin 205.

Dummy oxide 405 may be formed on fin 205, source 210 and drain 215 using a conventional process, as shown in FIG. 4A. Dummy oxide 405, for example, may be thermally grown on fin 205, source 210 and drain 215. Dummy oxide 405 may include an oxide, such as, for example, silicon oxide and may range, for example, from about 50 Å to about 150 Å in thickness. As further shown in FIG. 4B, a layer of polysilicon 410 may be formed over fin 205, source 210 and drain 215. The thickness of polysilicon layer 410 may range, for example, from about 700 Å to about 2000 Å. Polysilicon layer 410 may be polished back using, for example, a chemical-mechanical polishing (CMP) process, to achieve a planar surface to improve subsequent gate lithography. As shown in FIGS. 5A and 5B, a dummy gate 505 may be defined in polysilicon layer 410 using a conventional process, such as, for example, a conventional patterning and etching process.

As shown in FIG. 6, a dielectric layer 605 may be formed over dummy gate 505 using, for example, conventional deposition techniques. Dielectric layer 605 may include, for example, tetraethylorthosilicate (TEOS), or any other dielectric material. The thickness of dielectric layer 605 may range, for example, from about 1000 Å to about 2500 Å. Dielectric layer 605 may then be polished back to expose the upper surface of dummy gate 505 using, for example, a CMP process, as illustrated in FIG. 6.

Dummy gate 505 and dummy oxide 405 may then be removed, as shown in FIG. 7, leaving a gate trench 705. Dummy gate 505 and dummy oxide 405 may be removed using, for example, conventional etching processes. As shown in FIG. 8, a portion of the fin channel exposed within gate trench 705 may be thinned to produce a locally thinned fin region 805. The portion of the fin channel exposed within gate trench 705 may be thinned, for example, via selective etching of the fin channel. Gate insulation 910 may then be formed in gate trench 705, as shown in FIG. 9. Gate insulation 910 may be thermally grown or deposited using conventional processes. Gate insulation 910 may include SiO, SiO_2, SiN, SiON, HFO_2, ZrO_2, Al_2O_3, HFSiO(x) ZnS, MgF_2, or other high-K dielectric materials.

As shown in FIGS. 10A, 10B and 10C, a metal gate 1005 may be formed in gate trench 705 over gate insulation 910. Metal gate 1005 may be formed in gate trench 705 using a conventional metal deposition process and polished back to the upper surface of dielectric layer 605. Metal gate 1005 may include a metal material, such as, for example, TaN or TiN, though other metals may be used. As shown in FIG. 10C, the resulting metal gate 1005 is disposed on three sides of fin 205, thus, producing a tri-gate FinFET. The tri-gate FinFET, consistent with the invention, will have better short-channel control than double-gate and single-gate devices. The tri-gate FinFET will have higher drive current than a double-gate FinFET for the same area. The metal gate 905 of the tri-gate FinFET further also reduces poly depletion effects and gate resistance.

EXEMPLARY DIFFERENTIALLY DOPED
MOLYBDENUM FINFET GATES

FIGS. 11-12 illustrate an exemplary process for forming asymmetric molybdenum FinFET gates. As shown in FIG. 11, the exemplary process may begin with the deposition of molybdenum on a fin 1105 to produce molybdenum spacers 1110 and 1115. Fin 1105 may be formed in accordance with the exemplary process described above with respect to FIGS. 1 and 2. The molybdenum spacers 1110 and 1115 may range, for example, from about 200 Å to about 1500 Å in thickness.

Subsequent to deposition of the molybdenum, spacers 1110 and 1115 may be asymmetrically doped via implantation of different concentrations of nitrogen. Implantation of nitrogen in each of the spacers 1110 and 1115 alters the work function associated with each spacer. The asymmetric doping of spacers 1110 and 1115 results in dual work functions thus, producing asymmetric gates for the resulting FinFET.

In the previous descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the details specifically set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention. In practicing the present invention, conventional photolithographic and etching techniques may be employed, and hence, the details of such techniques have not been set forth herein in detail.

Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein.

CLAIMS

1. A method of forming a fin field effect transistor, characterized by:

forming a fin (205);

forming a source region (220) on a first end of the fin (205) and a drain region (215) on a second end of the fin (205);

forming an oxide cap (210) over upper surfaces of the fin (205), source region (210), and drain region (215);

forming a layer (305) of sacrificial oxide on the fin (205), source region (210) and drain region (215) after formation of the oxide cap (220);

removing the layer (305) of sacrificial oxide to remove defects from surfaces of the fin (205);

forming a dummy gate (505), with a first semi-conducting material, in a first pattern over the fin (205);

forming a dielectric layer (605) around the dummy gate (505);

removing the first semi-conducting material to leave a trench (705) in the dielectric layer (605) corresponding to the first pattern;

thinning a portion of the fin (205) exposed within the trench (705);

forming a layer (910) of gate insulation on the surfaces of the fin (205) exposed within the trench (705); and

forming a metal gate (1005) within the trench (705) over the layer (910) of gate insulation.

2. The method of claim 1, wherein the metal gate (1005) contacts at least three of the surfaces of the fin (205) and wherein the fin field effect transistor comprises a tri-gate fin field effect transistor.

3. The method of claim 1, wherein the dielectric layer (605) comprises tetraethylorthosilicate and wherein the first semi-conducting material comprises polysilicon.

AMENDED SHEET

4. The method of claim 1, wherein the gate insulation (910) comprises at least one of SiO, SiO_2, SiN, SiON, HFO_2, ZrO_2, Al_2O_2, $HFSiO_{(x)}$, ZnS, and MgF_2.

5. The method of claim 1, further comprising:

forming a layer of dummy oxide (405) over the fin (205) prior to forming the dummy gate (505),

wherein forming the dummy gate (505) comprises:

depositing a layer of the first semi-conducting material over the fin (205); and

etching the layer of the first semi-conducting material to form the dummy gate (505) in the first pattern,

6. The method of claim 1, wherein forming the metal gate (1005) comprises:

depositing a metal material within the trench (705).

7. The method of claim 1, wherein forming the layer (305) of sacrificial oxide comprises:

thermally growing the layer (305) of sacrificial oxide, and

wherein removing the layer (305) of sacrificial oxide to remove defects from sidewalls of the fin (205) comprises:

etching the layer (305) of sacrificial oxide.

AMENDED SHEET