PHOTORESIST STRIPPING CHAMBER AND METHODS OF ETCHING PHOTORESIST ON SUBSTRATES

BACKGROUND

[0001] Plasma processing apparatuses are used for processes including plasma etching, physical vapor deposition, chemical vapor deposition (CVD), ion implantation, and resist removal.

[0002] Photoresist materials are used in plasma processing operations to pattern materials. Commercial photoresists are blends of polymeric and other organic and inorganic materials. A photoresist is applied onto a substrate, and radiation is passed through a patterned mask to transfer the pattern into the resist layer. The two broad classifications of photoresist are negative-working resist and positive-working resist, which produce negative and positive images, respectively. After being developed, a pattern exists in the photoresist. The patterned photoresist can be used to define features in substrates by etching, as well as to deposit materials onto, or implant materials into, substrates. Commonly-assigned U.S. Patent Nos. 5,968,374, 6,362,110 and 6,692,649, the disclosures of which are hereby incorporated by reference, disclose plasma photoresist stripping techniques.

SUMMARY

[0003] A method of protecting an active area on a substrate, comprises positioning a substrate in an inductively coupled plasma processing chamber of a plasma reactor, the plasma reactor including a dielectric window overlying the substrate and at least one coil which inductively couples RF energy through the dielectric window and into a space between the dielectric window and the substrate, the substrate including an active area, supplying a process gas to the plasma processing chamber, generating a plasma from the process gas by supplying power to the coil, processing the substrate with the plasma so as to protect the active area by (a) maintaining a plasma potential of 5 to 15 volts at the substrate and/or (b) passivating the active area by using a silane-free process gas comprising at least one additive effective to form a protective layer on an active area of the substrate

wherein the protective layer includes at least one element from the additive which is already present in the active area and stripping the organic photoresist in a second step.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1A illustrates a process of removing an ion-implanted photoresist over an active area (AA) on a semiconductor wafer and FIG. 1B illustrates an inductively coupled plasma chamber which can be used to carry out the photoresist stripping process illustrated in FIG 1A.

[0005] FIG. 2 is a graphical simulation of ion penetrations into silicon oxide (SiOx) and silicon (Si).

[0006] FIG. 3 is a graphical representation of material loss as a function of direct current (DC) bias voltage at a bottom electrode used to support a semiconductor wafer.

[0007] FIG. 4 is a graphical representation of material loss as a function of chamber pressure.

[0008] FIG. 5 is a graphical representation of silicon loss as a function of TCP power for four process gas chemistries.

[0009] FIG. 6 is a graphical representation of photoresist strip rate as a function of TCP power for four process gas chemistries.

[0010] FIG. 7 is a graphical representation of silicon loss for five gas chemistries with 0 to 100 sccm Xe and 350 sccm O_2.

[0011] FIG. 8 is a graphical representation of silicon loss for four gas chemistries wherein the side-by-side bars represent 6Å and 12 Å native oxide, respectively.

[0012] FIG. 9 is a scanning electron micrograph (SEM) of an undesired residue resulting from use of process gas of 30 sccm CHF_3 and 350 sccm O_2 for 100 seconds followed by deionized water (DI) rinse.

[0013] FIG. 10 is a scanning electron micrograph (SEM) of an undesired residue on a substrate resulting from use of process gas of 30 sccm CF_4 and 350 sccm O_2 for 100 seconds followed by deionized water (DI) rinse.

[0014] FIG. 11 is a scanning electron micrograph (SEM) of a residue-free substrate resulting from use of process gas of 30 sccm CF_4 and 350 sccm O_2 for 10 seconds followed, process gas of 10 sccm CH_3F and 350 sccm O_2 for 100 seconds by deionized water (DI) rinse.

[0015] FIG. 12 is a scanning electron micrograph (SEM) of residue-free resulting from use of process gas of 10 sccm SiF_4 and 350 sccm O_2 for 2 seconds followed, process gas of 10 sccm CH_3F and 350 sccm O_2 for 90 seconds by deionized water (DI) rinse.

[0016] FIGS. 13A and B show SIM and SEM results for a 100Å oxide wafer which has not been processed.

[0017] FIGS. 13C and D show SIM and SEM results for a 100Å oxide wafer processed at a chamber pressure of 90 mTorr, 1.2 kW TCP power, 0 volts bias on the bottom electrode, 350 sccm O_2 and 10 sccm CHF_3 for 60 seconds.

[0018] FIG. 14 illustrates the effects of using a pulsed plasma on silicon loss.

[0019] FIG. 15 illustrates influence of SiF_4 flow rate on silicon loss and oxide thickness, FIG. 16 illustrates influence of chamber pressure at two SiF_4 flow rates and FIG. 17 illustrates influence of spacing between coil and wafer on silicon loss.

DETAILED DESCRIPTION

[0020] In integrated circuit (IC) manufacturing processes that utilize ion implantation, shrinking device geometries, increased ion implantation energies and doses, and new materials make it increasingly difficult to produce residue-free devices. Residues remaining from etching and ashing processes can produce undesirable electrical effects and corrosion that reduce product yields. *See* E. Pavel, "Combining Microwave Downstream and RF Plasma Technology for Etch and Clean Applications," 196th Meeting of the Electrochemical Society, (October, 1999).

[0021] In plasma processing techniques, such as plasma etching and reactive ion etching (RIE), and in ion implantation, photoresist is applied onto a substrate to protect selected regions of the substrate from being exposed to ions and

free radicals. Organic polymer compositions have been formulated for such resist applications.

[0022] Photoresists are removed, or "stripped," from the underlying substrate after the substrate has been processed by etching, ion implantation, or the like. It is desirable that the photoresist stripping process leave the substrate surface as clean as possible, desirably without any residual polymer film or resist material. Wet and dry stripping techniques can be used to remove photoresist. Wet stripping techniques use solutions containing organic solvents or acids. Dry stripping (or "ashing") techniques use an oxygen plasma for photoresist removal.

[0023] Ion implantation fabrication techniques are used to dope regions of a substrate with impurities to change the electrical properties of the substrate. Ion implantation can be used as a source of doping atoms, or to introduce regions of different composition in a substrate. During ion implantation, ions are accelerated at a sufficiently high voltage to penetrate the substrate surface to a desired depth. Increasing the accelerating voltage increases the depth of the concentration peak of the impurities.

[0024] Regions of the substrate at which implantation is not desired are protected with photoresist. However, the photoresist is modified during implantation, and is rendered more difficult to remove after implantation than a normal (non-implanted) photoresist. Particularly, implanted ions damage regions of the photoresist, thereby breaking near-surface C-H bonds and forming carbon-carbon single and double bonds. The resulting tough, carbon-rich or "carbonized" layer (or "skin" or "crust") of cross-linked, implanted photoresist encapsulates the distinct underlying bulk photoresist. The thickness of the carbon-rich layer is a function of the implant species, voltage, dose and current. The carbon-rich layer typically has a thickness of from about 200 Δ to about 2000 Δ. *See*, A. Kirkpatrick et al., "Eliminating heavily implanted resist in sub-0.25-Φm devices," *MICRO*, 71 (July/August 1998). According to E. Pavel, as implant doses and energies increase, implanted photoresist can become increasingly more difficult to remove.

[0025] Carbon-rich layers can also be formed in organic photoresist during plasma processing techniques, other than ion-implantation techniques, in which ion bombardment of the photoresist also occurs.

[0026] Oxygen plasma ashing techniques can remove the carbon-rich layer, but only at a slow rate of about 500 Δ/min or less. The etching mechanism of these techniques is the reaction of oxygen radicals with hydrocarbons in the photoresist to produce H_2O and CO_2.

[0027] It has been determined that an RF bias can be applied to the substrate to enhance the removal rate of the cross-linked layer. The applied RF bias provides energy to the carbon-rich layer, which breaks carbon single bonds and thereby enhances reactions with oxygen radicals.

[0028] However, it has also been determined that applying an RF bias to the substrate to enhance photoresist removal can also produce undesired effects. FIG. 1A schematically depicts a process of removing organic photoresist from an ion-implanted substrate 10. The substrate 10 includes silicon 11 that is ion implanted to form active areas 11a and a thin overlying inorganic layer 12 (*e.g.*, a silicon-containing layer, such as SiO_x). The inorganic layer 12 may be a silicon oxide layer that is formed by CVD or ion immersion, thermally grown, or may be a native oxide, and typically has a thickness of less than or equal to 20 Δ or a thickness of 20 to 40Å. A photoresist 16 applied over the inorganic layer 12 includes bulk photoresist 18, and an overlying carbon-rich layer 20 formed by the ion-implantation process. The features (contacts, vias, trenches, etc.) defined by the photoresist 16 are typically about 0.25 Φm or less in width on the substrate 10. In an RF biased system, energetic O_2^+ ions can cause sputtering of the inorganic layer 12. Sputtering of the inorganic layer 12 is undesirable because for typical process specifications the maximum amount of inorganic material (*e.g.*, oxide) loss during the removal of the carbon-rich layer 20 and the bulk photoresist 18 is less than about 2 Δ. The carbon-rich layer 20 can typically have a thickness of from about 200 to about 2000 Δ, and the bulk photoresist 18 can typically have a thickness of about several thousand angstroms. In addition, sputtered inorganic

material can re-deposit on the substrate and on the photoresist, resulting in organic and inorganic residue being present on the substrate after cleaning.

[0029] Another undesirable effect of applying a bias voltage to the substrate during processing such as photoresist removal is that oxygen ions of the plasma may have sufficiently high energy to penetrate the thin inorganic layer and oxidize the underlying silicon within the active area. The active area includes implanted silicon, strained silicon and/or a gate oxide on a semiconductor substrate of silicon, gallium arsenide or the like.

[0030] In light of the above-described findings, it has been determined that undesired silicon loss and/or growth of a silicon oxide layer can be achieved by processing the substrate while maintaining a plasma potential at the substrate surface of about 5 to 15 volts and/or passivating the active area using a silane-free process gas comprising at least one additive to form a protective layer on the active area optionally followed by crust and photoresist removal. During the first step, it is desirable to protect the active area from silicon loss due to impingement with oxygen ions and/or minimize growth of the gate oxide due to buildup of $SiO_xF_yC_z$ where x can be 0 to 2, y can be 0 to 2 and z can be 0 to 1. Accordingly, in the first step, the silicon loss can be minimized by forming a protective layer on the active area and/or plasma potential at the substrate (wafer) can be reduced to a desired value (e.g., below 20 volts, preferably 5 to 15 volts) by various chamber design and/or process modifications. For example, the outermost periphery of the one or more induction coils overlying the dielectric window can be spaced inwardly of the chamber wall surrounding the substrate support (e.g., provide a spacing of at least 5 cm between outer turn of the coil and inner wall of chamber), the dielectric window can have an increased thickness (e.g., provide a window at least 4 cm thick), the distance between the substrate and the coil can be increased (e.g., lower the substrate support and/or add a spacer between the dielectric window and the top of the chamber to move the coil further from the substrate) such that the inductively coupled plasma chamber can be operated without use of a Faraday Shield. Another way to reduce plasma potential is by pulsing RF power

applied to the induction coil during the first step, increasing impedance of ground path seen by the substrate and/or including high atomic number neutral gas species in the process gas (e.g., Ne, Kr, Xe). Passivation can be achieved by including an additive which forms a protective layer over the active area wherein the protective layer includes at least one element already present in the active area (e.g., Si, Ge, As, Sb, In, P or B through addition of a silane-free gas such as SiF_4, GeF_4, GeH_4, AsH_3, PH_3, B_2, H_6). If desired, other gases such as N_2O, NH_3, CF_4, CO, or the like can be added in the first step.

[0031] In step 2, during which the crust and/or bulk photoresist is stripped, the process gases may include various constituents including an oxygen-containing gas, one or more hydrocarbon, fluorocarbon and fluorohydrocarbon gases, and the additive used in the first step. The inorganic material can be, for example, a silicon-containing material (*e.g.*, Si, SiO_x [*e.g.* SiO_2], Si_xN_y [*e.g.*, Si_3N_4], $Si_xO_yN_z$, high-k metal oxide gates (e.g., $HfSi_xO_y$) and the like). The photoresist can be present on various semiconductor substrate materials such as wafers including, *e.g.*, silicon, SiO_2, Si_3N_4, and the like.

[0032] The plasma is preferably generated from the process gas by applying radio frequency (RF) to one or more electrically conductive coils outside of the plasma processing chamber. The substrate is preferably a wafer placed in the vicinity of the plasma generation region. In a preferred embodiment, the coil is a planar coil and the exposed surface of the wafer faces and is parallel to the plane of the coil.

[0033] The plasma reactor is preferably an inductively coupled plasma reactor, more preferably a high density TCP™reactor available from Lam Research Corporation, the assignee of the present application. Embodiments of the methods of removing photoresist from substrates, such as 300 mm and 200 mm substrates, can be performed in an inductively-coupled plasma reactor, such as the reactor 100 shown in FIG. 1B. The reactor 100 includes an interior 102 maintained at a desired vacuum pressure by a vacuum pump connected to an outlet 104. Process gas can be supplied to a showerhead arrangement by supplying gas from a gas

supply 106 to a plenum 108 extending around the underside of a dielectric window 110. A high density plasma can be generated in the interior 102 by supplying RF energy from an RF source 112 to an external RF antenna 114, such as a planar spiral coil having one or more turns disposed outside the dielectric window 110 on top of the reactor 100.

[0034] A substrate 116, such as a semiconductor wafer, is supported within the interior 102 of the reactor 100 on a substrate support 118. The substrate support 118 can include a chucking apparatus, such as an electrostatic chuck 120, and the substrate 116 can be surrounded by a dielectric focus ring 122. The chuck 120 can include an RF biasing electrode for applying an RF bias to the substrate during plasma processing of the substrate 116. The process gas supplied by the gas supply 106 can flow through channels between the dielectric window 110 and an underlying gas distribution plate 124 and enter the interior 102 through gas outlets in the plate 124. Alternatively, the gas can be supplied by one or more gas injectors extending through the window. See, for example, commonly-assigned U.S. Patent No. 6,230,651. The reactor can also include a liner 126 extending from the plate 124.

[0035] An exemplary plasma reactor that can be used for generating plasma is the 2300 TCP™ reactor available from Lam Research Corporation. Typical operation conditions for the plasma reactor are as follows: from about 400 to about 10,000 watts inductive power applied to upper electrode (coil), reaction chamber pressure of from about 10 to about 500 mTorr, and a total process gas flow rate of from about 200 to about 600 sccm during the passivation and photoresist removal steps.

[0036] During the passivation and photoresist removal steps, the substrate is preferably maintained at a sufficiently low temperature on a substrate support (e.g., ESC) to prevent rupturing of the carbon-rich layer. For example, a carbon-rich layer may rupture when solvents in the photoresist composition are volatilized by heating, producing particles that may deposit on the substrate. To avoid such rupturing of the carbon-rich layer, the substrate support is preferably maintained at a temperature of less than about 150°C, and more preferably from about -20 to about

75°C, and a chamber pressure of less than about 200 mTorr during passivation and removal of the photoresist.

[0037] During the passivation and photoresist removal steps, an RF bias is preferably not applied to the substrate with the bottom electrode on which the substrate is supported. Instead, the impedance path to ground seen by the substrate is preferably increased to reduce plasma potential seen at the substrate surface. Alternatively, an RF bias can be applied during the photoresist removal step during which the RF bias can accelerate ions in the plasma and add energy to the substrate, which increases the removal rate of the photoresist. The RF bias voltage applied to the substrate is preferably less than about 100 volts (with respect to ground), more preferably less than about 20 volts.

[0038] Although the chamber can be designed to provide reduced plasma potential at the substrate surface, adjustments to the plasma potential can be made by various techniques. For instance, power to the coil and/or pressure in the chamber can be adjusted to achieve a desired plasma potential. Also, gases such as Xe and Kr can be added to the process gas to lower the plasma potential and gases such as He can be added to the process gas to raise the plasma potential during the passivation and/or photoresist removal steps.

[0039] The second step can be tailored to remove the entire photoresist or the second step can include a crust break through stage followed by a photoresist strip stage. If desired, the complete removal of the carbon-rich layer can be detected during the etching process by using an endpoint detection technique, which can determine the time at which the underlying bulk photoresist is exposed. For example, the endpoint for carbon-rich layer removal can be determined by an optical emission technique (e.g., the optical emission technique can monitor the emission from carbon monoxide (CO) at a wavelength such as about 520 nm.) During the removal of the carbon-rich layer, a small CO signal is produced due to the low etch rate. Once the carbon-rich layer is opened, the exposed underlying bulk photoresist is etched at a faster rate than the carbon-rich layer and, consequently, the CO concentration and the corresponding CO signal increase.

[0040] After removal of the carbon-rich layer, the underlying bulk photoresist can be removed using a different photoresist etch process. For example, the bulk photoresist can be removed by oxygen ashing at a higher temperature than the temperature preferably used during the carbon-rich layer etching step. For example, the substrate temperature can range from about 150°C to about 300°C, preferably 200 to 280°C, during the bulk photoresist etching step. The chamber pressure is preferably greater than about 500 mTorr during bulk photoresist removal. Oxygen ashing also can achieve a high removal rate of the bulk photoresist. For example, an O_2/N_2 plasma can remove the bulk photoresist at a rate of from about 4 to about 6 microns/min. An optional over-ash step can also be used. Volatile solvents in the photoresist can be exhausted from the plasma processing chamber as the photoresist is ashed.

[0041] The bulk photoresist is preferably removed in the same chamber or a different chamber using a plasma generated upstream from the substrate. However, the bulk photoresist removal step can be performed in the same processing chamber that is used for the passivation and crust removal steps. Alternatively, the bulk photoresist can be removed in a different processing chamber. That is, the substrate can be removed from the processing chamber after the passivation and crust removal steps, and placed in a different processing chamber to etch the bulk photoresist. Using different processing chambers can obviate changing gas chemistries and/or the substrate temperature during removal of the carbon-rich layer and ashing, respectively.

[0042] Exemplary process conditions for passivation and/or photoresist removal on a 300 mm wafer are as follows: chamber pressure of about 10-500 mTorr, preferably 50 to 90 mTorr, power applied to upper electrode (coil) of about 400-10,000 Watts, preferably 400 to 3500 Watts of pulsed time averaged power during the passivation step, power applied to bias electrode of about 0-10 Watts, preferably 0 Watts during the passivation step, gas flow rates of about 1 to 20 sccm for the additive-containing gas (e.g., 1 to 20 sccm SiF_4), about 200 to 500 sccm for the oxygen-containing gas, 10 to 50 sccm fluorocarbon and/or fluorohydrocarbon gas (e.g., CF_4), 100 to 800 sccm inert or high atomic number gas (e.g., Ar, Ne, Kr,

Xe) and substrate support temperature of below 75°C, preferably from -20°C to about 20°C.

[0043] If the entire photoresist is not removed in the second step, it is desirable that any residue is soluble in deionized water, thereby minimizing the need for wet stripping techniques. Process parameters such as the flow rates of the process gases and their pressures may be adjusted to achieve selective etching of the carbon-rich layer relative to the inorganic layer and the bulk photoresist can be removed using the same or different process gas.

[0044] In the case where the entire photoresist is not removed during the second step, exemplary process conditions for removing the remaining bulk photoresist in a downstream plasma strip chamber are as follows: chamber pressure of about 1000 mTorr, about 2500 Watts of power applied to the plasma source, total process gas flow rate of about 4400 sccm, and substrate temperature of about 220°C.

[0045] As device geometries shrink to 65nm and below, certain difficulties with material loss are encountered in front end of line (FEOL) processing, such as in etch and post implant strip and clean. The active areas of substrates are subjected to various levels of implants, followed by strip and post strip cleans. The dry or wet effects on active area can be detrimental from a material or dopant loss prospective. Material loss can occur as the active area is subjected to repetitive strip and cleans or etch processes. As material loss increases various device characteristics change, including drive current, leakage, resistivity and short channel effects. Device sensitivity to material loss increases even further as device geometries decrease beyond 65nm. Active area characteristics are a precision-engineered part of the any device for optimum performance, and therefore, material loss due to FEOL processing - such as post implant strip, is detrimental to device performance.

[0046] In FEOL post implant strip processing, the concern is to remove a hardened photoresist (PR) layer, followed by the remaining bulk PR, without adversely affecting (or removing) any exposed dielectric layer over the underlying

active area silicon, which may or may not include N or P dopants and/or Ge . In addition to stringent material loss goals, it is required that the strip process not result in a residue layer that is hard to remove in post implant strip wet cleans. It is desired that any residue after dry strip be water soluble, and or easily removable by conventional techniques such as SPM and/or APM.

[0047] Material loss during dry strip occurs due to charged chemical species from the plasma penetrating through the thin dielectric layer into the active area, and reacting with the Si, Ge, or dopants. An example for such a reaction is oxidizing radicals that are driven through the thin dielectric layer by sufficient energy to react and oxidize active area constituents. Results of such an action lead to active area Si or Ge loss. Reducing species (i.e. Hydrogen) can also be disruptive to active area region. The effects of active area damage in dry strip can be realized further by excessive material loss during post strip chemical cleans. It is postulated that penetrating ions from the plasma during dry strip are disruptive enough to the active area surface, bulk, lattice or periodicity causing this area to become ostensibly more susceptible to wet chemical attacks, thus resulting in excessive material loss. To summarize, the extent of active area material loss is not just realized during dry strip, but also during subsequent wet cleans, if the effects of ion energies are not properly controlled or reduced.

[0048] In one embodiment, post implant strip is carried out in a plasma reactor modified to reduce the plasma potential (or ion energy). Such changes include, but are not limited to: 1) use of pulsed power plasma generator for plasma source, 2) use of high powered inductive plasma source and/or high chamber pressure, 3) optimize reactor geometry to reduce ion energies at the wafer level and/or 4) use of high impedance path to ground bottom electrode to support the substrate. The forgoing can be used with or without 5) process window changes targeting lower ion-energy regions and/or 6) forming a protective film over the active area prior to, or during any sequence of steps for crust or PR removal.

[0049] Crust and bulk PR strip process window changes involve development and characterization of a strip process where ion energies are lowered significantly to a few volts, to be much less disruptive to active area integrity. These

process changes involve the use of higher plasma powers (1200 – 10,000W) and higher range of strip pressures (10 – 500mT) in various sequences for crust and bulk removal to achieve the desired results. These process changes can be coupled with the use of process gas constituents to produce a protective layer to the active area to preserve it significantly during crust and bulk PR removal. The protective layer constituents can include Si, Ge, C, O, H, B, P, As, Sb, F, N and compounds thereof. Process gas constituents used to form this protective layer preferably produce the most effective results in preserving the active area region. These can be non-silane silicon containing gases such as SiF_4, germanium containing gases such as GeF_4 and GeH_4, nitrogen containing gases such as N_2O and NH_3, carbon containing gases such as CF_4 and CO, boron containing gases such as B_2H_6, phosphorous containing gases such as PH_3, arsenic containing gases such as AsH_3, etc. to limit or eliminate disruption to active area during dry plasma strip. While not wishing to be bound by theory, it is believed that the protective layer lowers active area material loss in a bi-functional way; one by being physically protective over the active area, and the other by being sacrificial or reactive with the plasma. The physically protective aspects of the protective layer from charged species during dry plasma strip provides a shield or buffer to the active area from ions. The sacrificial or reactive nature of the protective layer involves providing constituents similar to the ones in the active area, so that any plasma-wafer interactions, especially involving chemical reactions such as oxidation or reduction, would now occur in the protective layer, instead of the active area. Therefore this chemically protective layer would now endure any chemical disruption due to wafer-plasma interactions rather than the active area region.

[0050] As explained above, the "engineered" protective layer over active area region provides a dual function; a chemical protection where it reacts with the plasma preventing active area disruption, as well as a physical protection where it acts as a shield from penetrating ions. The protective layer can be formed under process and apparatus conditions with substantially lower ion energies, but not necessarily limited to those conditions. To illustrate an example of a protective layer, consider a p-type active area (i.e. B or BF2 implanted); where the active area

Si is strained with Ge for improved device performance, thus having a SiGe B doped active area. It is envisioned that with $SiF_4 + GeF_4 + B_2H_6$ (in addition to O_2 or N_2O & $C_xH_yF_z$), a thin protective area can be formed to physically shield the active area, and prevent any chemical losses of Si, Ge, or B from the active area.

[0051] As explained below, reduction in active area consumption can be achieved through the use of higher plasma power and higher pressure, reduction of active area Si consumption can be achieved through the use of process gas constituents which form a protective layer prior to crust removal and inert carrier gases can be used to lower ion energies.

[0052] With reference to FIGS. 2 and 3, active area material loss is correlated with penetration of ions into the substrate. More specifically, FIG. 2 shows simulation results of ion penetrations into SiO_2 and Si for various ion energies, typical in FEOL plasma processing, as a demonstration of the disruption to active area region caused by penetrating ions. FIG. 3 shows the relation of DC bias on material loss. As the ion energy increases, material loss increases, either due to dry processing alone, or post subsequent wet clean, due to the enhanced reactivity of the wet clean chemistry with the disrupted active area region. Even at zero bias there is significant material loss. In this case, most of the loss is due to ion energy imparted by the plasma potential. Ion energy can be reduced by reducing the plasma potential.

[0053] With reference to FIGS. 4 and 5, effects of chamber pressure and TCP power are discussed. In a TCP reactor, an increase in pressure can be used to reduce plasma potential and collisional slowing of ions, therefore lowering ion energy. FIG. 4 shows material loss as function of pressure. In addition, fluorocarbon and/or hydrofluorocarbon addition to the process gas can provide protection of the substrate. Preferably, one or more fluorocarbons or hydrofluorocarbons are added to oxygen (or other oxidants) to achieve a significant impact on material loss. FIG. 5 demonstrates the effect of TCP power on silicon loss for several processes. The data were obtained using a TCP reactor without a Faraday shield: The addition of CF_4 and CHF_3 coupled with increased TCP leads to reduction of silicon loss. However, a pure O_2 process, or addition of CH_3F, does not

lead to reduction of silicon loss at high TCP power. The increased TCP power leads to an increased plasma potential and CF_4 and CHF_3 additives are dissociated more at higher TCP power to provide increased number of polymerizable species, such as CF and CF_2. However, CH_3F cannot dissociate to form protective poly-fluorocarbons and hence leads to an increase in silicon loss. Not only does CH_3F not form poly-fluorocarbons, but at high TCP power CH_3F forms an excess of fluorine, thereby furthering the loss of silicon. The presence of fluorine and fluorocarbons in a plasma can lead to direct oxide loss by etching. However, higher TCP power does reduce the etch rate of silicon dioxide. The lower oxide etch rate for $O_2 + CH_3F$ suggests that other fluorocarbon or hydrofluorocarbon additives to oxygen may be able to achieve lower SiO_2 etch rates while keeping silicon loss low.

[0054] With reference to FIG. 6, it can be seen that the photoresist strip rate increases with increase in TCP power for four process gas chemistries (O_2+CF_4, O_2+CHF_3, O_2+CH_3F, O_2). A higher TCP power provides the advantage of a higher photoresist strip rate. This is an advantage since at a higher strip rate the exposure time of the substrate to the plasma will be shorter. A shorter time will mean lower material losses.

[0055] The addition of heavy inert gases such Kr or Xe can have a two fold effect. First, the heavy inert gases can lower the plasma potential since their ionization potential is lower than O_2. The potential is lowered since it requires less energy to ionize these high atomic number gases. This "cools" the plasma electrons leading to a lower plasma potential. Second, the presence of heavy inert gases can provide additional bombardment energy to the crust leading to its faster removal. The heavy atoms can also help remove residues. FIG. 7 shows the effect of addition of Xe to an O_2 TCP plasma on silicon loss in a TCP reactor without a Faraday shield.

[0056] FIG. 8 combines process regimes at lower plasma potential (lower ion energy – using high TCP power and high pressure), and formations of a protective layer over the active area. The results are outstanding with respect to Si loss. In essence, with roughly 12A of native oxide over the active area, and a protective layer using SiF_4, silicon loss can effectively be eliminated.

[0057] FIGS. 9 and 10 are illustrations of bad residue results where it can be seen crust is not clearly removed. FIGS. 11 and 12 are examples of early development of protective layer and residue results. FIG. 11 shows the evidence of a protective layer with SEM as well as the SIMS makeup of a protective layer. FIG. 13 demonstrates residue free performance using lower ion energy process window with a protective layer.

[0058] FIG. 14 shows the effect of using a pulsed plasma on silicon loss with a process gas of SiF_4+Ar compared to O_2+CH_3F. Active area protection was carried out for 4 seconds while the TCP reactor was run at 3 or 4.4 kW pulsed TCP power, 0 volt bias, 20°C substrate support temperature, 5 sccm SiF_4+250 sccm Ar, 90 mTorr chamber pressure followed by a photoresist strip for 60 seconds while in a second test the TCP reactor was run at 3 kW TCP power without pulsing, 0 volt bias, 20°C substrate support temperature, 10 sccm CH_3F+350 sccm O_2, 90 mTorr chamber pressure.

[0059] The influence of SiF_4 flow rate on silicon loss and oxide thickness are shown in FIG. 15. As the SiF_4 flow rate increases from 2 to 20 sccm, the oxide thickness increases from about 40Å to about 120Å wherein the silicon loss decreases from about 6Å to 0Å. To minimize increase in oxide thickness and silicon loss, a SiF_4 flow rate of about 5 to 10 sccm is preferred.

[0060] The influence of chamber pressure at two SiF_4 flow rates is shown in FIG. 16. As the pressure increases from 50 mTorr to 200 mTorr, the silicon loss increases from about 0.5 to about 2.5Å for a 10 sccm SiF_4 flow rate and from about 1Å to about 2.5Å for a 5 sccm SiF_4 flow rate. To minimize silicon loss, a SiF_4 flow rate of about 10 sccm at a chamber pressure of 50 to 100 mTorr is preferred.

[0061] The influence of spacing between the coil and the substrate is shown in FIG. 17. During removal of the photoresist, penetration of oxygen and fluorine into the active area causes silicon loss by forming a layer of SiOF in a region of the silicon adjacent the active area. As a result, the 6Å native oxide in effect becomes thicker and the silicon in the active area is lost due to conversion to the SiOF layer. The results shown in FIG. 17 show that silicon loss can be substantially improved when the coil to water spacing is changed from 18 to 28 cm.

[0062] It has been determined that silicon loss can be minimized without using a Faraday shield. Increasing of TCP power increases plasma density which leads to lower electron temperature. Lower electron temperature provides lower plasma potential seen by the wafer and thus lower ion energy. Thus, reducing plasma potential can provide less penetration of ions into the active area of the wafer. Faraday shields are used with inductively coupled plasma chambers to remove capacitive coupling from the induction coil. Such capacitive coupling from the coil can raise the relative plasma potential. However, capacitive coupling can also be minimized by plasma geometry modifications. Such modifications include thickness of the dielectric window beneath the coil, distance between the coil and the chamber walls, and distance between the substrate and the coil. It has been determined that by adjusting chamber geometry to reduce plasma potential, it is not necessary to include a Faraday shield to remove capacitively coupling from the inductive coil. For example, the window can be made at least 4 cm thick, the outer periphery of the coil can be spaced at least 5 cm from the inner wall of the chamber and/or the substrate can be located at least 10 cm, preferably at least 20 to 35 cm from the coil.

[0063] It will be apparent to those skilled in the art that various changes and modifications can be made, and equivalents employed, to the foregoing detailed description with reference to specific embodiments thereof, without departing from the scope of the appended claims.

What is claimed is:

1. A method of protecting an active area on a substrate, comprising:

positioning a substrate in an inductively coupled plasma processing chamber of a plasma reactor, the plasma reactor including a dielectric window overlying the substrate and at least one coil which inductively couples RF energy through the dielectric window and into a space between the dielectric window and the substrate, the substrate including an active area;

supplying a process gas to the plasma processing chamber,

generating a plasma from the process gas by supplying power to the coil;

processing the substrate with the plasma so as to protect the active area by (a) maintaining a plasma potential of about 5 to 15 volts at the substrate during the processing and/or (b) passivating the active area by using a silane-free process gas comprising at least one additive effective to form a protective layer on an active area of the substrate wherein the protective layer includes at least one element from the additive which is already present in the active area.

2. The method of Claim 1, wherein the additive element comprises Si, Ge, As, Sb, In, P and/or B and compounds thereof including BF_2.

3. The method of Claim 1, wherein the passivating is carried out while pulsing supply of power to the coil with power on for 2 to 20 μsec and power off for 30 to 100 μsec.

4. The method of Claim 1, wherein the passivating is carried out while supplying 400 to 10,000 watts of power to the coil.

5. The method of Claim 1, wherein the passivating is carried out without RF bias applied to the substrate.

6. The method of Claim 1, wherein the method is carried out while maintaining the chamber at a pressure of 10 to 500 mTorr.

7. The method of Claim 1, wherein in the passivating the process gas includes at least one of SiF_4, O_2, Ar, Ne, Kr, Xe, C_xF_y where $x \geq 1$ and $y \geq 2$, $C_xF_yH_z$ where $x \geq 1$, $y \geq 2$ and $z \geq 1$.

8. The method of Claim 1, further comprising stripping photoresist from the substrate.

9. The method of Claim 1, wherein the coil is a planar coil and the substrate is spaced 10 to 30 cm from the coil during the processing.

10. The method of Claim 1, wherein the process gas includes 100 to 800 sccm total of O_2, Ar, Ne, Kr and Xe during the processing.

11. The method of Claim 1, wherein the dielectric window is at least 4 cm thick, the coil has an outer periphery spaced inward of the inner wall of the chamber by at least 5 cm, the substrate is spaced at least 10 cm from the coil, and the chamber does not include a Faraday shield.

12. The method of Claim 1, further comprising stripping an ion-implanted photoresist from the substrate.

13. The method of Claim 1, wherein a silicon-oxide layer overlies the active area and the additive is present in an amount effective to passivate the silicon-containing layer.

14. The method of Claim 1, wherein the processing is carried out by passivating the active layer for less than 10 seconds.

15. The method of Claim 13, wherein the silicon oxide layer is a native oxide, a thermally grown oxide, or is formed by CVD or ion immersion.

16. The method of Claim 13, wherein the silicon oxide layer has a thickness of 20 to 40Å or less than or equal to 20 Δ.

17. The method of Claim 1, further comprising stripping photoresist on the substrate with an oxygen plasma in the chamber, wherein the substrate includes silicon in the active region and no more than 2 Δ of the silicon is lost by conversion during the stripping.

18. The method of Claim 1, wherein the substrate is supported on a substrate support maintained at a temperature of -20 to 75°C and pressure in the chamber is less than 500 mTorr during the processing.

19. The method of Claim 1, further comprising, after the processing, cleaning the substrate with deionized water or other wet clean chemistry.

20. The method of Claim 1, wherein the plasma chamber does not include a Faraday shield.