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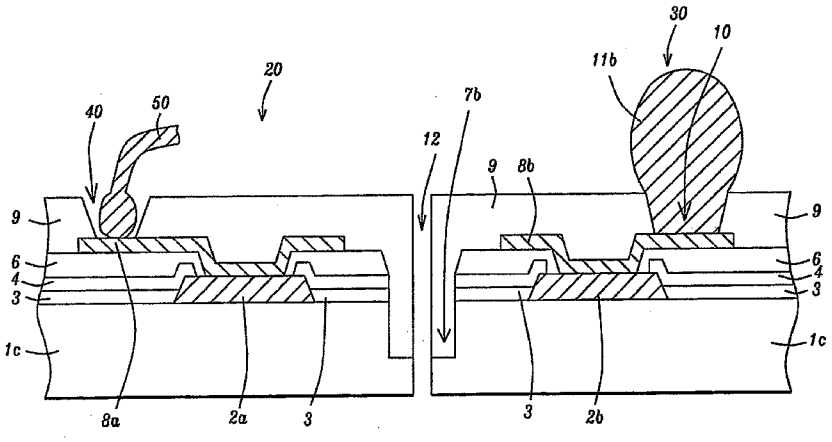
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(54) **Title:** POLYMER ENCAPSULATED DICING LANE (PEDL) TECHNOLOGY FOR Cu/LOW/ULTRA-LOW k DEVICES



(57) **Abstract:** A process for packaging semiconductor devices for flip chip and wire bond applications, wherein specific material the semiconductor devices are protected during device processing sequences and dicing procedures. After definition the copper interconnect structures [2a] surrounded by a low k insulator layer [4], a protective, first photosensitive polymer layer [6] comprised with a low dielectric constant is applied. Openings are then defined in the f photosensitive polymer layer exposing portions of the top surface of the copper interconnect structures, and a dicing lane opening is defined in materials between copper interconnect. An opening is defined in the second photosensitive polymer layer [9] followed by a placement of the solder ball. A reflow anneal procedure results in the solder wetting only the portion of the exposed redistribution shape. Solder ball, flip chip regions are separated from the bond regions by dicing performed in the dicing lane [7b].

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