

MEMORY CELLS, NON-VOLATILE MEMORY ARRAYS, METHODS OF
OPERATING MEMORY CELLS, METHODS OF READING TO AND
WRITING FROM A MEMORY CELL, AND METHODS OF PROGRAMMING
A MEMORY CELL

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TECHNICAL FIELD

Embodiments disclosed herein pertain to memory cells, to non-volatile
memory arrays, to methods of operating memory cells, to methods of reading to
and writing from a memory cell, and to methods of programming a memory cell.

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BACKGROUND

Memory is one type of integrated circuitry, and is used in computer
systems for storing data. Such is typically fabricated in one or more arrays of
individual memory cells. The memory cells might be volatile, semi-volatile, or
non-volatile. Non-volatile memory cells can store data for extended periods of
time, and in many instances when the computer is turned off. Volatile memory
dissipates and therefore is required to be refreshed/rewritten, and in many
instances multiple times per second. Regardless, the smallest unit in each array
is termed as a memory cell and is configured to retain or store memory in at
least two different selectable states. In a binary system, the storage conditions
are considered as either a "0" or a "1". Further, some individual memory cells
can be configured to store more than two bits of information.

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Integrated circuitry fabrication continues to strive to produce smaller and
denser integrated circuits. Accordingly, the fewer components an individual
circuit device has, the smaller the construction of the finished device can be.
Likely the smallest and simplest memory cell will be comprised of two
conductive electrodes having a programmable material received there-between.

quantity of the fluorine vacancies in the locations where such are received. In such embodiment, lateral region 24 may or may not comprise MgF_2 having lower density of or no fluorine vacancies in comparison to lateral region 22.

In one embodiment, the mobile dopants comprise aluminum atom
5 interstitials in a nitrogen-containing material. In one embodiment, the mobile dopants comprise Cu atoms or ions in any of HfO_2 , ZrO_2 , GeO_x , and SiO_2 . In one embodiment, the mobile dopants comprise or Ag in amorphous silicon and/or chalcogen glasses (i.e., GeS and/or GeSe).

Material 16 may be of any suitable thickness T and of any suitable lateral
10 width W that may be dependent upon composition of surrounding material such as dielectric, upon composition of the mobile dopants, if present, within said surrounding material, and/or upon the quantity of mobile dopants present in said surrounding material. Dimensions T and W, respectively, may be constant (as shown) or may be variable. Regardless, in one embodiment, the resistance
15 switchable material has a minimum elevational thickness that is at least twice as great as its minimum lateral width. Example thicknesses T include from about 50 nanometers to about 150 nanometers, with an example width W being no greater than 25 nanometers. In one embodiment where memory cell 10 is in the "off" or "0" state of Fig. 1, a very high electric field would be required in the T
20 oriented direction for current to flow between opposing electrodes 12 and 14 upon application of suitable differential voltage to electrodes 12 and 14. In one embodiment, such required field is at least 50 megavolts/meter, and in one embodiment is at least 500 megavolts/meter.

Fig. 1 depicts memory cell 10 in a high or highest resistance state, while
25 Fig. 2 depicts memory cell 10 in a low or lowest resistance state. Resistance

switchable material 22 in the lowest resistance state of Fig. 2 comprises a conductive channel/filament 26 which is localized along only one of the two laterally opposing edges 18, 20 and extends toward and away from first and second electrodes 12 and 14. Conductive channel 26 may or may not contact at least one of conductive electrodes 12 and 14, with the embodiment of Fig. 2 showing such conductive channel contacting each of first conductive electrode 12 and second conductive electrode 14. Regardless, conductive channel 26 may or may not be of constant lateral width along its length. Fig. 2 depicts an embodiment wherein conductive channel 26 is of constant lateral width along its length. As an example where channel/region 26 comprises oxygen vacancies as mobile dopants that are received in surrounding TiO₂, an overall average oxygen vacancy density greater than 5×10^{18} vacancies/cm³ may render region/channel 26 electrically conductive.

Conductive channel 26 may have constant conductivity per unit length of channel 26 between first and electrodes 12 and 14 (i.e. the same conductivity along all of the shortest straight-line distance between electrodes 12 and 14.) Such is exemplified in Fig. 2 by the depicted constant density of stippling within region 26 between electrodes 12 and 14. Fig. 3 depicts an alternate embodiment low or lowest resistance state memory cell 10a. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "a". In Fig. 3, conductive channel 26a has greater conductivity per unit length of channel 26a more proximate one of the first and second electrodes (i.e., electrode 12) than proximate the other of the first or second electrodes (i.e., electrode 14). Such is exemplified in Fig. 3 by the depicted greater density of stippling proximate

electrode 12 along some fractional amount of the shortest straight-line distance within region 26a between electrodes 12 and 14 than proximate electrode 14 along the same fractional amount.

Figs. 2 and 3 depict embodiments wherein conductive channels 26 and 26a are each of some respective constant lateral width along their lengths.

Fig. 4 depicts an alternate embodiment low or lowest resistance state memory cell 10b where a conductive channel 26b has variable lateral width. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being indicated with the suffix “b”. Additionally, Fig. 4 depicts an example embodiment wherein a conductive channel 26b is narrower more proximate one of the electrodes than it is proximate the other of the electrodes. Further in such embodiment where, for example, conductivity is achieved or increases due to greater mobile dopant density, conductive channel 26b may have constant conductivity per unit length analogous to the embodiment of Fig. 2 as described above and as shown.

Fig. 5 depicts an alternate embodiment low or lowest resistance state memory cell 10cb where a conductive channel 26c has variable lateral width. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being indicated with the suffix “c”. Fig. 5 depicts an example embodiment wherein conductive channel 26c has greater conductivity per unit length more proximate one of the first and second electrodes than proximate the other of the first or second electrodes analogous to the embodiment of Fig. 3 as described above and as shown. Regardless, Figs. 4 and 5 also depict embodiments wherein the conductive formed channels have a

respective tapered or wedge-like shape. The embodiments of Fig. 2-5 may be programmed back to the Fig. 1 state, or to some other state(s).

The above-depicted embodiments show first and second lateral regions 22, 24 being of different composition relative one another in the programmed state of Fig. 1 and in the programmed states of Figs. 2-5. Fig. 6 depicts an alternate example embodiment memory cell 10d (in a low or lowest resistance state) having a substantially homogenous resistance switchable material 16d that is capable of being repeatedly programmed to at least two different resistance states. Like numerals from the above-described

embodiments have been utilized where appropriate, with some construction differences being indicated with the suffix "d". Memory cell 10d of Fig. 6 may be programmed to a low or lowest resistance state which comprises a conductive channel (not shown) as described above in connection with the embodiments of Figs. 2-5, and then programmed back to the Fig. 6 state, or to some other state(s). Accordingly, the embodiment of Fig. 6 may also be repeatedly programmed between lower or lowest resistance states and higher or highest resistance states.

In one embodiment, a method of programming a memory cell comprising a pair of opposing conductive electrodes having resistance switchable material received there-between includes application of an electric field through the resistance switchable material. Such field is applied in a prevailingly laterally oriented direction to cause mobile dopants within the resistance switchable material to move laterally toward or away from one of the opposing lateral edges of the resistance switchable material to change resistance between the pair of electrodes. A prevailingly laterally oriented direction does not have to be

CLAIMS:

1. A method of operating a memory cell comprising using different electrodes to change a programmed state of the memory cell than are used to read the programmed state of the memory cell.

2. A method of writing to and reading from a memory cell comprising using first and second opposing electrodes to read from the memory cell and using third and fourth opposing electrodes to write to the memory cell; the first, second, third, and fourth electrodes constituting different electrodes.

3. A method of programming a memory cell comprising a pair of opposing conductive electrodes having resistance switchable material received there-between, comprising:

applying an electric field through the resistance switchable material in a prevailingly laterally oriented direction to cause mobile dopants within the resistance switchable material to move laterally toward or away from one of opposing lateral edges of the resistance switchable material to change resistance between the pair of electrodes, the resistance switchable material retaining the changed resistance after said applied electric field is removed.

4. The method of claim 3 wherein the applying of the electric field comprises applying a voltage differential across two additional conductive electrodes received laterally of opposing sides of the pair of opposing conductive electrodes, the two additional conductive electrodes being electrically insulated from the pair of opposing conductive electrodes during the applying of the electric field.

5. The method of claim 4 wherein the two additional conductive electrodes across which said voltage differential is applied are received elevationally away from the resistance switchable material.

6. The method of claim 4 wherein the two additional conductive electrodes across which said voltage differential is applied elevationally overlap the resistance switchable material.

7. The method of claim 6 wherein the two additional conductive electrodes across which said voltage differential is applied are elevationally coincident with the resistance switchable material.

8. The method of claim 3 wherein the opposing conductive electrodes of the pair are pulled to substantially the same voltage during said applying.

9. The method of claim 8 wherein each of the pair of opposing conductive electrodes is pulled to 0V during said applying.

10. The method of claim 3 wherein no external voltage is applied to the pair of opposing conductive electrodes during said applying.

11. A method of writing to and reading from a cross point memory cell of an array of cross point memory cells comprising a plurality of word lines and a plurality of bit lines crossing the plurality of word lines, individual of the cross point memory cells comprising a different one of the crossings of the plurality of word lines and the plurality of bit lines relative to one another, the method comprising:

writing to a memory cell by applying a differential write voltage between the two immediately adjacent bit lines which are on opposing lateral sides of said memory cell; and

reading from the memory cell by applying a differential read voltage between the crossing word line and the crossing bit line of the memory cell and sensing current resulting from the applying of the read voltage.

12. The method of claim 11 wherein the two immediately adjacent bit lines are electrically insulated from the memory cell.

13. The method of claim 11 wherein the differential read voltage and the differential write voltage are different from one another.

14. The method of claim 11 wherein the individual memory cells comprise resistance switchable material received between the crossing word lines and bit lines, the writing comprising switching the resistance of the resistance switchable material between at least two different resistance states which statically remains in a programmed resistance state until programmed to a different resistance state.

15. The method of claim 14 wherein the writing comprises causing mobile dopants within the resistance switchable material to move laterally toward or away from one of opposing lateral edges of the resistance switchable material.

16. The method of claim 15 wherein the writing moves the mobile dopants toward the one lateral edge to form a conductive channel which is localized along the one lateral edge.

17. The method of claim 16 wherein the writing forms the conductive channel to be of constant lateral width between the crossing word line and bit line of the memory cell.

18. The method of claim 17 wherein the writing forms the conductive channel to be of constant conductivity per unit length of the channel between the crossing bit line and crossing word line of the memory cell.

19. The method of claim 17 wherein the writing forms the conductive channel to be more conductive per unit length of the channel more proximate the crossing bit line of the memory cell than proximate the crossing word line of the memory cell.

20. The method of claim 16 wherein the writing forms the conductive channel to be of variable lateral width between the crossing word line and bit line of the memory cell.

21. The method of claim 20 wherein the writing forms the conductive channel to be wider more proximate the crossing bit line of the memory cell than proximate the crossing word line of the memory cell.

22. The method of claim 21 wherein the writing forms the conductive channel to be of constant conductivity per unit length of the channel between the crossing bit line and crossing word line of the memory cell.

23. The method of claim 21 wherein the writing forms the conductive channel to be more conductive per unit length of the channel more proximate the crossing bit line of the memory cell than proximate the crossing word line of the memory cell.

24. The method of claim 20 wherein the writing forms the lateral width of the conductive channel to taper.

25. The method of claim 15 wherein,
the resistance switchable material comprises a conductive channel of the mobile dopants which is localized along the one lateral edge; and
the writing moves the mobile dopants away from the one lateral edge to remove the conductive channel.

26. The method of claim 11 wherein the writing is simultaneously to multiple memory cells received between said pair of immediately adjacent bit lines.

27. The method of claim 11 further comprising during the writing, applying a voltage to at least some other word lines other than the crossing word line of the memory cell and that is different from any voltage that is applied to the crossing word line.

28. The method of claim 27 wherein the applying of the voltage to at least some other word lines results in an electric field component directionally different from an electric field component resulting from applying of the differential write voltage.

29. The method of claim 27 wherein the applying of the voltage to at least some other word lines prevents other memory cells associated with the other word lines from being written to by the differential write voltage.

30. A method of writing to cross point memory cells of an array of cross point memory cells comprising a plurality of word lines and a plurality of bit lines crossing the plurality of word lines, individual of the cross point memory cells comprising a different one of the crossings of the plurality of word lines and the plurality of bit lines relative to one another, the method comprising:

writing to a memory cell by applying a differential write voltage between the two immediately adjacent bit lines which are on opposing lateral sides of said memory cell.

31. The method of claim 30 comprising simultaneously writing to multiple memory cells received between said two immediately adjacent bit lines.

32. A memory cell comprising:

first and second opposing electrodes having resistance switchable material received there-between, the resistance switchable material being capable of being repeatedly programmed to at least two different resistance states, the resistance switchable material in a lowest resistance state comprising a conductive channel localized along only one of two laterally opposing edges of the resistance switchable material and extending toward and away from the first and second electrodes.

33. The memory cell of claim 32 wherein the conductive channel contacts at least one of the first and second conductive electrodes.

34. The memory cell of claim 33 wherein the conductive channel contacts each of the first and second conductive electrodes.

35. The memory cell of claim 32 wherein the resistance switchable material has a minimum elevational thickness that is at least twice as great as its minimum lateral width.

36. The memory cell of claim 32 wherein the conductive channel is of constant lateral width.

37. The memory cell of claim 36 wherein the conductive channel has constant conductivity per unit length of the channel between the first and second electrodes.

38. The memory cell of claim 36 wherein the conductive channel has greater conductivity per unit length of the channel more proximate one of the first and second electrodes than proximate the other of the first and second electrodes.

39. The memory cell of claim 32 wherein the conductive channel is of variable lateral width.

40. The memory cell of claim 39 wherein the conductive channel has constant conductivity per unit length of the channel between the first and second electrodes.

41. The memory cell of claim 39 wherein the conductive channel has greater conductivity per unit length of the channel more proximate one of the first and second electrodes than proximate the other of the first and second electrodes.

42. The memory cell of claim 39 wherein the conductive channel is narrower and more conductive proximate one of the electrodes than it is proximate the other electrode.

43. The memory cell of claim 32 comprising a cross point memory cell, one of the opposing electrodes comprising a word line extending in a first direction, the other of the opposing electrodes comprising a bit line extending in a second direction different from the first direction.

44. The memory cell of claim 43 wherein the conductive channel is wider more proximate the bit line than proximate the word line.

45. A memory cell comprising:

first and second opposing electrodes having material received there-between, the material comprising first and second lateral regions of different composition relative one another, one of the first and second lateral regions being received along one of two laterally opposing edges of the material, another of the first and second lateral regions being received along the other of said two laterally opposing edges of the material, at least one of the first and second lateral regions being capable of being repeatedly programmed to at least two different resistance states.

46. The memory cell of claim 45 wherein only one of the first and second regions is capable of being repeatedly programmed to at least two different resistance states.

47. A non-volatile memory array comprising:

a plurality of word lines;

a plurality of bit lines crossing the plurality of word lines; and

a plurality of memory cells individually corresponding to a different one of the crossings of the plurality of word lines and the plurality of bit lines relative to one another, the memory cells individually comprising resistance switchable material received between the word lines and the bit lines where such cross and which is capable of being repeatedly programmed to at least two different resistance states, the resistance switchable material of at least one of the memory cells comprising a conductive channel localized along only one of two laterally opposing edges of said at least one memory cell and extending toward and away from the crossing word line and bit line.

Memory Cells, Non-Volatile Memory Arrays, Methods Of Operating Memory Cells, Methods Of Writing To And Reading From A Memory Cell, And Methods Of Programming A Memory Cell

TECHNICAL FIELD

Embodiments disclosed herein pertain to memory cells, to non-volatile memory arrays, to methods of operating memory cells, to methods of writing to and reading from a memory cell, and to methods of programming a memory cell.

BACKGROUND

Memory is one type of integrated circuitry, and is used in computer systems for storing data. Such is typically fabricated in one or more arrays of individual memory cells. The memory cells might be volatile, semi-volatile, or non-volatile. Non-volatile memory cells can store data for extended periods of time, and in many instances when the computer is turned off. Volatile memory dissipates and therefore is required to be refreshed/rewritten, and in many instances multiple times per second. Regardless, the smallest unit in each array is termed as a memory cell and is configured to retain or store memory in at least two different selectable states. In a binary system, the storage conditions are considered as either a "0" or a "1". Further, some individual memory cells can be configured to store more than two bits of information.

Integrated circuitry fabrication continues to strive to produce smaller and denser integrated circuits. Accordingly, the fewer components an individual circuit device has, the smaller the construction of the finished device can be. Likely the smallest and simplest memory cell will be comprised of two conductive electrodes having a programmable material received there-between.

quantity of the fluorine vacancies in the locations where such are received. In such embodiment, lateral region 24 may or may not comprise MgF_2 having lower density of or no fluorine vacancies in comparison to lateral region 22.

5 In one embodiment, the mobile dopants comprise aluminum atom interstitials in a nitrogen-containing material. In one embodiment, the mobile dopants comprise Cu atoms or ions in any of HfO_2 , ZrO_2 , GeO_x , and SiO_2 . In one embodiment, the mobile dopants comprise Ag in amorphous silicon and/or chalcogen glasses (i.e., GeS and/or GeSe).

Material 16 may be of any suitable thickness T and of any suitable lateral
10 width W that may be dependent upon composition of surrounding material such as dielectric, upon composition of the mobile dopants, if present, within said surrounding material, and/or upon the quantity of mobile dopants present in said surrounding material. Dimensions T and W, respectively, may be constant (as shown) or may be variable. Regardless, in one embodiment, the resistance
15 switchable material has a minimum elevational thickness that is at least twice as great as its minimum lateral width. Example thicknesses T include from about 50 nanometers to about 150 nanometers, with an example width W being no greater than 25 nanometers. In one embodiment where memory cell 10 is in the "off" or "0" state of Fig. 1, a very high electric field would be required in the T
20 oriented direction for current to flow between opposing electrodes 12 and 14 upon application of suitable differential voltage to electrodes 12 and 14. In one embodiment, such required field is at least 50 megavolts/meter, and in one embodiment is at least 500 megavolts/meter.

Fig. 1 depicts memory cell 10 in a high or highest resistance state, while
25 Fig. 2 depicts memory cell 10 in a low or lowest resistance state. Resistance

switchable material 22 in the lowest resistance state of Fig. 2 comprises a conductive channel/filament 26 which is localized along only one of the two laterally opposing edges 18, 20 and extends toward and away from first and second electrodes 12 and 14. Conductive channel 26 may or may not contact at least one of conductive electrodes 12 and 14, with the embodiment of Fig. 2 showing such conductive channel contacting each of first conductive electrode 12 and second conductive electrode 14. Regardless, conductive channel 26 may or may not be of constant lateral width along its length. Fig. 2 depicts an embodiment wherein conductive channel 26 is of constant lateral width along its length. As an example where channel/region 26 comprises oxygen vacancies as mobile dopants that are received in surrounding TiO_2 , an overall average oxygen vacancy density greater than 5×10^{18} vacancies/cm³ may render region/channel 26 electrically conductive.

Conductive channel 26 may have constant conductivity per unit length of channel 26 between first and second electrodes 12 and 14 (i.e. the same conductivity along all of the shortest straight-line distance between electrodes 12 and 14.) Such is exemplified in Fig. 2 by the depicted constant density of stippling within region 26 between electrodes 12 and 14. Fig. 3 depicts an alternate embodiment low or lowest resistance state memory cell 10a. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "a". In Fig. 3, conductive channel 26a has greater conductivity per unit length of channel 26a more proximate one of the first and second electrodes (i.e., electrode 12) than proximate the other of the first or second electrodes (i.e., electrode 14). Such is exemplified in Fig. 3 by the depicted greater density of stippling proximate electrode 12 along some fractional amount of the shortest straight-line distance within region 26a between electrodes 12 and 14 than proximate electrode 14 along the same fractional amount.

Figs. 2 and 3 depict embodiments wherein conductive channels 26 and 26a are each of some respective constant lateral width along their lengths.

Fig. 4 depicts an alternate embodiment low or lowest resistance state memory cell 10b where a conductive channel 26b has variable lateral width. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "b". Additionally, Fig. 4 depicts an example embodiment wherein a conductive channel 26b is narrower more proximate one of the electrodes than it is proximate the other of the electrodes. Further in such embodiment where, for example, conductivity is achieved or increases due to greater mobile dopant density, conductive channel 26b may have constant conductivity per unit length analogous to the embodiment of Fig. 2 as described above and as shown.

Fig. 5 depicts an alternate embodiment low or lowest resistance state memory cell 10c where a conductive channel 26c has variable lateral width. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "c". Fig. 5 depicts an example embodiment wherein conductive channel 26c has greater conductivity per unit length more proximate one of the first and second electrodes than proximate the other of the first or second electrodes analogous to the embodiment of Fig. 3 as described above and as shown. Regardless, Figs. 4 and 5 also depict embodiments wherein the conductive formed channels have a respective tapered or wedge-like shape. The embodiments of Fig. 2-5 may be programmed back to the Fig. 1 state, or to some other state(s).

The above-depicted embodiments show first and second lateral regions 22, 24 being of different composition relative one another in the programmed state of Fig. 1 and in the programmed states of Figs. 2-5. Fig. 6 depicts an alternate example embodiment memory cell 10d (in a low or lowest resistance state) having a substantially homogenous resistance switchable material 16d that is capable of being repeatedly programmed to at least two different resistance states. Like numerals from the above-described embodiments have been utilized where appropriate, with some construction differences being indicated with the suffix "d". Memory cell 10d of Fig. 6 may be programmed to a low or lowest resistance state which comprises a conductive channel (not shown) as described above in connection with the embodiments of Figs. 2-5, and then programmed back to the Fig. 6 state, or to some other state(s). Accordingly, the embodiment of Fig. 6 may also be repeatedly programmed between lower or lowest resistance states and higher or highest resistance states.

In one embodiment, a method of programming a memory cell comprising a pair of opposing conductive electrodes having resistance switchable material received there-between includes application of an electric field through the resistance switchable material. Such field is applied in a prevailingly laterally oriented direction to cause mobile dopants within the resistance switchable material to move laterally toward or away from one of the opposing lateral edges of the resistance switchable material to change resistance between the pair of electrodes. A prevailingly laterally oriented direction does not have to be

The invention claimed is:

1. A method of programming a memory cell comprising a pair of opposing conductive electrodes having resistance switchable material received there-between, comprising:

applying an electric field through the resistance switchable material in a prevailingly laterally oriented direction to cause mobile dopants within the resistance switchable material to move laterally toward or away from one of opposing lateral edges of the resistance switchable material to change resistance between the pair of electrodes, the resistance switchable material retaining the changed resistance after said applied electric field is removed.

2. The method of claim 1 wherein the applying of the electric field comprises applying a voltage differential across two additional conductive electrodes received laterally of opposing sides of the pair of opposing conductive electrodes, the two additional conductive electrodes being electrically insulated from the pair of opposing conductive electrodes during the applying of the electric field.

3. The method of claim 2 wherein the two additional conductive electrodes across which said voltage differential is applied are received elevationally away from the resistance switchable material.

4. The method of claim 2 wherein the two additional conductive electrodes across which said voltage differential is applied elevationally overlap the resistance switchable material.

5. The method of claim 4 wherein the two additional conductive electrodes across which said voltage differential is applied are elevationally coincident with the resistance switchable material.

6. The method of claim 1 wherein the opposing conductive electrodes of the pair are pulled to substantially the same voltage during said applying.

7. The method of claim 6 wherein each of the pair of opposing conductive electrodes is pulled to 0V during said applying.

8. The method of claim 1 wherein no external voltage is applied to the pair of opposing conductive electrodes during said applying.

9. A method of writing to and reading from a cross point memory cell of an array of cross point memory cells comprising a plurality of word lines and a plurality of bit lines crossing the plurality of word lines, individual of the cross point memory cells comprising a different one of the crossings of the plurality of word lines and the plurality of bit lines relative to one another, the method comprising:

writing to a memory cell by applying a differential write voltage between the two immediately adjacent bit lines which are on opposing lateral sides of said memory cell; and

reading from the memory cell by applying a differential read voltage between the crossing word line and the crossing bit line of the memory cell and sensing current resulting from the applying of the read voltage.

10. The method of claim 9 wherein the two immediately adjacent bit lines are electrically insulated from the memory cell.

11. The method of claim 9 wherein the differential read voltage and the differential write voltage are different from one another.

12. The method of claim 9 wherein the individual memory cells comprise resistance switchable

material received between the crossing word lines and bit lines, the writing comprising switching the resistance of the resistance switchable material between at least two different resistance states which statically remains in a programmed resistance state until programmed to a different resistance state.

13. The method of claim 12 wherein the writing comprises causing mobile dopants within the resistance switchable material to move laterally toward or away from one of opposing lateral edges of the resistance switchable material.

14. The method of claim 13 wherein the writing moves the mobile dopants toward the one lateral edge to form a conductive channel which is localized along the one lateral edge.

15. The method of claim 14 wherein the writing forms the conductive channel to be of constant lateral width between the crossing word line and bit line of the memory cell.

16. The method of claim 15 wherein the writing forms the conductive channel to be of constant conductivity per unit length of the channel between the crossing bit line and crossing word line of the memory cell.

17. The method of claim 15 wherein the writing forms the conductive channel to be more conductive per unit length of the channel more proximate the crossing bit line of the memory cell than proximate the crossing word line of the memory cell.

18. The method of claim 14 wherein the writing forms the conductive channel to be of variable lateral width between the crossing word line and bit line of the memory cell.

19. The method of claim 18 wherein the writing forms the conductive channel to be wider more proximate the crossing bit line of the memory cell than proximate the crossing word line of the memory cell.

20. The method of claim 19 wherein the writing forms the conductive channel to be of constant conductivity per unit length of the channel between the crossing bit line and crossing word line of the memory cell.

21. The method of claim 19 wherein the writing forms the conductive channel to be more conductive per unit length of the channel more proximate the crossing bit line of the memory cell than proximate the crossing word line of the memory cell.

22. The method of claim 18 wherein the writing forms the lateral width of the conductive channel to taper.

23. The method of claim 13 wherein, the resistance switchable material comprises a conductive channel of the mobile dopants which is localized along the one lateral edge; and the writing moves the mobile dopants away from the one lateral edge to remove the conductive channel.

24. The method of claim 9 wherein the writing is simultaneously to multiple memory cells received between said pair of immediately adjacent bit lines.

25. The method of claim 9 further comprising during the writing, applying a voltage to at least some other word lines other than the crossing word line of the memory cell and that is different from any voltage that is applied to the crossing word line.

26. The method of claim 25 wherein the applying of the voltage to at least some other word lines

results in an electric field component directionally different from an electric field component resulting from applying of the differential write voltage.

27. The method of claim 25 wherein the applying of the voltage to at least some other word lines prevents other memory cells associated with the other word lines from being written to by the differential write voltage.

28. A method of writing to cross point memory cells of an array of cross point memory cells comprising a plurality of word lines and a plurality of bit lines crossing the plurality of word lines, individual of the cross point memory cells comprising a different one of the crossings of the plurality of word lines and the plurality of bit lines relative to one another, the method comprising:

writing to a memory cell by applying a differential write voltage between the two immediately adjacent bit lines which are on opposing lateral sides of said memory cell.

29. The method of claim 28 comprising simultaneously writing to multiple memory cells received between said two immediately adjacent bit lines.

30. A memory cell comprising:

first and second opposing electrodes having resistance switchable material received there-between, the resistance switchable material being capable of being repeatedly programmed to at least two different resistance states, the resistance switchable material in a lowest resistance state comprising a conductive channel localized along only one of two laterally opposing edges of the resistance switchable material and extending toward and away from the first and second electrodes.

31. A non-volatile memory array comprising:

a plurality of word lines;

a plurality of bit lines crossing the plurality of word lines; and

a plurality of memory cells individually corresponding to a different one of the crossings of the plurality of word lines and the plurality of bit lines relative to one another, the memory cells individually comprising resistance switchable material received between the word lines and the bit lines where such cross and which is capable of being repeatedly programmed to at least two different resistance states, the resistance switchable material of at least one of the memory cells comprising a conductive channel localized along only one of two laterally opposing edges of said at least one memory cell and extending toward and away from the crossing word line and bit line.

32. The memory cell of claim 30 wherein the conductive channel contacts at least one of the first and second conductive electrodes.

33. The memory cell of claim 32 wherein the conductive channel contacts each of the first and second conductive electrodes.

34. The memory cell of claim 30 wherein the resistance switchable material has a minimum elevational thickness that is at least twice as great as its minimum lateral width.

35. The memory cell of claim 30 wherein the conductive channel is of constant lateral width.

36. The memory cell of claim 35 wherein the conductive channel has constant conductivity per unit length of the channel between the first and second electrodes.

37. The memory cell of claim 35 wherein the conductive channel has greater conductivity per unit length of the channel more proximate one of the first and second electrodes than proximate the other of the first and second electrodes.

38. The memory cell of claim 30 wherein the conductive channel is of variable lateral width.

39. The memory cell of claim 38 wherein the conductive channel has constant conductivity per unit length of the channel between the first and second electrodes.

40. The memory cell of claim 38 wherein the conductive channel has greater conductivity per unit length of the channel more proximate one of the first and second electrodes than proximate the other of the first and second electrodes.

41. The memory cell of claim 38 wherein the conductive channel is narrower and more conductive proximate one of the electrodes than it is proximate the other electrode.

42. The memory cell of claim 30 comprising a cross point memory cell, one of the opposing electrodes comprising a word line extending in a first direction, the other of the opposing electrodes comprising a bit line extending in a second direction different from the first direction.

43. The memory cell of claim 42 wherein the conductive channel is wider more proximate the bit line than proximate the word line.