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"A recording/playing circuit".

The present invention relates to a recording/playing circuit in a recording/playing apparatus for magnetic tapes.

A recording/playing circuit as shown in Figure 1 of the accompanying drawings has already been proposed by us, and is described in catalogue "'79 SEMICONDUCTOR DATA BOOK" (pp. 144 - 157) which was published in December 1979 by us.

This circuit includes: a switching circuit 1 for switching recording/playing signals (R_{IN}/P_{IN}), the switching circuit 1 utilizing a differential transistor circuit; a noise reduction circuit consisting of an expander/compressor 4 for higher frequency signals; and a switching circuit 2 which is similar to the switching circuit 1. A muting circuit consists of a switching circuit 3 similar to the switching circuit 1, the muting circuit being provided in the playing output in order to prevent a shock noise at the recording/playing switching

in the playing output.

The circuit also includes a control circuit 7, which forms a recording/playing switching signal R/P and a mute signal M. The circuit further includes a head-
5 phone amplifier 5, and a recording amplifier 6.

We have found that the above circuit shown in Figure 1 has the disadvantage that three sets of switching circuits are required and that when the circuit is fabricated in the form of a monolithic integrated
10 circuit as shown in Figure 1, a large number of external terminals are needed.

It is therefore an object of the present invention to provide an improved recording/playing circuit.

According to the present invention there is
15 provided a recording/playing circuit including:

(a) a noise reduction circuit in the form of an expander/compressor having a pre-amplifier, a combining network, an inverter circuit and a network for deriving only a high frequency signal;

20 (b) a first switching circuit which includes first, second and third input positions and an output terminal, wherein said first input position is coupled to an output of said pre-amplifier of said expander/compressor said second input position is coupled to
25 an output of said inverter circuit of said expander/compressor, said output

terminal is coupled to said high frequency signal deriving network of said expander/compressor and said third input position is provided to perform a muting function; and

(c) a control circuit which serves to transmit
5 to said output terminal of said switching circuit selectively one of electric signals applied to said first, second and third input positions of said switching circuit.

The present invention will now be described in
10 greater detail by way of example with reference to the remaining figures of the accompanying drawings, wherein:-

Figure 2 is a block circuit diagram showing a preferred embodiment of a recording/playing circuit;

Figure 3 is a circuit diagram showing a first
15 detailed arrangement of the circuit shown in Figure 2; and

Figure 4 is a circuit diagram showing a second detailed arrangement of the circuit shown in Figure 2.

Referring first to the circuit shown in Figure 2, the arrangement is such that the switching between a
20 recording signal R_{IN} and a playing signal P_{IN} is effected by a switching circuit 1 which utilizes a differential transistor circuit, and that a noise reduction circuit which consists of an expander/compressor 4 for higher frequencies and a switching circuit 2' having a muting

function is arranged in a stage following the switching circuit 1.

The expander/compressor 4 consists of a pre-amplifier 4a, an adder network 4d which adds the
5 output of the pre-amplifier and the output of a network 4c for deriving only a high frequency signal, and an inverter circuit 4b which inverts the added output. The switching circuit 2' consists of a three-position switching circuit which has a muting position M as well as a
10 playing input position P and a recording input position R.

The recording/playing switching output from the switching circuit 1 is applied to the pre-amplifier 4a through a coupling capacitor C_1 . The output of the pre-amplifier 4a is applied to the recording position input
15 R of the switching circuit 2' through a coupling capacitor C_2 , whilst the output of the inverter circuit 4b is applied to the playing position input P of the switching circuit 2' through a coupling capacitor C_3 .

The output of the switching circuit 2' is applied
20 to the network 4c through a coupling capacitor C_4 , and also provides a playing output P_{OUT} . The output of the switching circuit 2' is also applied to a headphone amplifier 5 which provides a playing output P_{OUT}' through a coupling capacitor C_6 . The output of the inverter circuit

4b is applied to a recording amplifier 6 to provide a recording output R_{OUT} for a record head.

The operation of the above described noise reduction circuit is as follows.

5 When it is desired to record, the switching circuit 2' is set to the recording position R by the control circuit 7. A recording signal which is the output of the pre-amplifier 4a has added thereto an in-phase higher frequency signal which is formed through
10 the switching circuit 2' and the network 4c, and an output signal for recording with the higher frequency expanded is formed by means of the inverter circuit 4b.

 In the case where a playing signal thus recorded
15 is to be played, the switching circuit 2' is set at the playing position P by the control circuit 7. The expanded playing signal which is the output of the pre-amplifier 4a has added thereto an anti-phase higher frequency signal (resulting in a subtraction) which is
20 formed by means of the switching circuit 2' and the network 4c after the inversion by the inverter circuit 4b. At the output of the switching circuit 2', the playing signal with the high frequency compressed into the original level is obtained, and a high region

noise is compressed.

On the other hand, such switchable noise reduction system having the above described feedback network has been disclosed in detail in "Dolby B-Type Noise Reduction System", the SERT Journal, Vol 8, May/June 1974, pp. 99 - 103, by R. Berkovitz and K. Gundry. "Dolby" is a registered trade mark.

In the embodiment shown in Figure 2, the switching circuit 2' which forms part of the noise reduction circuit has three switching positions, one of which is provided with a muting function.

It is thus possible to achieve a simplification of the circuit arrangement and also to reduce the number of external terminals of the IC.

Furthermore, in order that the circuit 2' shall prevent the occurrence of the shock noise attributed to the switching of the switching circuit 1, a recording/playing switching signal R/P formed by the control circuit 7 is passed through a gate circuit G, to form a recording/playing switching signal for the switching circuit 2' and a mute signal M is used as a gate control signal in this case so that when the mute signal M is provided, the recording/playing switching signal may be inhibited to afford a preference to the muting operation.

Even when, in this manner, the switching circuit constituting the noise reduction circuit is provided with the muting function to reduce the number of external terminals in the fabrication of the monolithic IC while achieving the simplification of the circuit arrangement, it does not effect the functioning of the circuit in other respects.

Figure 3 shows a detailed circuit diagram of one preferred form of the switching circuit 2' as well as the control circuit 7.

As will be seen from Figure 3, the output sides of voltage follower circuits which are formed from a plurality of differential transistor circuits, are made common, and a plurality of emitter constant-current sources forming a plurality of differential transistors are selectively switched to operate only one set of differential transistors, whereby a switching operation is carried out.

More specifically, the outputs of the differential circuits, which are respectively formed by differential transistors Q_1 and Q_2 and an emitter constant-current source consisting of a transistor Q_{15} and a resistor R_6 , differential transistors Q_3 and Q_4 and an emitter constant-current source consisting of a

transistor Q_{16} and a resistor R_5 , and differential transistors Q_5 and Q_6 and an emitter constant-current source consisting of a transistor Q_{17} and a resistor R_4 , are all connected in common.

5 The differential circuits are provided with a load circuit which consists of a current mirror circuit comprising transistors Q_{13} and Q_{14} .

10 The output of the current mirror circuit is applied to an emitter follower circuit which consists of a transistor Q_{45} , level shift diodes Q_{19} and Q_{47} in the form of diode connected transistors, and a constant-current source I_0 . The output of the emitter follower is used to drive a complementary push-pull output circuit consisting of transistors Q_{46} and Q_{48} so as to
15 obtain an output.

 This output is negatively fed-back to the base electrodes of the transistors Q_2 , Q_4 and Q_6 which are the inverting input terminals of the differential transistor circuits.

20 The base electrodes of the transistors Q_1 , Q_3 and Q_5 which are the non-inverting inputs of the differential transistor circuits are supplied with a base bias voltage V_{B2} through resistors R_3 , R_2 and R_1 , respectively. The base electrode of the transistor Q_1

is supplied with only the bias voltage V_{B2} in order to use it as a mute position input, whereas the base electrodes of the transistors Q_5 and Q_3 are respectively associated with coupling capacitors C_3 and C_2 which are used as a playing position input P and a recording position input R respectively.

Differential transistors Q_{43} and Q_{44} , whose emitter electrodes are commoned, are supplied with a constant-current from a circuit I_0 . The constant current I_0 is selectively applied to diodes Q_{20} and Q_{21} in accordance with a recording/playing switching input R/P.

The diodes Q_{20} and Q_{21} are respectively provided with series resistors R_8 and R_9 , to constitute current mirror circuits with the transistors Q_{17} and Q_{16} respectively.

Upon switching "on" the respective differential transistors Q_{43} and Q_{44} , the appropriate current mirror circuit operates to turn "on" either the differential transistors Q_3 and Q_4 or the differential transistors Q_5 and Q_6 , whereby circuit is switched to either the recording or the playing mode respectively.

Differential transistors Q_{41} and Q_{42} , whose emitter electrodes are commoned, are supplied with a

constant-current from a circuit I_o . This circuit generates a voltage across a diode Q_{18} and a resistor R_7 in response to the "on" output of the transistor Q_{17} which is turned "on" by the mute position input M.

5 This voltage drives the transistor Q_{15} to operate the differential transistors Q_1 and Q_2 which constitute the mute position. The voltage across the diode Q_{18} and the resistor R_7 also turns "on" transistors $Q_{22} - Q_{24}$, and thus render the respective current source circuits of
10 the differential transistors Q_3 and Q_4 and the differential transistors Q_5 and Q_6 of the recording and playing positions to be ineffective. The differential transistors Q_{41} and Q_{42} thus form a bias circuit of constant input current, to effect the muting operation
15 based on the muting position input signal M irrespective of the recording/playing switching signal R/P.

Diodes $Q_7 - Q_{12}$ which are respectively arranged at the emitter electrodes of the differential transistors $Q_1 - Q_6$ are provided to prevent the counter
20 flows of the input signals of the transistors Q_3 and Q_5 in the "off" states to the other positions. They prevent the counter flows due to the reverse breakdown across the base and emitter electrodes of the transistors, but they are unnecessary when signal

amplitudes are small.

Figure 4 shows a detailed circuit diagram of a second preferred form of the switching circuit 2' as well as the control circuit 7.

5 All circuit elements inside a broken line IC are constructed within a monolithic semiconductor integrated circuit. Symbols a - k enclosed with circles indicate external terminals of the monolithic semiconductor integrated circuit.

10 During recording, a control signal R/P which is applied to the external terminal h is at a high level, and a mute control signal M which is applied to the external terminal i is also at the high level.

Accordingly, transistors Q_{27} , Q_{43} and Q_{42} of
15 the control circuit 7 turn "off", whereas the other transistors Q_{28} , Q_{44} and Q_{41} turn "on".

Accordingly, a transistor Q_{30} of the switching circuit 1 is switched to the "on" state and a transistor Q_{35} is switched to the "off" state. A
20 transistor Q_{16} of the switching circuit 2' is switched to the "on" state and transistors Q_{15} and Q_{17} are switched to the "off" states.

which
A recording signal R_{IN} is applied to the external terminal a, is transmitted to the external

terminal c through transistors Q_{31} and Q_{32} , diodes Q_{33} and Q_{34} and emitter follower transistors Q_{49} and Q_{50} .

The recording signal R_{IN} which is transmitted to the external terminal c, is applied to the expander/compressor 4 through a coupling capacitor C_1 . The output signal from the pre-amplifier 4a is applied to the external terminal e through a coupling capacitor C_2 , and an output signal from the inverter circuit 4b is applied to the external terminal f through a coupling capacitor C_3 .

During the recording, the transistor Q_{16} of the switching circuit 2' is in the "on" state and the transistors Q_{17} and Q_{15} are in the "off" state, so that only the output signal of the pre-amplifier 4a which is applied to the external terminal e, is applied to the network 4c of the expander/compressor 4 through the transistors Q_3 and Q_4 , diodes Q_9 and Q_{10} , a current mirror circuit consisting of transistors Q_{13} and Q_{14} , an emitter follower transistor Q_{45} , a complementary push-pull output circuit consisting of transistors Q_{46} and Q_{48} , the external terminal g and a coupling capacitor C_4 .

Thus, a higher frequency signal formed through the switching circuit 2' and the network 4c is added to the recording signal of the pre-amplifier 4a,

and a signal for recording with the higher frequency expanded can be provided from the output of the inverter circuit 4b.

During playing, the control signal R/P which is applied to the external terminal h is at a low level, and the mute control signal M which is applied to the external terminal i is at the high level. Accordingly, the transistors Q_{28} , Q_{44} and Q_{42} of the control circuit 7 turn "off", whereas the other transistors Q_{27} , Q_{43} and Q_{41} turn "on".

Consequently, the transistor Q_{35} of the switching circuit 1 is switched to the "on" state and the transistor Q_{30} is switched to the "off" state, and the transistor Q_{17} of the other switching circuit 2' is switched to the "on" state and the transistors Q_{15} and Q_{16} are switched to the "off" states.

A playing signal P_{IN} , which is applied to the external terminal b, is transmitted to the external terminal c through transistors Q_{36} and Q_{37} , diodes Q_{38} and Q_{39} and emitter follower transistors Q_{49} and Q_{50} .

The playing signal P_{IN} transmitted to the external terminal c is applied to the expander/compressor 4 through the coupling capacitor C_1 . Further, the output signal of the pre-amplifier 4a is applied to the

external terminal e through the coupling capacitor C_2 , and the output signal of the inverter circuit 4b is applied to the external terminal f through the coupling capacitor C_3 .

5 During playing, the transistor Q_{17} of the switching circuit 2' is in the "on" state and the transistors Q_{15} and Q_{16} are in the "off" states. Hence, only the output signal of the inverter circuit 4b, which is applied to the external terminal f, is applied to the
10 network 4c of the expander/compressor 4 through transistors Q_5 and Q_6 , diodes Q_{11} and Q_{12} , the current mirror circuit Q_{13} and Q_{14} , the emitter follower transistor Q_{45} , the complementary push-pull output circuit Q_{46} and Q_{48} , the output terminal g and the
15 coupling capacitor C_4 .

 Thus, an anti-phase higher frequency signal formed through the switching circuit 2' and the network 4c after inversion by the inverter circuit 4b is added to the playing signal of the pre-amplifier 4a
20 and the playing signal with its higher frequency compressed into the original level can be obtained at the output of the switching circuit 2' at the output terminal g.

 During the muting operation, the mute control

signal M which is applied to the external terminal i is at a low level, and hence, the transistor Q_{41} of the control circuit 7 turns "off" and transistors Q_{42} , Q_{22} , Q_{23} and Q_{24} turn "on".

5 As a result, the transistor Q_{15} of the switching circuit 2' is switched to the "on" state and the transistors Q_{16} and Q_{17} are switched to the "off" state, so that the respective signal components applied to both the external terminals e and f are inhibited
10 from being transmitted to the external terminal g.



CLAIMS.

1. A recording/playing circuit including:

(a) a noise reduction circuit in the form of an expander/compressor having a preamplifier, a combining network, an inverter circuit and a network for deriving
5 only a high frequency signal;

(b) a first switching circuit which includes first, second and third input positions and an output terminal, wherein said first input position is coupled to an output of said pre-amplifier of said expander/
10 compressor, said second input position is coupled to an output of said inverter circuit of said expander/
compressor, said output terminal is coupled to said high frequency signal deriving network of said expander/
compressor and said third input position is provided to
15 perform a muting function; and

(c) a control circuit which serves to transmit to said output terminal of said switching circuit selectively one of electric signals applied to said first, second and third input positions of said
20 switching circuit.

2. A recording/playing circuit according to Claim 1, wherein a recording/playing switching control signal and a mute control signal are applied to said control circuit.

25 3. A recording/playing circuit according to Claim 2, further including a gate circuit with which, when said



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third input position is selected by the application of said mute control signal, said switching circuit is inhibited from being set to said first or second input position by said recording/playing switching signal.

- 5 4. A recording/playing circuit according to any one of the preceding claims, further including a second switching circuit which serves to transmit selectively either a recording signal or a playing signal to said pre-amplifier of said expander/compressor.
- 10 5. A recording/playing circuit according to any one of the preceding claims, wherein said first switching circuit comprising:
- (a) a first differential pair of transistors;
 - (b) a second differential pair of transistors;
 - 15 (c) a third differential pair of transistors;
 - (d) a first current source transistor which is coupled in common to the emitter electrodes of said first differential pair of transistors;
 - (e) a second current source transistor which
 - 20 is coupled in common to the emitter electrodes of said second differential pair of transistors;
 - (f) a third current source transistor which is coupled in common to the emitter electrodes of said third differential pair of transistors;

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(g) a load circuit which is coupled in common to said first, second and third differential pairs of transistors; and

(h) an emitter follower circuit which is arranged between said load circuit and said output terminal of said first switching circuit;

6. A recording/playing circuit according to Claim 5, wherein: a bias voltage is connected in common to the base electrodes of said first, second and third differential pairs of transistors on one side; a voltage of said output terminal of said switching circuit is applied in a negative feedback voltage to the base electrodes of said first, second and third differential pairs of transistors on the other side; the base electrode of said first differential pair of transistors on said one side is connected to said first input position; the base electrode of said second differential pair of transistors on said one side is connected to said second input position; the base electrode of said third differential pair of transistors on said one side is connected to said third input position; and one of said first, second and third current source transistors is selectively rendered conductive by said control circuit.



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7. A recording/playing circuit according to Claim 4, or either Claim 5 or 6 as dependent on Claim 4, wherein said second switching circuit comprises:

- (a) a first differential pair of transistors;
- 5 (b) a second differential pair of transistors;
- (c) a first current source transistor which is coupled in common to the emitter electrodes of said first differential pair of transistors;
- (d) a second current source transistor which
10 is coupled in common to the emitter electrodes of said second differential pair of transistors;
- (e) a load circuit which is coupled in common to said first and second differential pairs of transistors; and
- 15 (f) an emitter follower circuit which is arranged between said load circuit and said pre-amplifier of said expander/compressor.

8. A recording/playing circuit according to Claim 7, wherein: the recording signal is applied to a base
20 electrode of one of said first differential pair of transistors; the playing signal is applied to a base electrode of one of said second differential pair of transistors; and either the first or the second current source transistors is selectively rendered conductive by said control circuit.



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9. A recording/playing circuit constructed and arranged to operate substantially as herein described with reference to and as shown in Figures 2 and 3 or Figure 4 of the accompanying drawings.

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