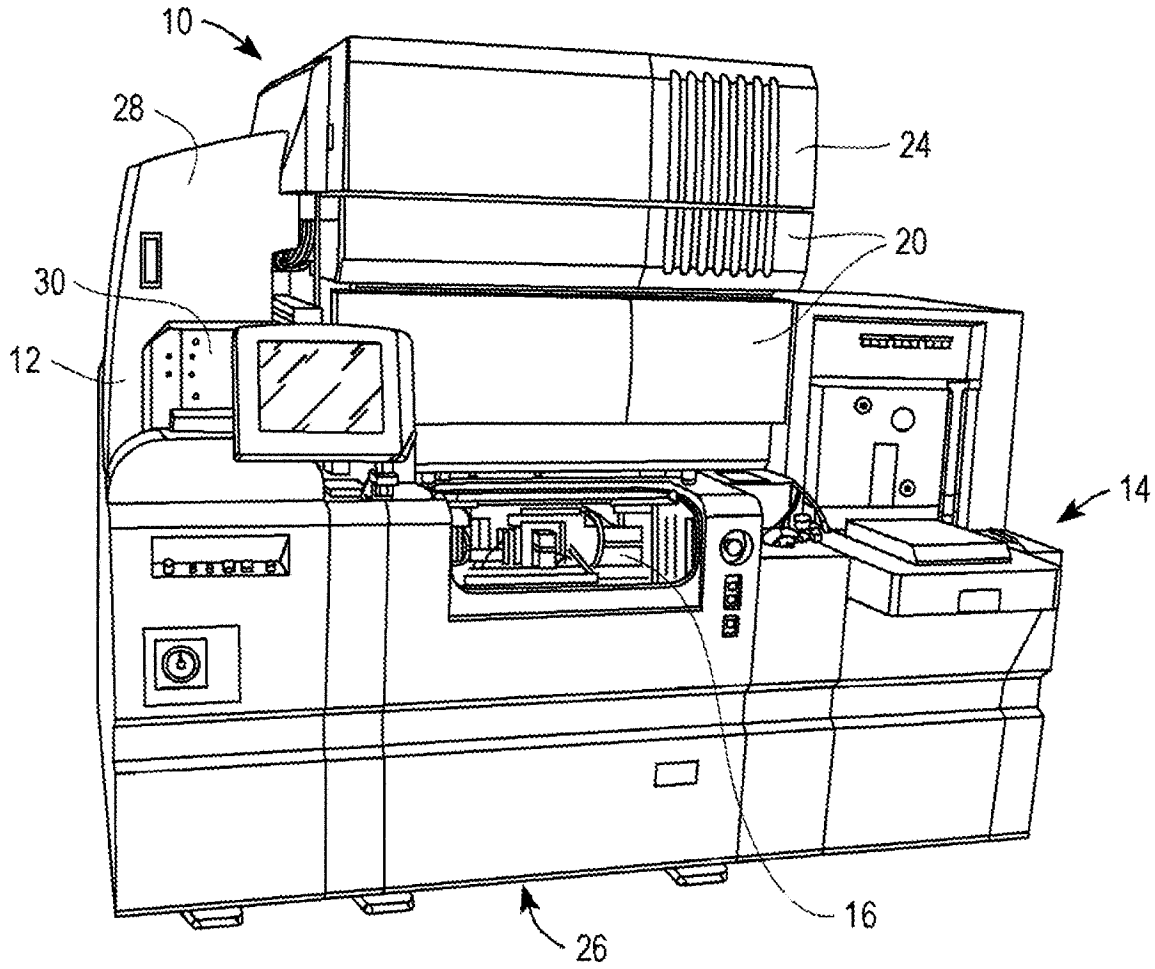

FIG. 1

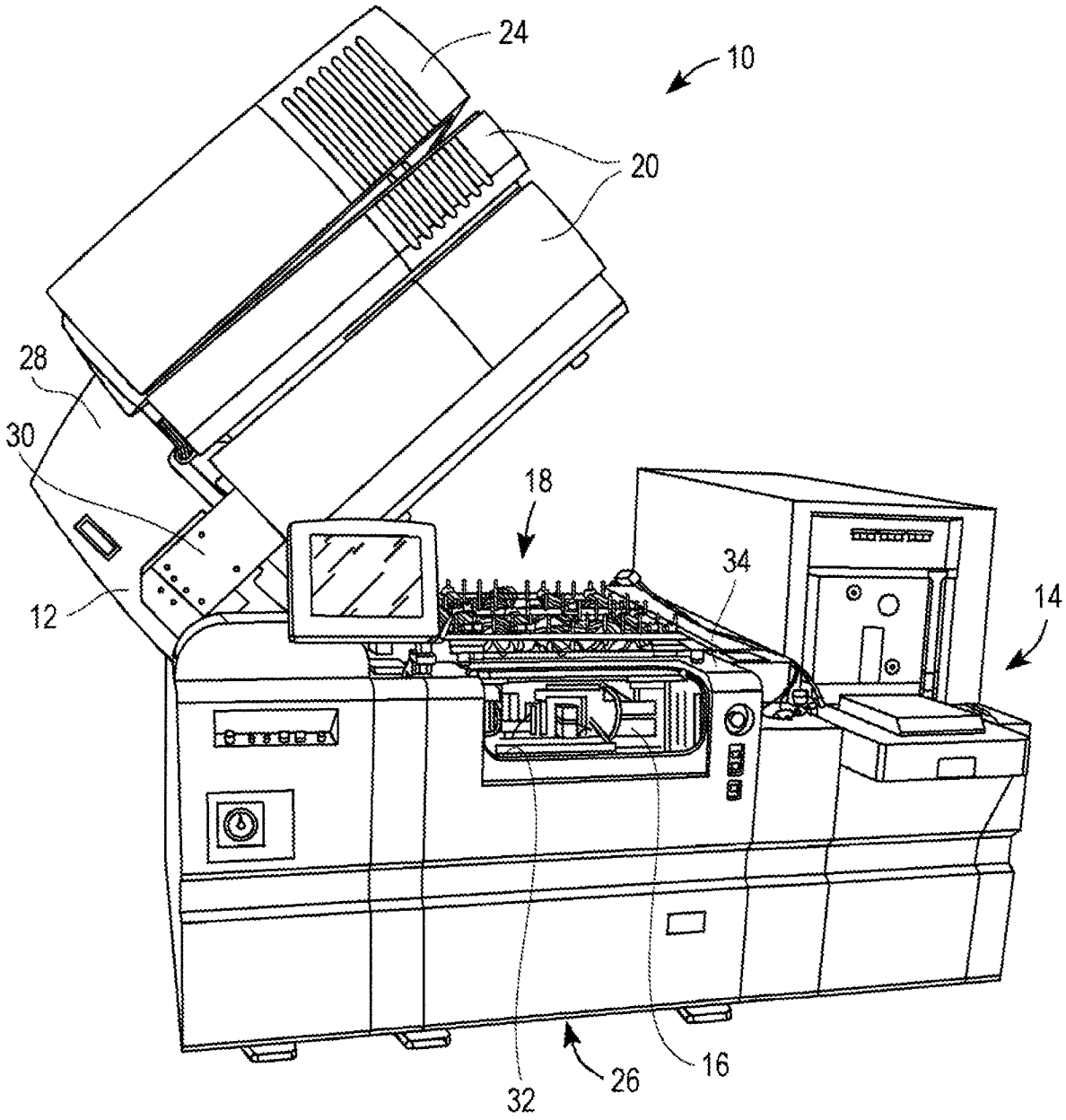

FIG. 2

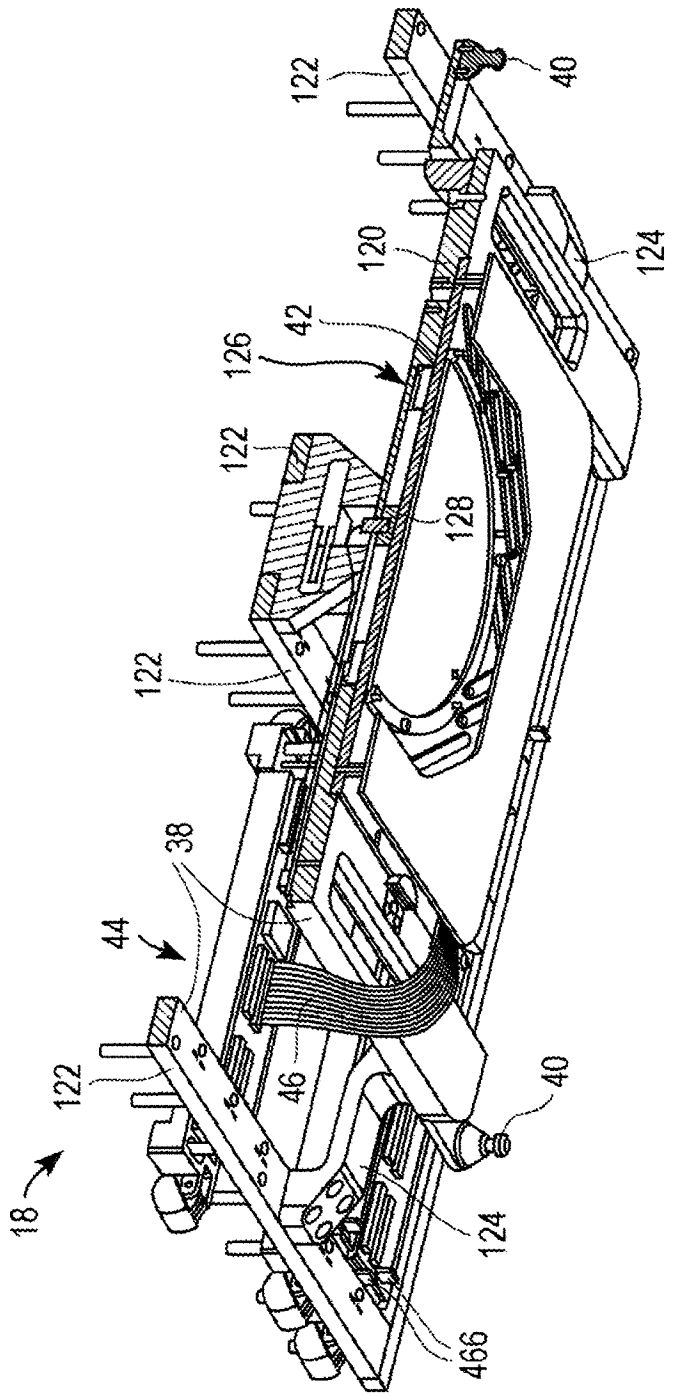

FIG. 3

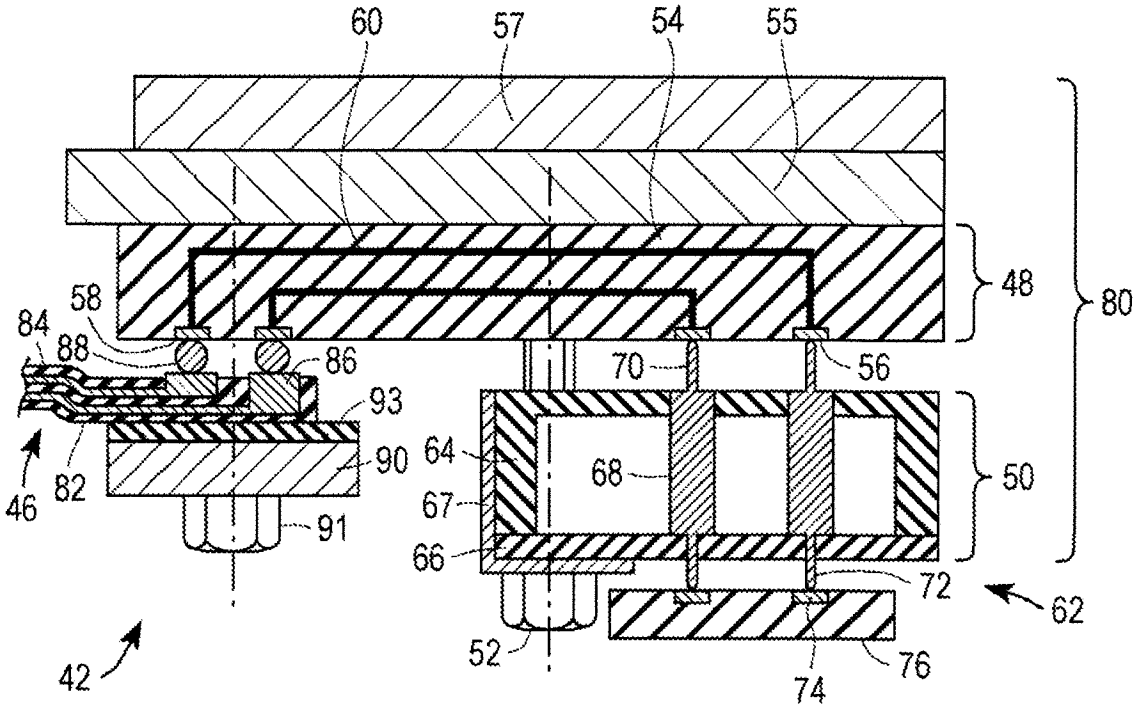
60
57
54
55
48
80
58
84
88
86
70
56
93
64
68
50
90
67
82
46
91
66
72
62
42
52
74
76

FIG. 4

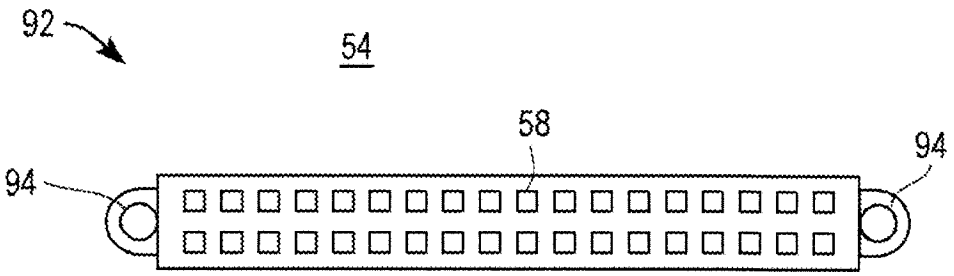
92
54
58
94
94

FIG. 5

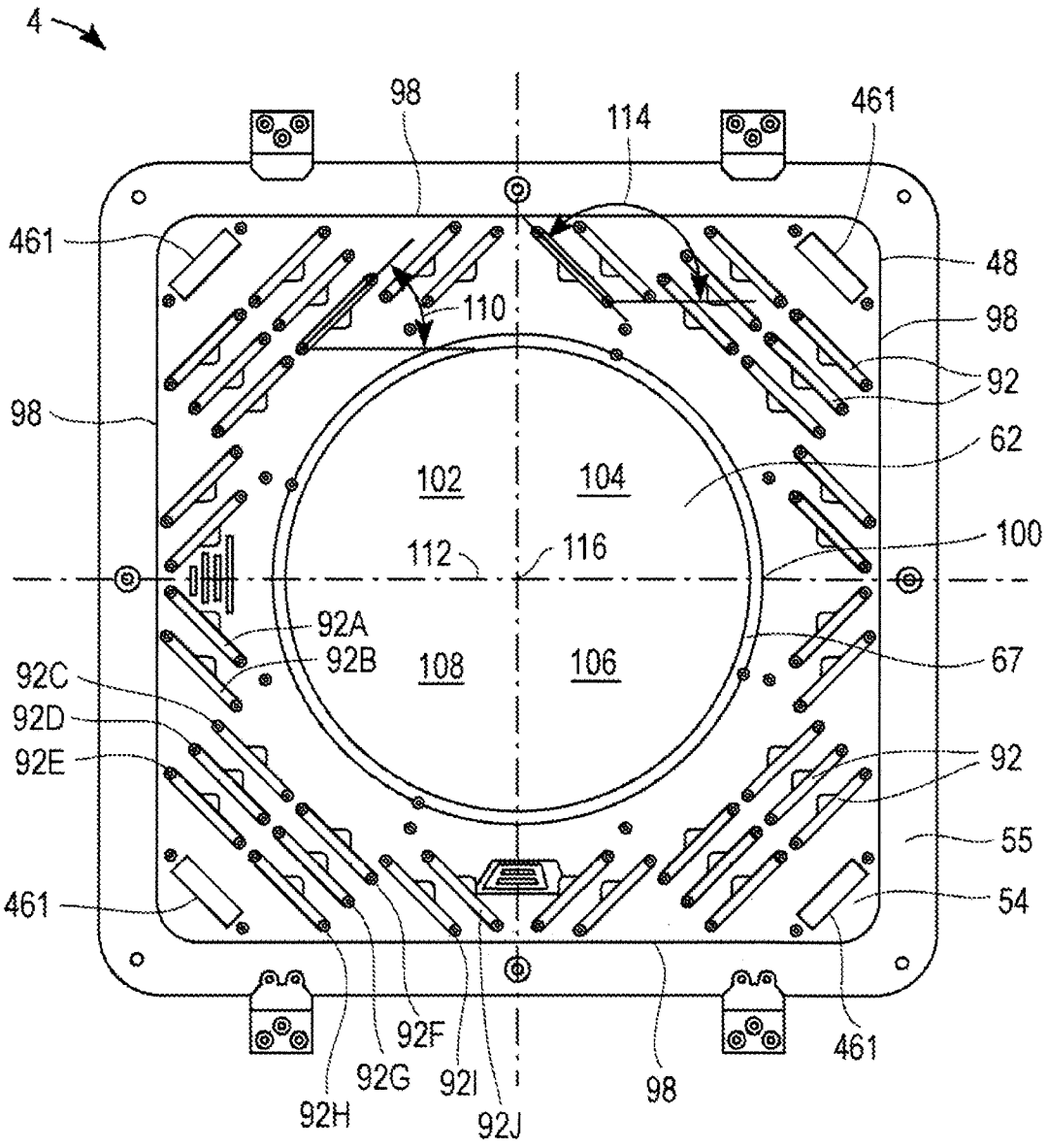
4
98
114
461
461
48
110
98
92
98
62
102
104
100
112
116
92A
92B
108
106
67
92C
92D
92E
92
55
461
54
92F
92G
92I
92J
98
461
92H

FIG. 6

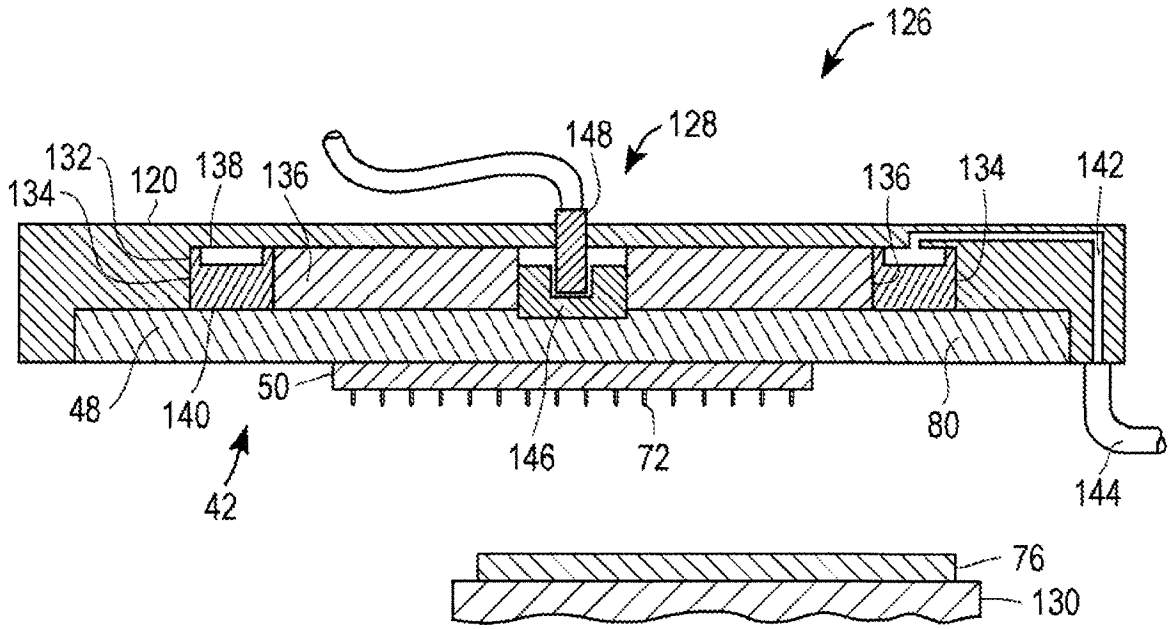
126
128
148
132
120
138
136
134
136
134
142
48
140
50
146
72
80
144
42
76
130

FIG. 7

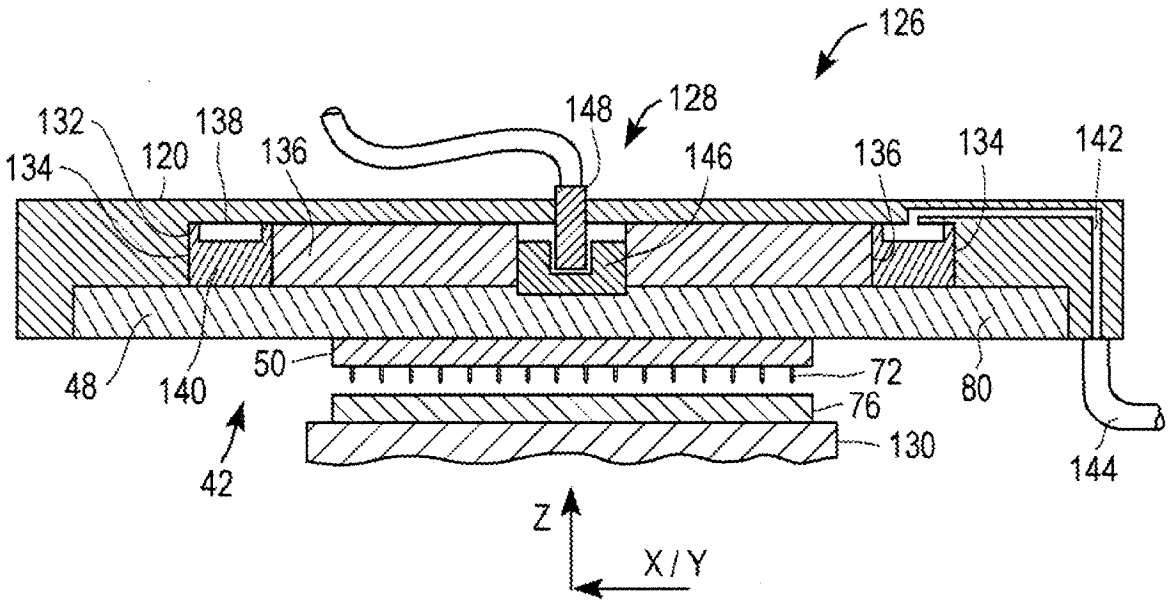
126
128
148
132
138
120
136
134
146
136
134
142
48
140
50
72
80
76
130
144
42
Z
X / Y

FIG. 8

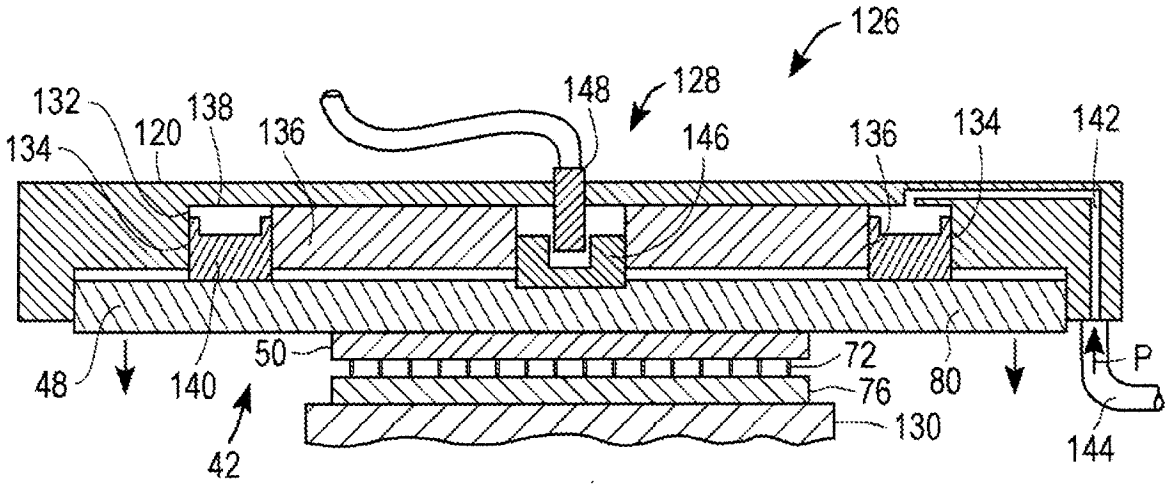
126
128
148
132
120
138
136
146
136
134
142
134
48
140
50
72
76
80
P
130
42
144

FIG. 9

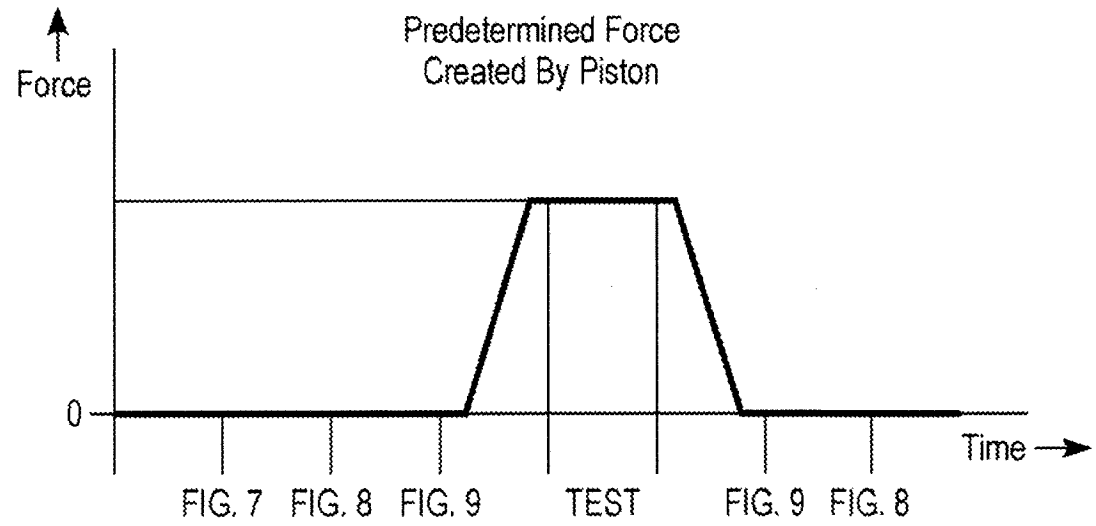
Predetermined Force
Created By Piston
Force
0
Time
FIG. 7
FIG. 8
FIG. 9
TEST
FIG. 9
FIG. 8

FIG. 10

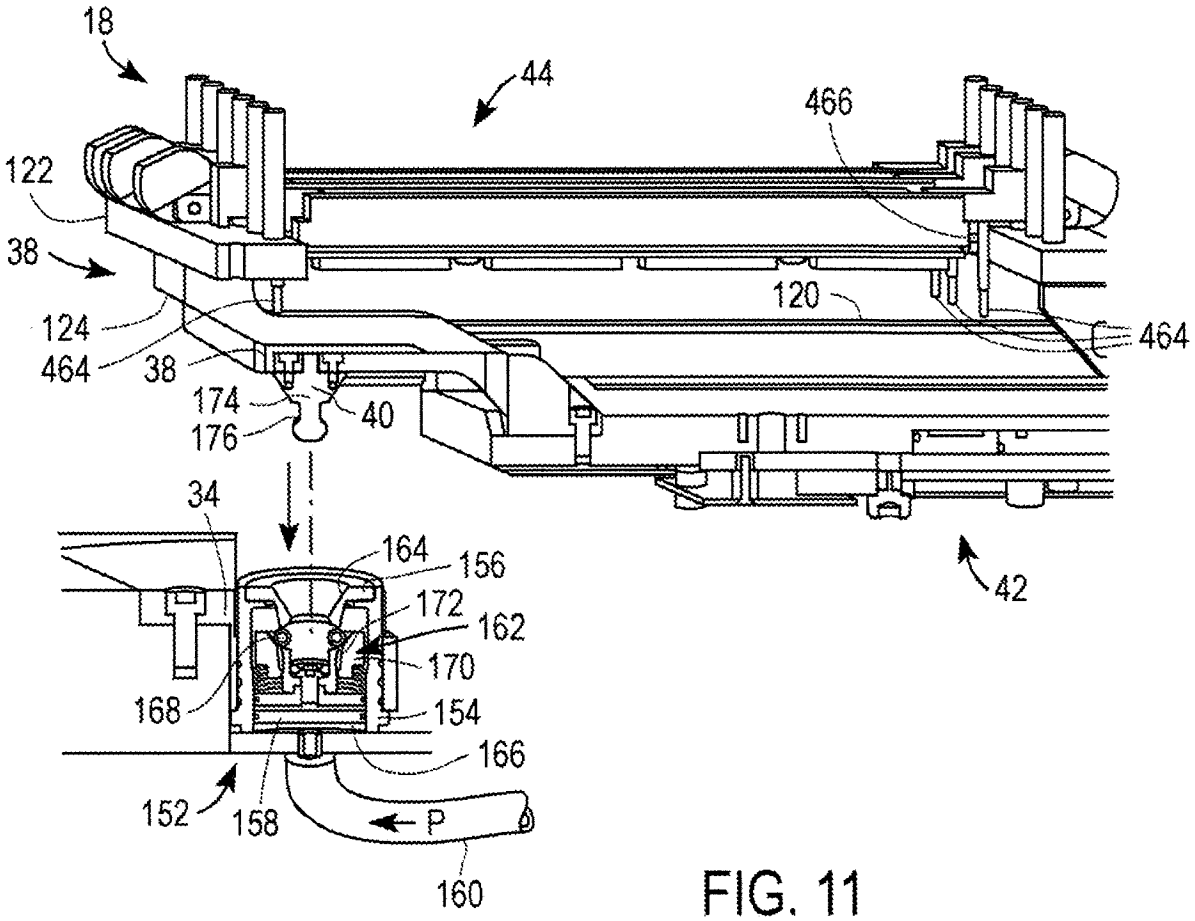
18
44
466
122
38
120
464
124
464
38
174
176
40
34
164
156
172
162
170
168
154
166
152
158
P
160
42

FIG. 11

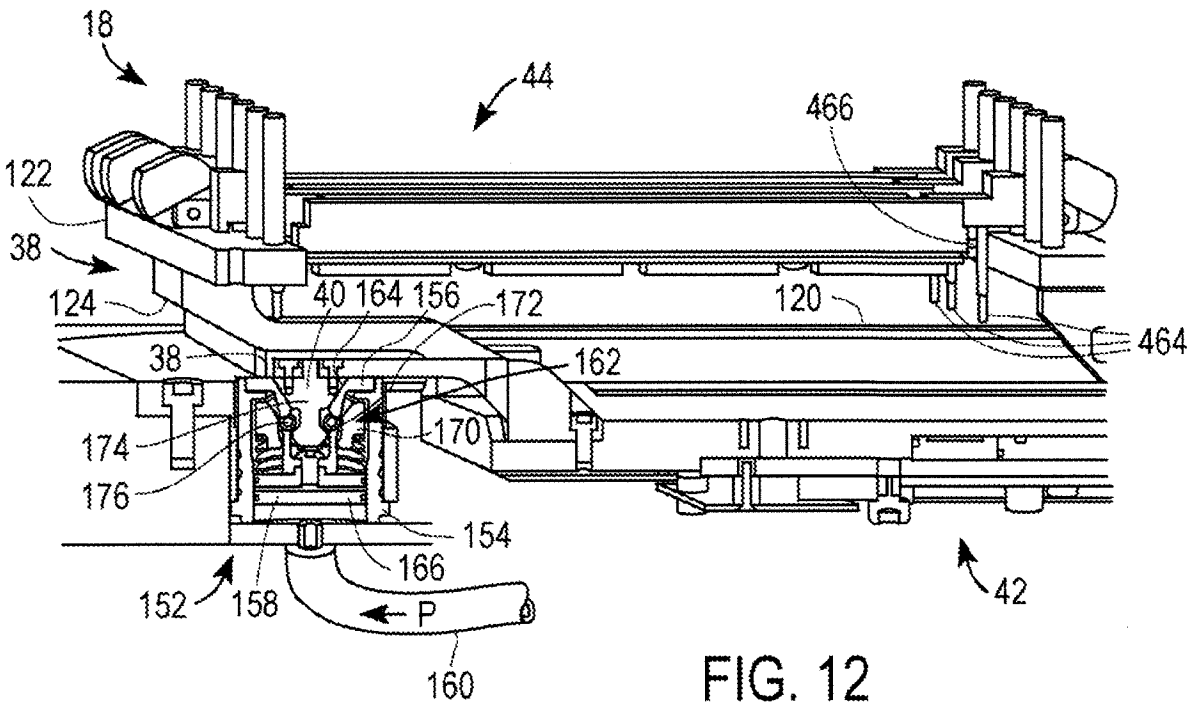
18
44
466
122
38
40 164 156
172
120
464
124
38
162
174
170
176
154
166
152
158
P
160
42

FIG. 12

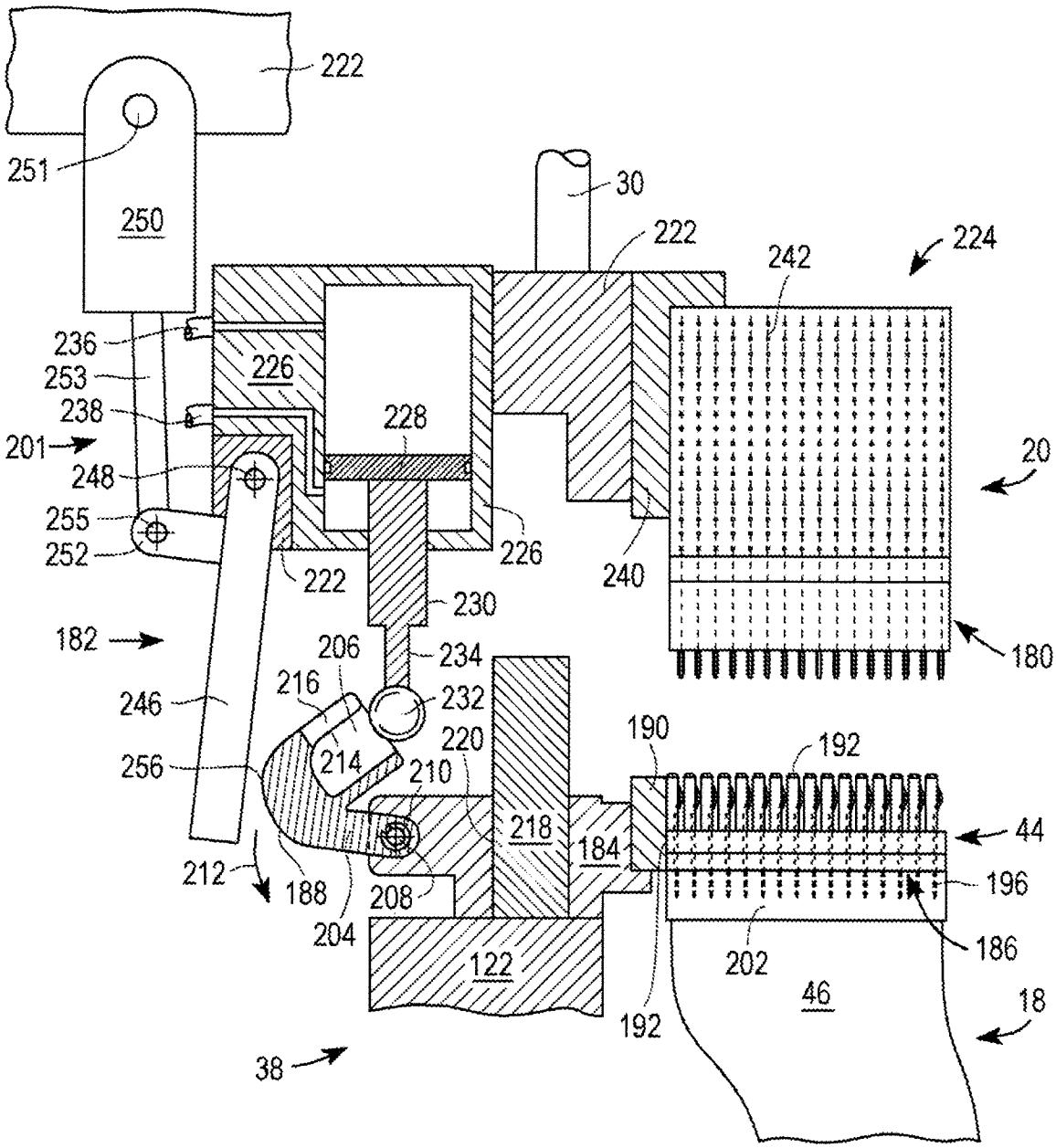
222
251
250
30
222
242
224
236
253
238
226
228
201
248
255
252
222
226
240
20
230
182
206
234
216
232
246
256
214
210
220
190
192
218
184
44
212
188
208
204
196
186
202
122
46
192
18
38
180

FIG. 13

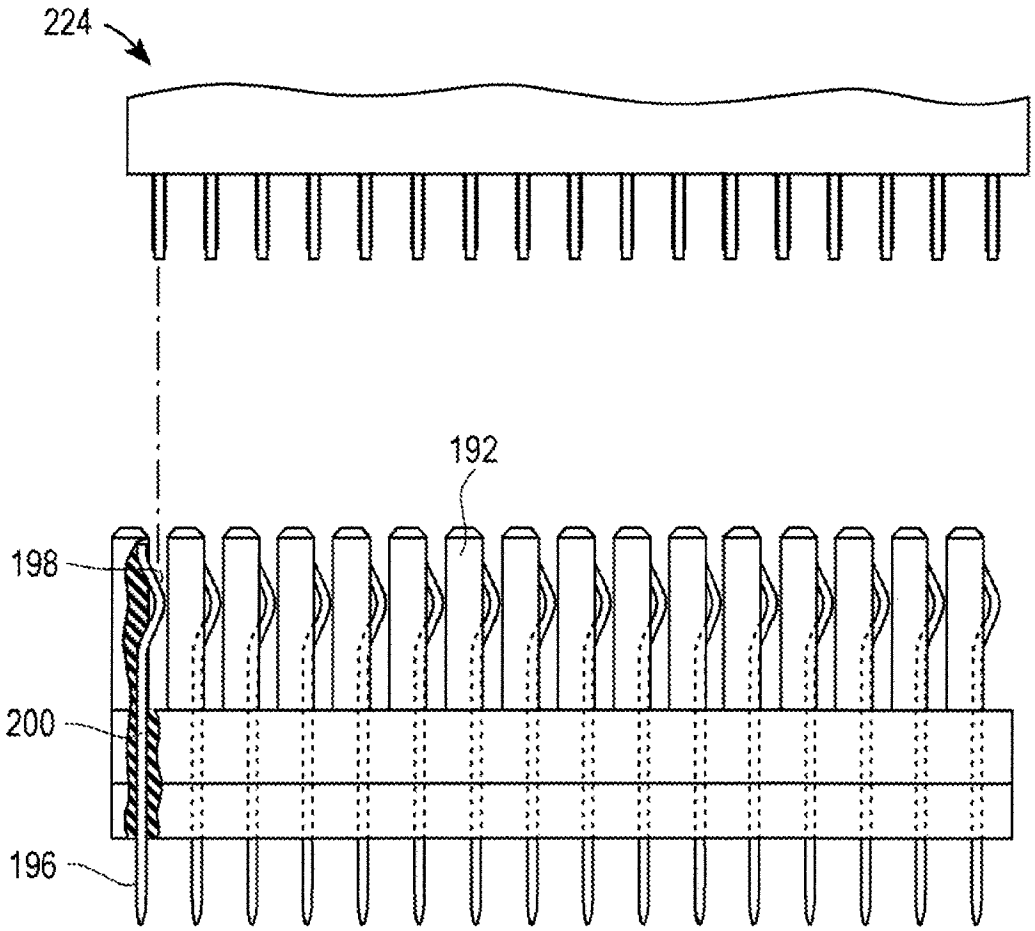

FIG. 14

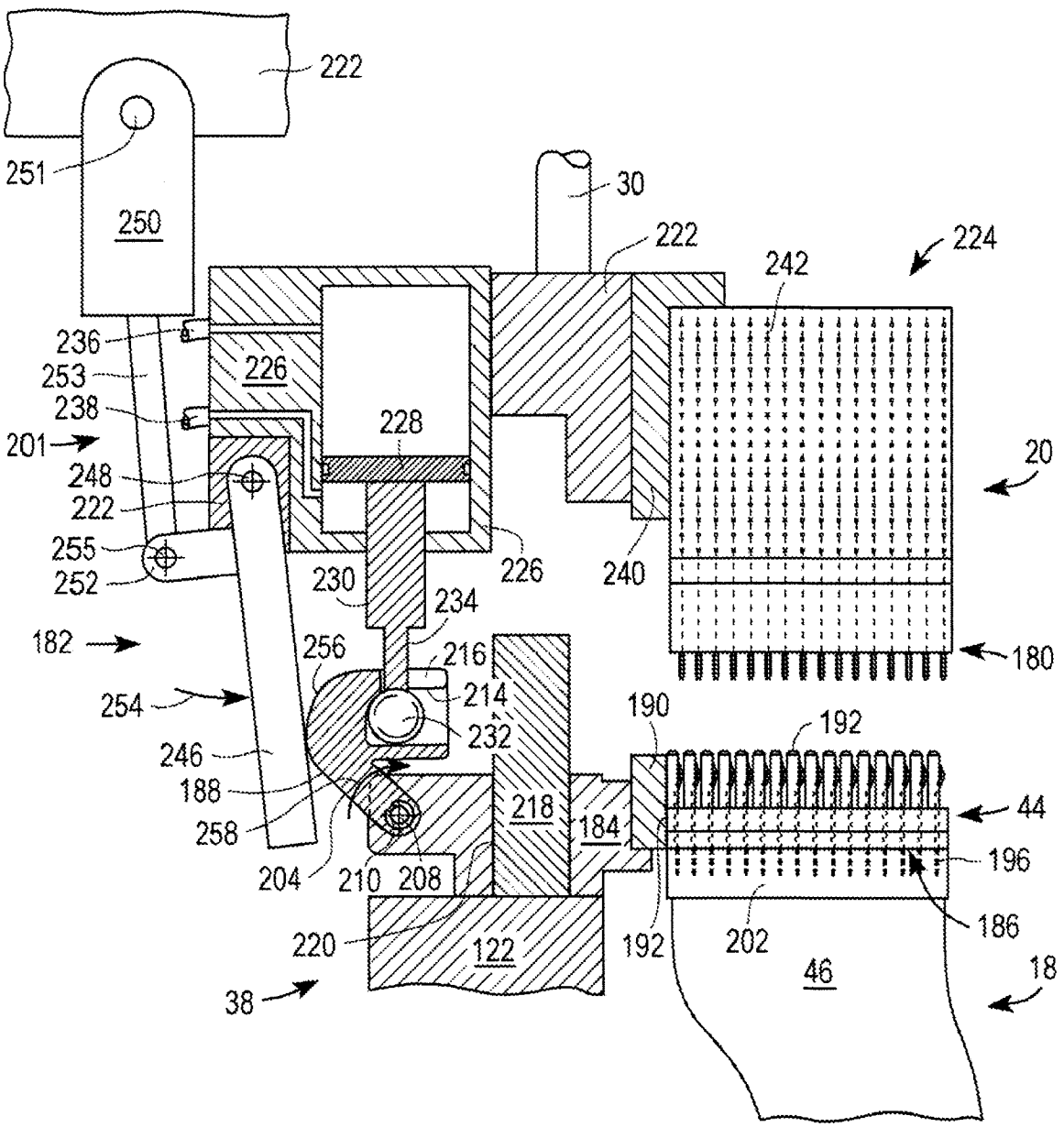
222
251
250
30
222
224
242
236
253
238
226
228
201
248
222
255
252
230
226
240
20
234
182
256
216
214
254
232
190
192
246
188
218
184
44
258
204
210
208
196
186
220
122
192
202
46
18
38

FIG. 15

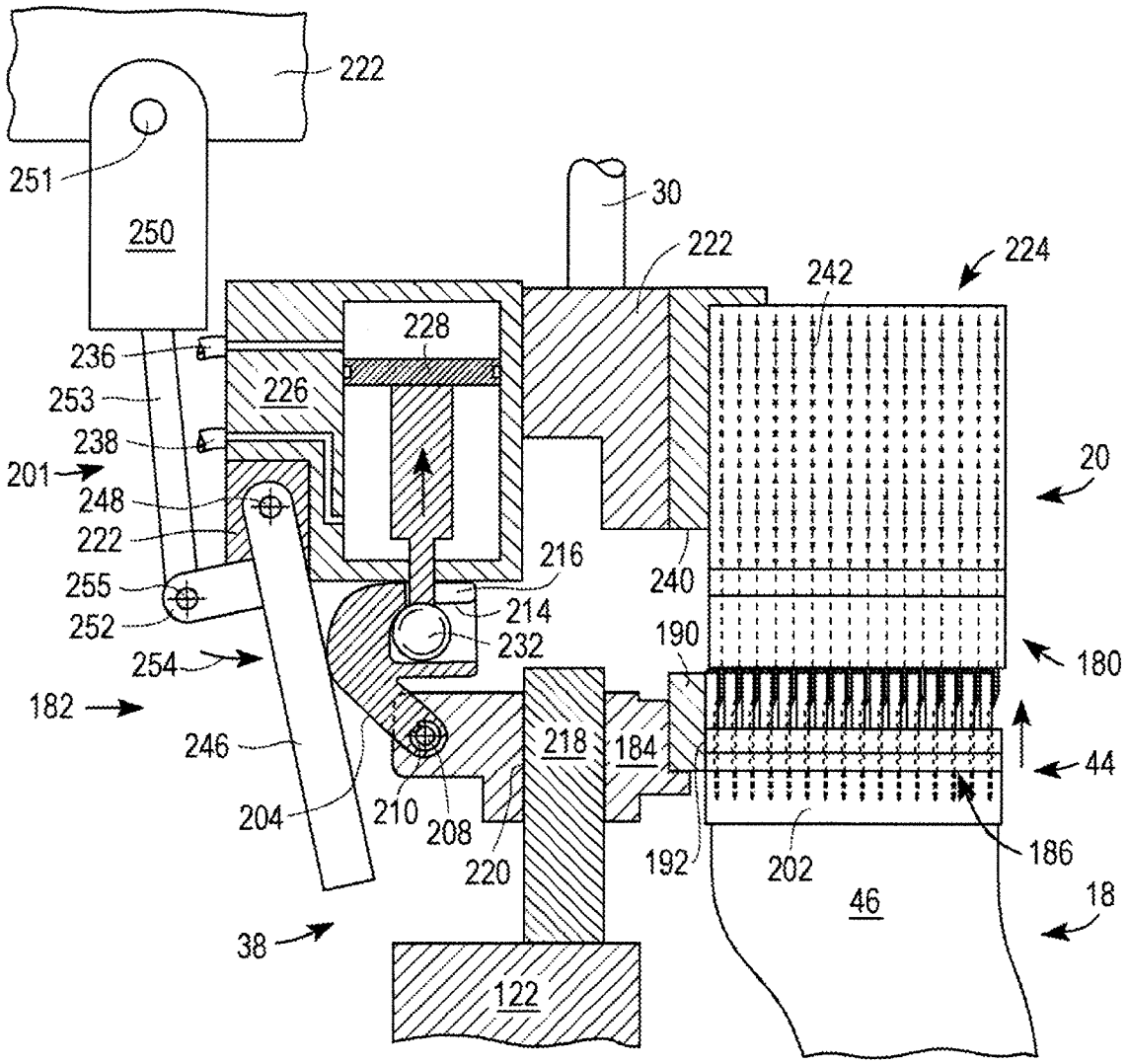
222
251
250
30
222
224
242
228
236
226
253
238
201
248
222
255
252
254
182
246
204
210
208
220
216
214
232
240
190
180
20
44
218
184
186
192
202
46
18
38
122

FIG. 16

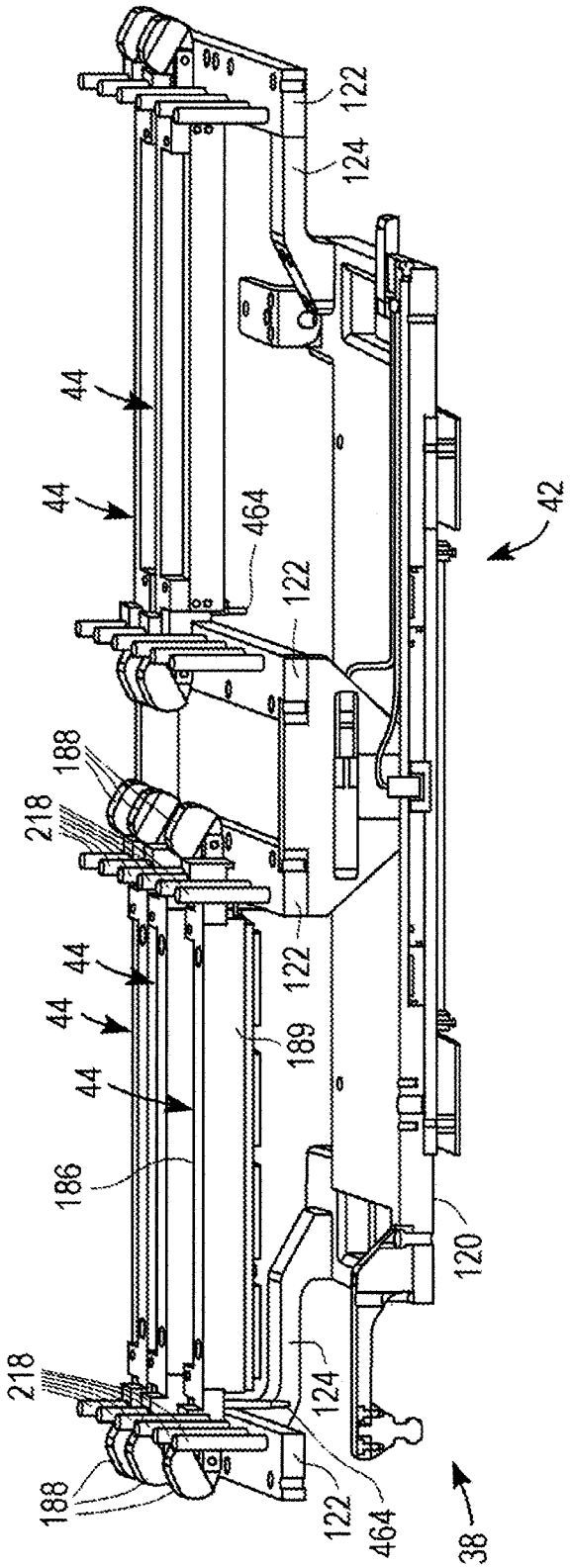
122
124
44
44
464
122
42
188
218
122
44
44
44
189
186
120
218
124
188
122
464
38

FIG. 17

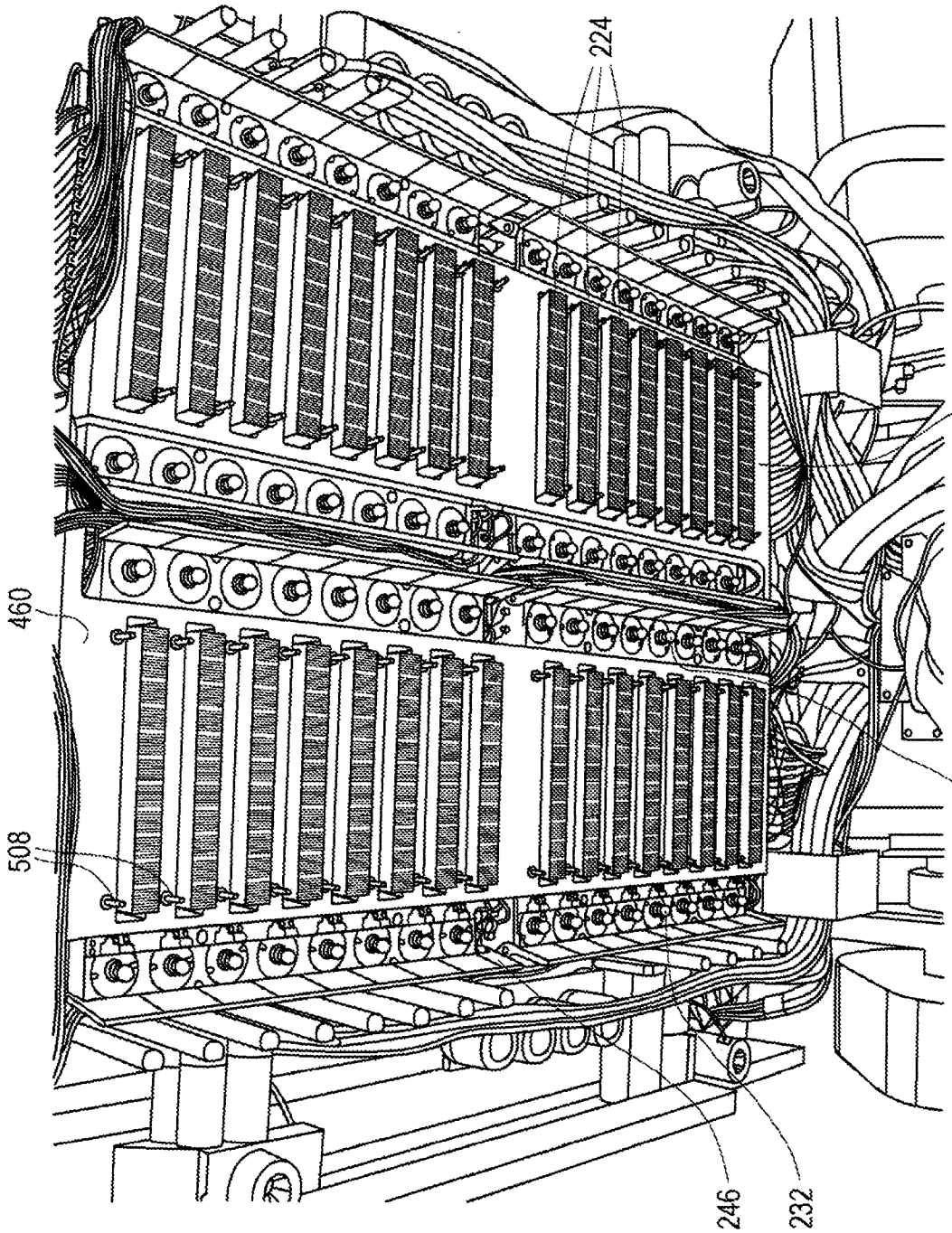

FIG. 18

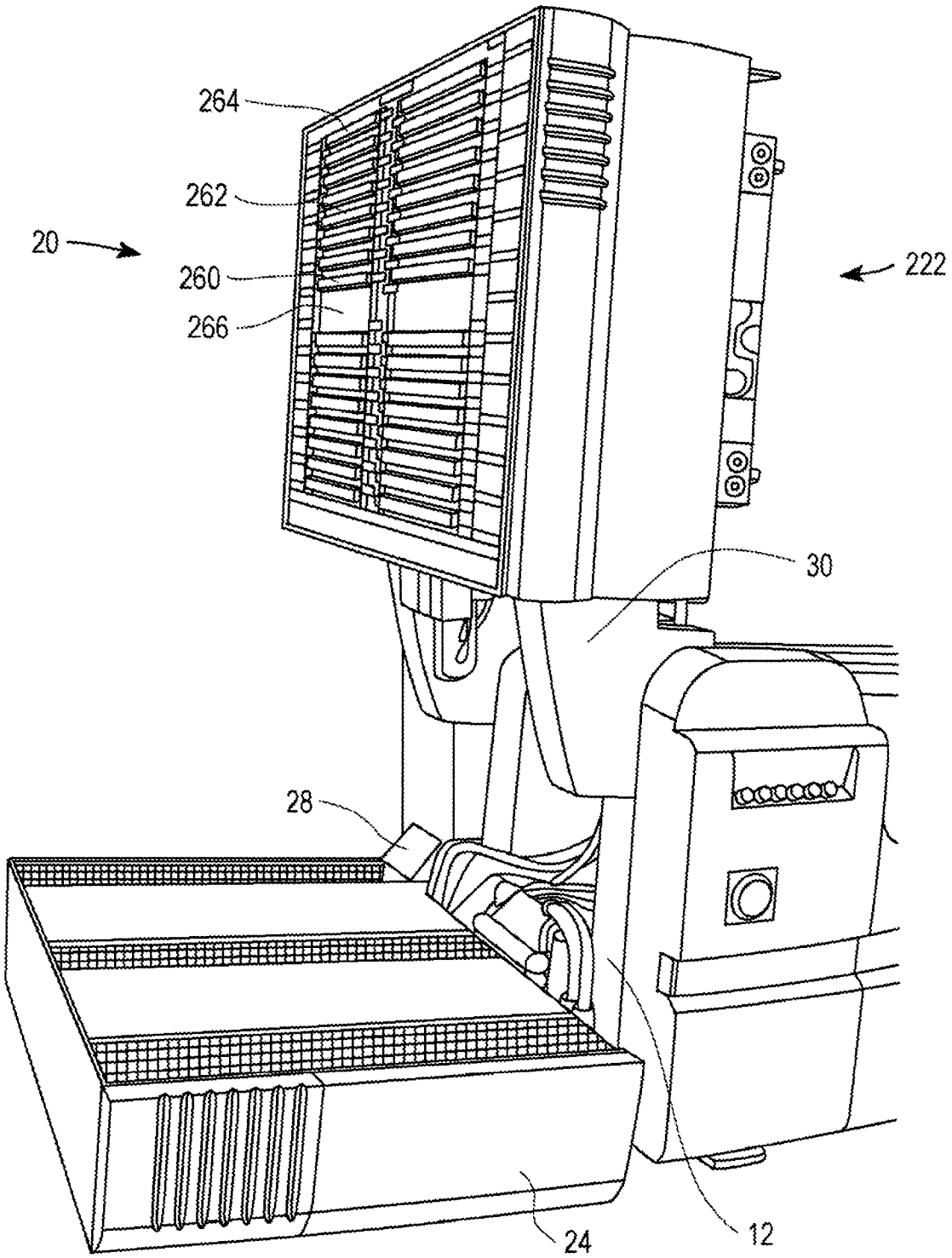

FIG. 19

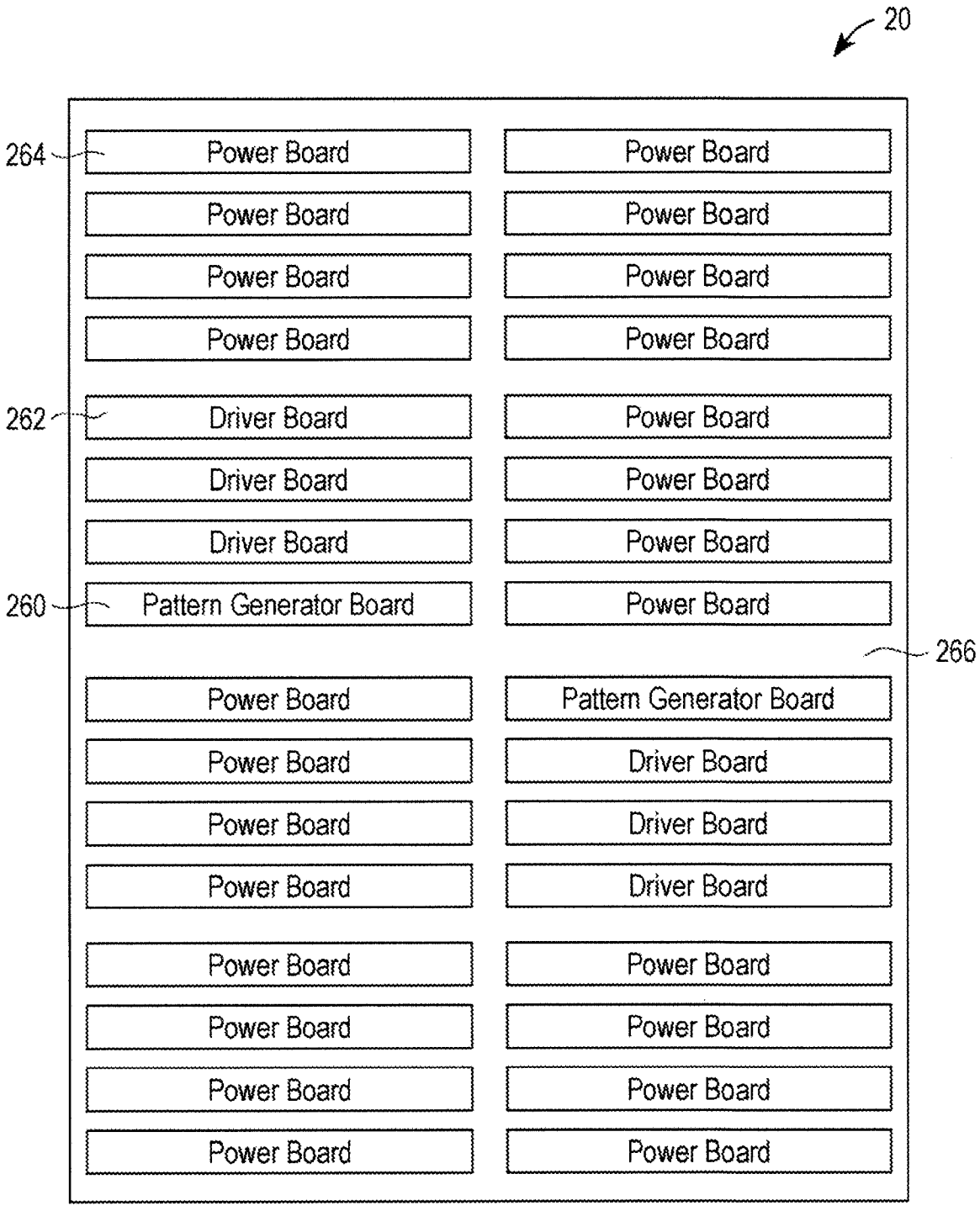
20
264
262
260
266
Power Board
Driver Board
Pattern Generator Board

FIG. 20

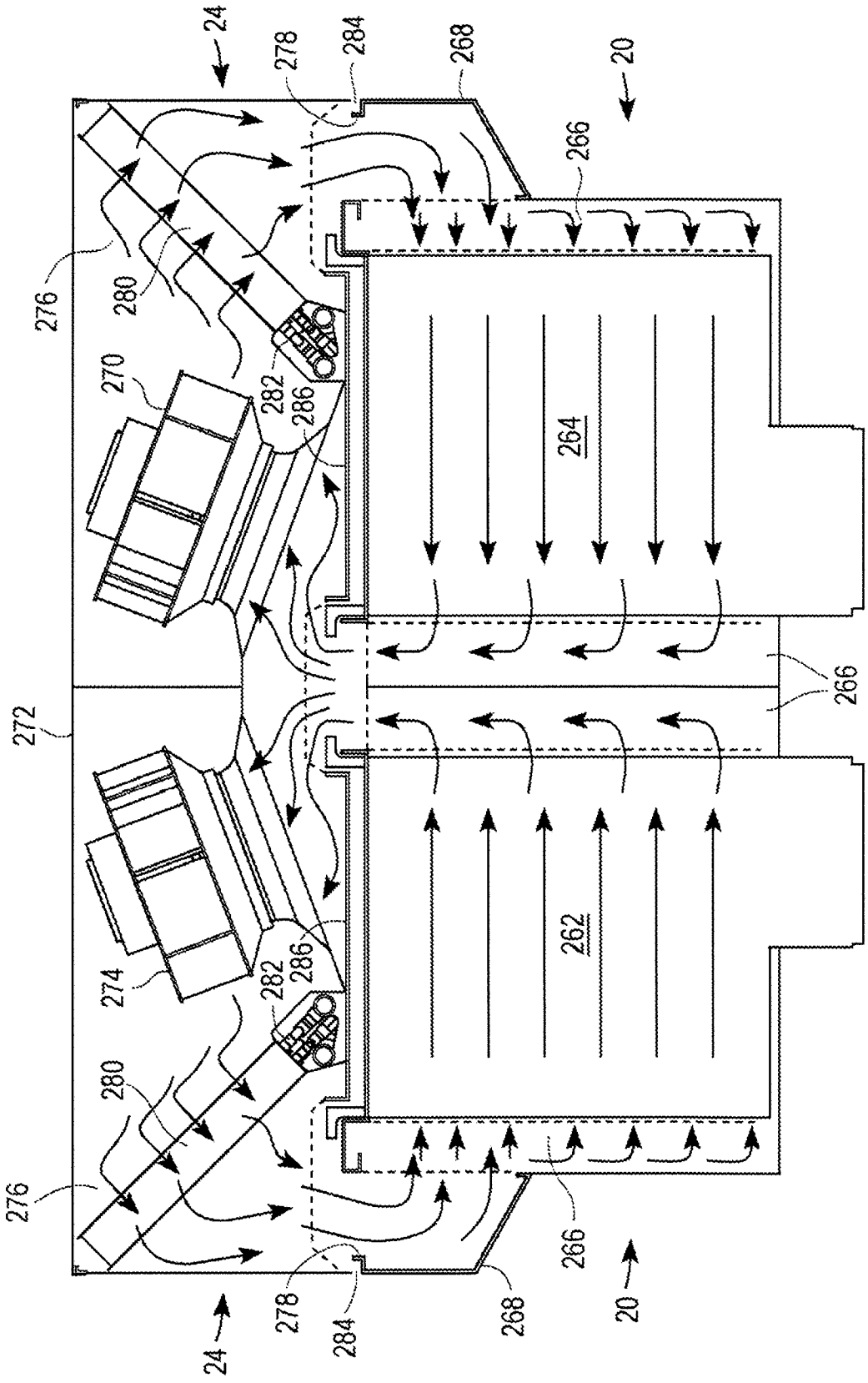
24
278
284
268
20
266
276
280
270
282
286
264
272
274
262
24
278
284
268
20
266

FIG. 21

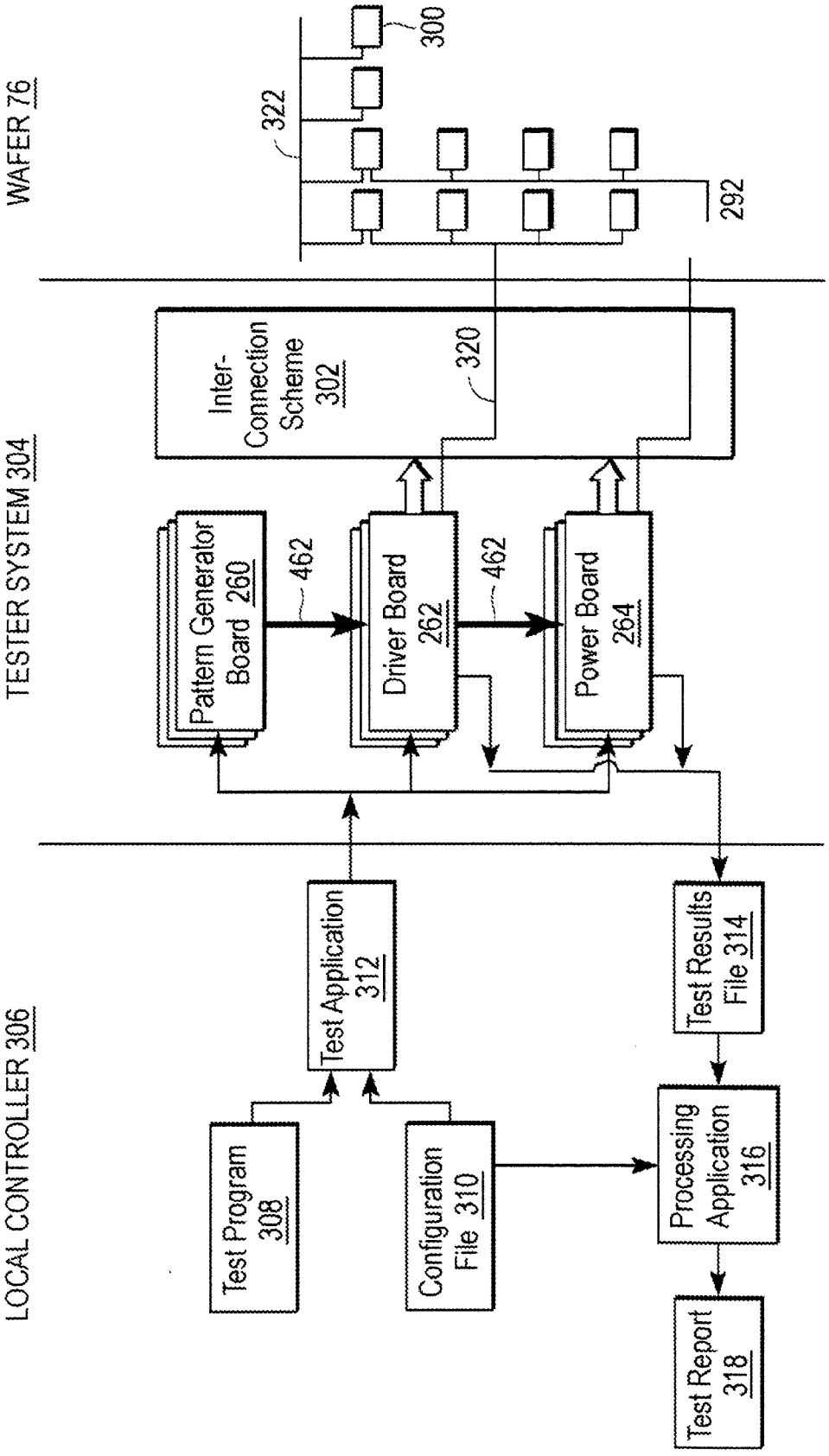
WAFER 76
TESTER SYSTEM 304
LOCAL CONTROLLER 306
300
322
292
Inter-Connection Scheme 302
320
Pattern Generator Board 260
462
Driver Board 262
462
Power Board 264
Test Application 312
Test Program 308
Configuration File 310
Test Results File 314
Processing Application 316
Test Report 318

FIG. 22

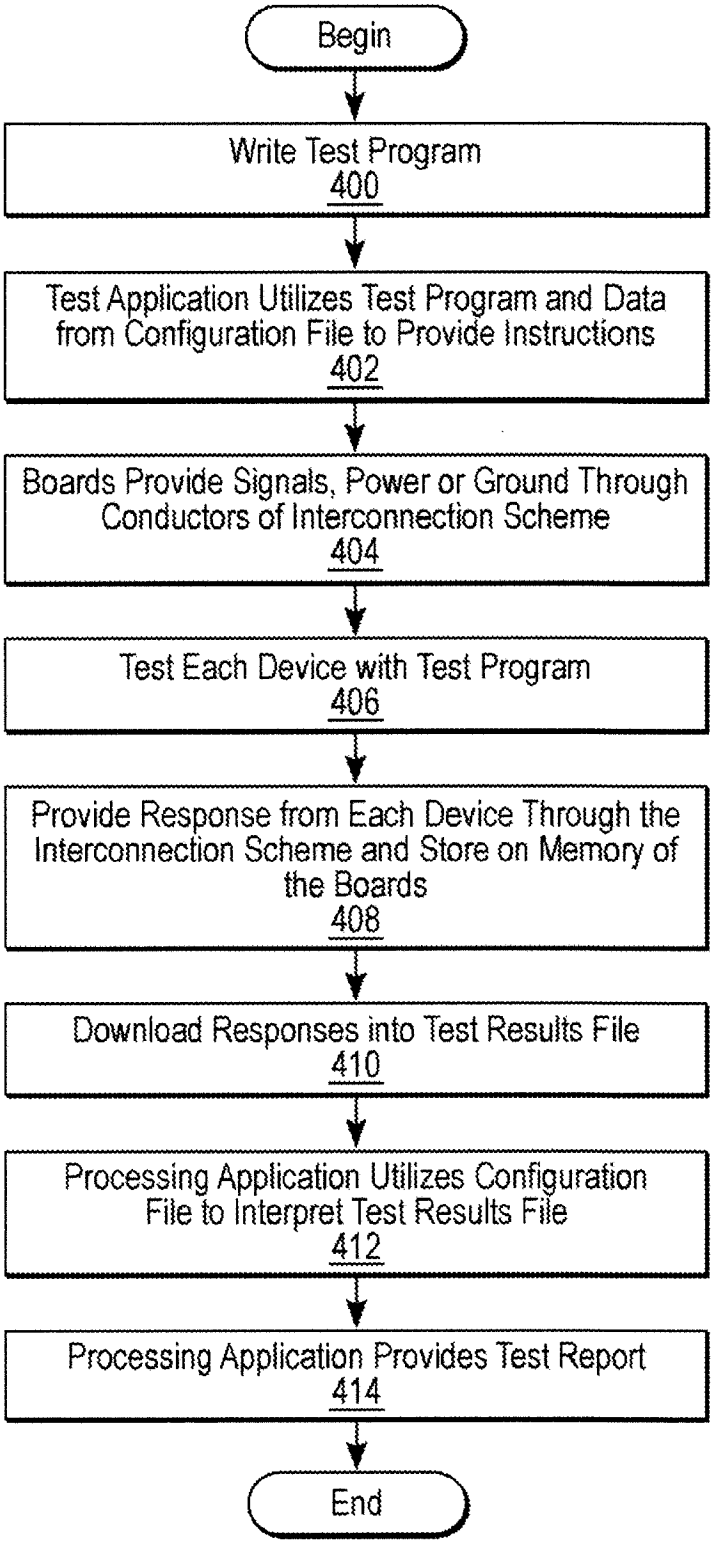
Begin
Write Test Program
400
Test Application Utilizes Test Program and Data from Configuration File to Provide Instructions
402
Boards Provide Signals, Power or Ground Through Conductors of Interconnection Scheme
404
Test Each Device with Test Program
406
Provide Response from Each Device Through the Interconnection Scheme and Store on Memory of the Boards
408
Download Responses into Test Results File
410
Processing Application Utilizes Configuration File to Interpret Test Results File
412
Processing Application Provides Test Report
414
End

FIG. 23

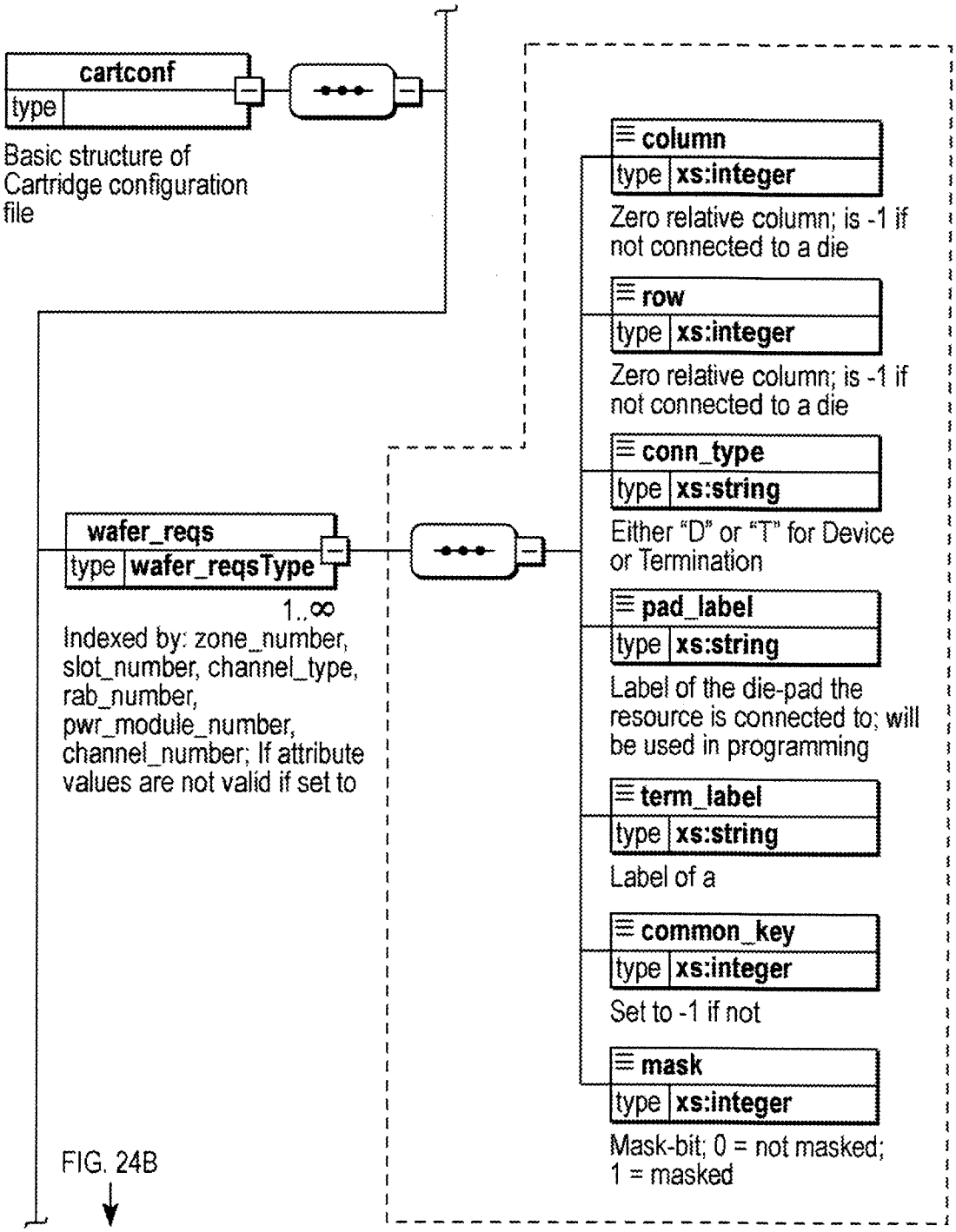
cartconf
type
Basic structure of Cartridge configuration file
wafer_reqs
type wafer_reqsType
1..∞
Indexed by: zone_number, slot_number, channel_type, rab_number, pwr_module_number, channel_number; If attribute values are not valid if set to
column
type xs:integer
Zero relative column; is -1 if not connected to a die
row
type xs:integer
Zero relative column; is -1 if not connected to a die
conn_type
type xs:string
Either "D" or "T" for Device or Termination
pad_label
type xs:string
Label of the die-pad the resource is connected to; will be used in programming
term_label
type xs:string
Label of a
common_key
type xs:integer
Set to -1 if not
mask
type xs:integer
Mask-bit; 0 = not masked; 1 = masked
FIG. 24B

FIG. 24A

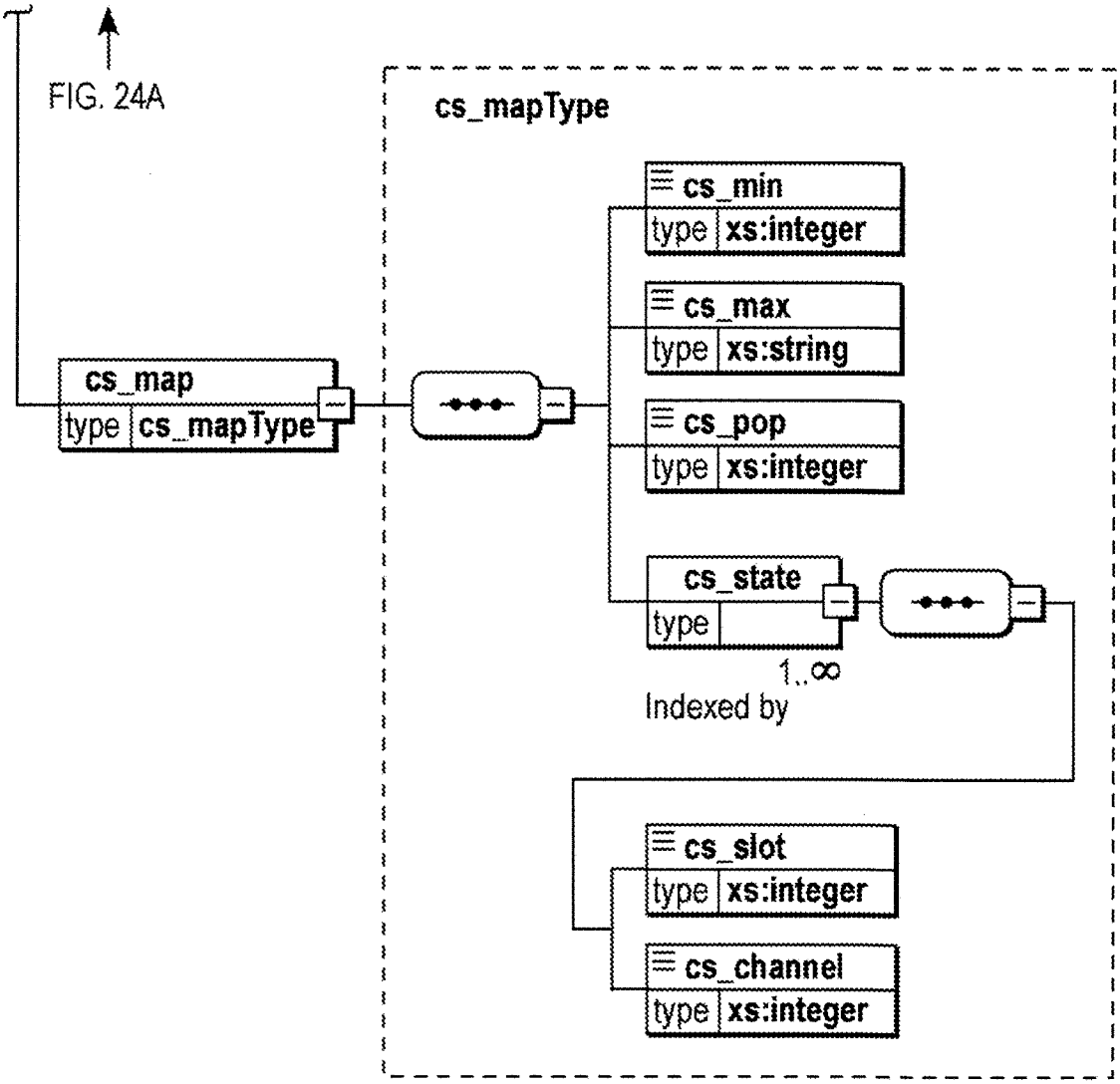
FIG. 24A
cs_mapType
cs_min
type
xs:integer
cs_max
type
xs:string
cs_map
type
cs_mapType
cs_pop
type
xs:integer
cs_state
type
1..∞
Indexed by
cs_slot
type
xs:integer
cs_channel
type
xs:integer

FIG. 24B

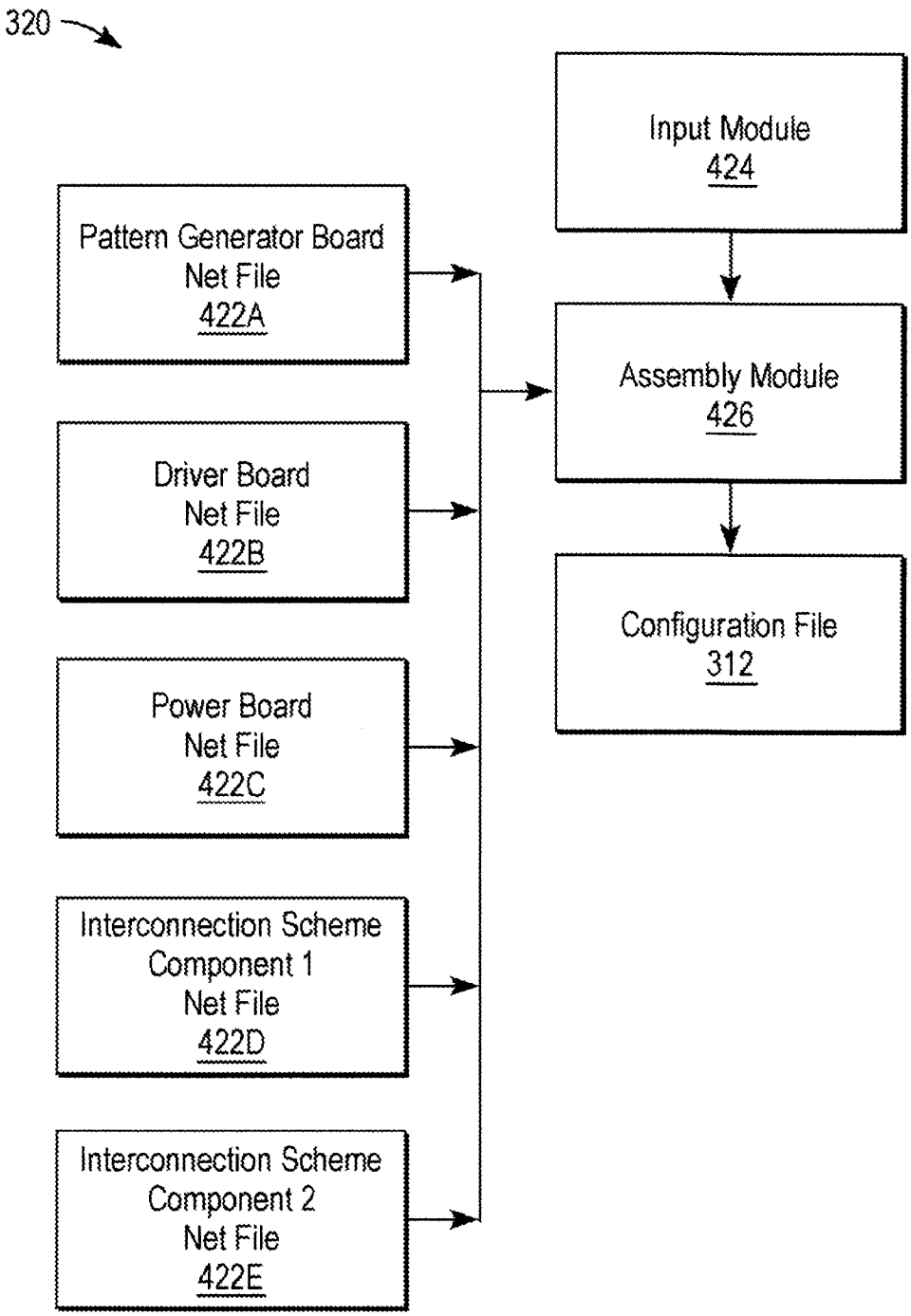
320
Input Module
424
Pattern Generator Board
Net File
422A
Assembly Module
426
Driver Board
Net File
422B
Configuration File
312
Power Board
Net File
422C
Interconnection Scheme
Component 1
Net File
422D
Interconnection Scheme
Component 2
Net File
422E

FIG. 25

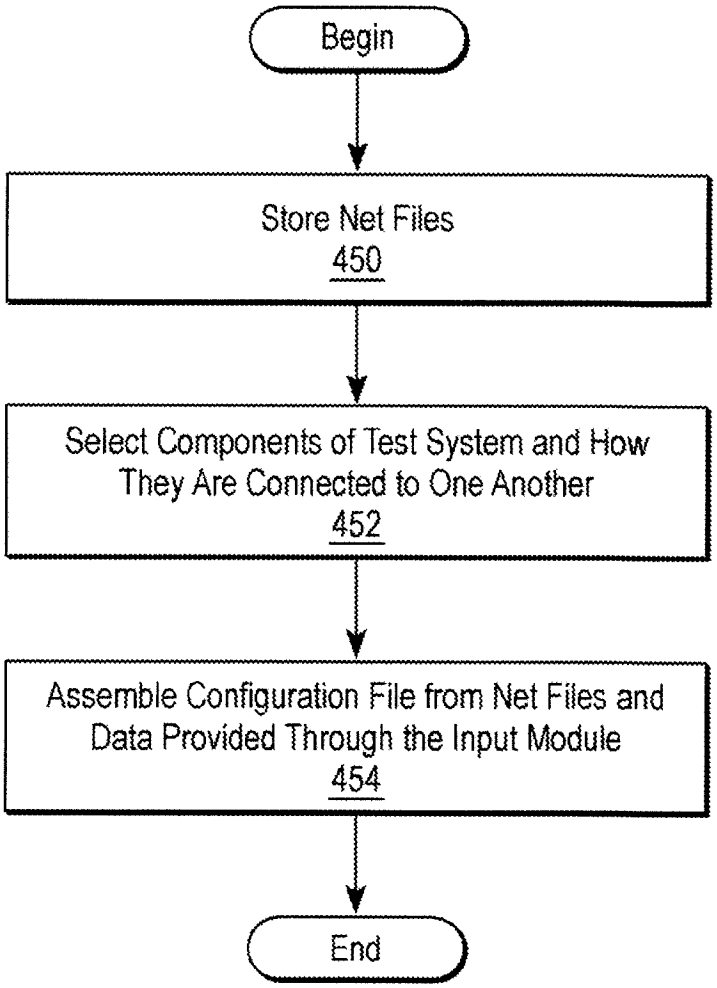
Begin
Store Net Files
450
Select Components of Test System and How They Are Connected to One Another
452
Assemble Configuration File from Net Files and Data Provided Through the Input Module
454
End

FIG. 26

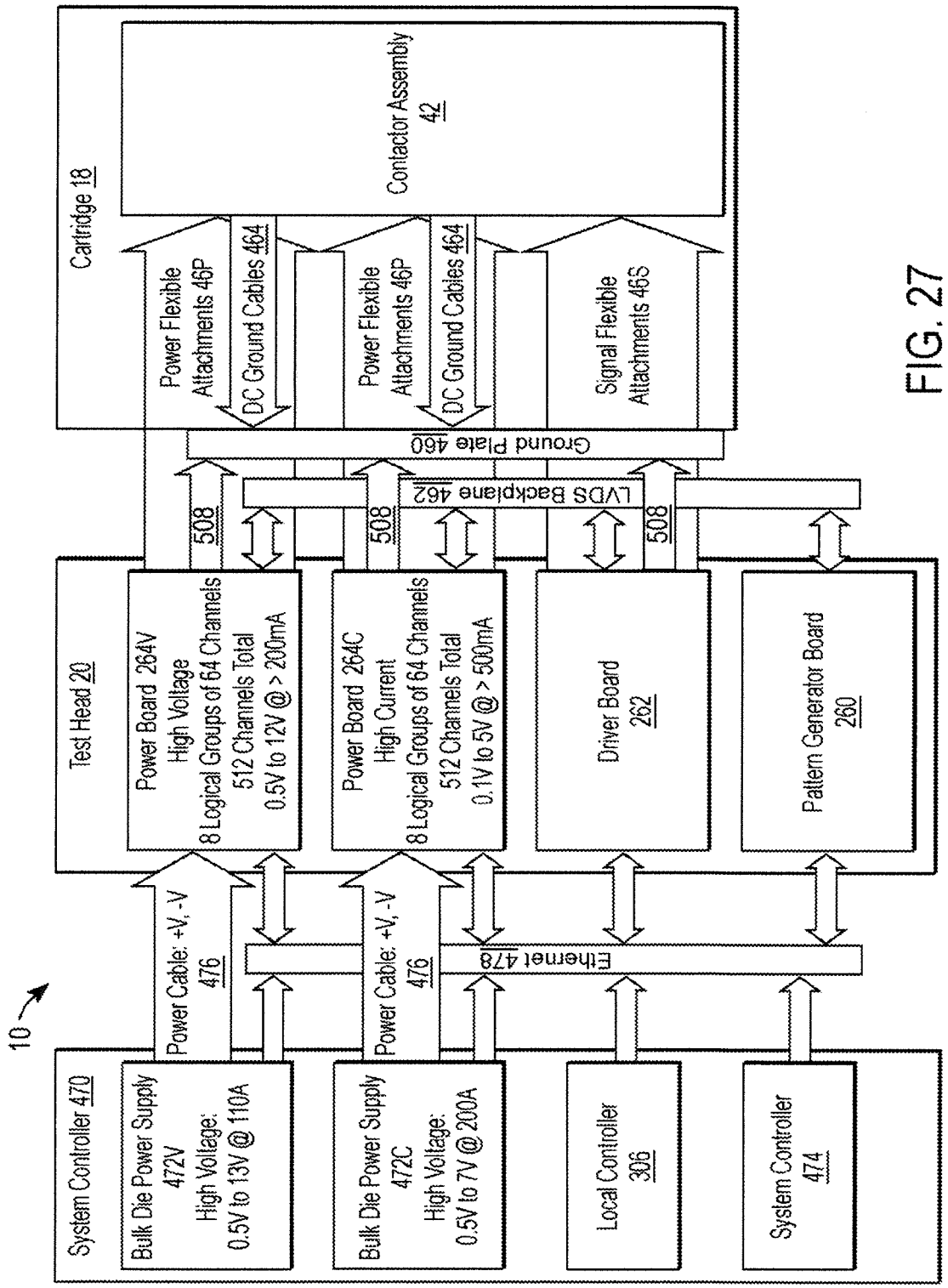
10
System Controller 470
Bulk Die Power Supply 472V
High Voltage:
0.5V to 13V @ 110A
Bulk Die Power Supply 472C
High Voltage:
0.5V to 7V @ 200A
Local Controller 306
System Controller 474
Power Cable: +V, -V 476
Power Cable: +V, -V 476
Ethernet 478
Test Head 20
Power Board 264V
High Voltage
8 Logical Groups of 64 Channels
512 Channels Total
0.5V to 12V @ > 200mA
Power Board 264C
High Current
8 Logical Groups of 64 Channels
512 Channels Total
0.1V to 5V @ > 500mA
Driver Board 262
Pattern Generator Board 260
508
508
508
LVDS Backplane 462
Ground Plate 460
Cartridge 18
Power Flexible Attachments 46P
DC Ground Cables 464
Power Flexible Attachments 46P
DC Ground Cables 464
Signal Flexible Attachments 46S
Contactor Assembly 42

FIG. 27

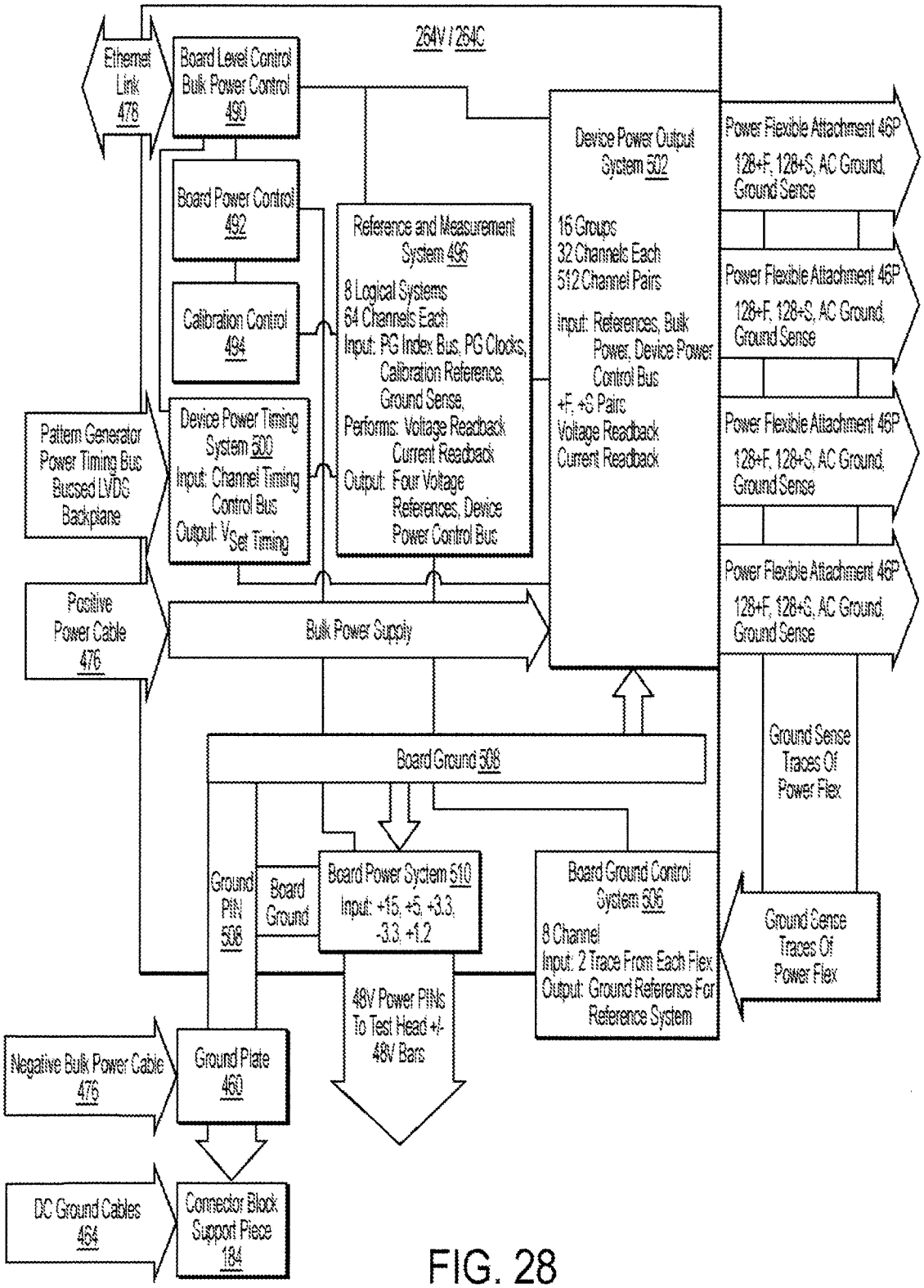
264V / 264C
Ethernet Link 478
Board Level Control Bulk Power Control 490
Board Power Control 492
Calibration Control 494
Reference and Measurement System 496
8 Logical Systems
64 Channels Each
Input: PG Index Bus, PG Clocks, Calibration Reference, Ground Sense,
Performs: Voltage Readback Current Readback
Output: Four Voltage References, Device Power Control Bus
Device Power Output System 502
16 Groups
32 Channels Each
512 Channel Pairs
Input: References, Bulk Power, Device Power Control Bus
+F, +S Pairs
Voltage Readback
Current Readback
Power Flexible Attachment 46P
128+F, 128+S, AC Ground, Ground Sense
Power Flexible Attachment 46P
128+F, 128+S, AC Ground, Ground Sense
Power Flexible Attachment 46P
128+F, 128+S, AC Ground, Ground Sense
Power Flexible Attachment 46P
128+F, 128+S, AC Ground, Ground Sense
Pattern Generator Power Timing Bus Bussed LVDS Backplane
Device Power Timing System 500
Input: Channel Timing Control Bus
Output: VSet Timing
Positive Power Cable 476
Bulk Power Supply
Board Ground 508
Ground Sense Traces Of Power Flex
Ground PIN 508
Board Ground
Board Power System 510
Input: +15, +5, +3.3, -3.3, +1.2
Board Ground Control System 506
8 Channel
Input: 2 Trace From Each Flex
Output: Ground Reference For Reference System
Ground Sense Traces Of Power Flex
48V Power PINs To Test Head +/- 48V Bars
Negative Bulk Power Cable 476
Ground Plate 460
DC Ground Cables 464
Connector Block Support Piece 184

FIG. 28

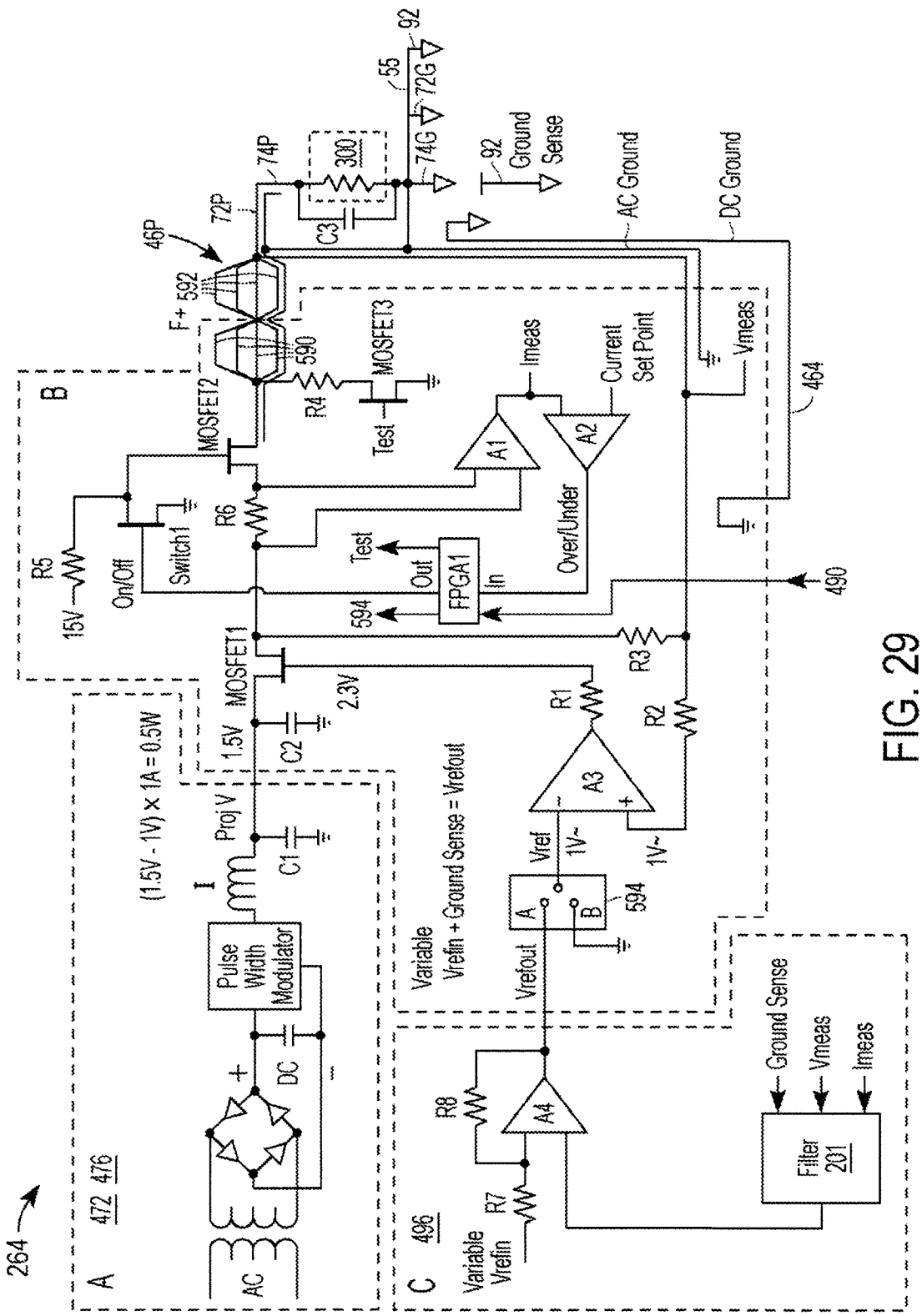
264
A
472 476
AC
DC
Pulse Width Modulator
I
Proj V
C1
(1.5V - 1V) x 1A = 0.5W
1.5V
C2
2.3V
MOSFET1
B
R5
15V
On/Off
Switch1
R6
MOSFET2
R4
590
MOSFET3
Test
F+ 592
46P
72P
74P
C3
300
74G
55
72G
92
92
Ground Sense
AC Ground
DC Ground
Imeas
Current Set Point
Vmeas
464
A1
A2
Over/Under
Test
Out
FPGA1
In
594
490
R3
R1
R2
A3
Vref
1V~
1V~
594
A
B
Variable Vrefin + Ground Sense = Vrefout
Vrefout
C
496
Variable Vrefin
R7
R8
A4
Ground Sense
Vmeas
Imeas
Filter 201

FIG. 29

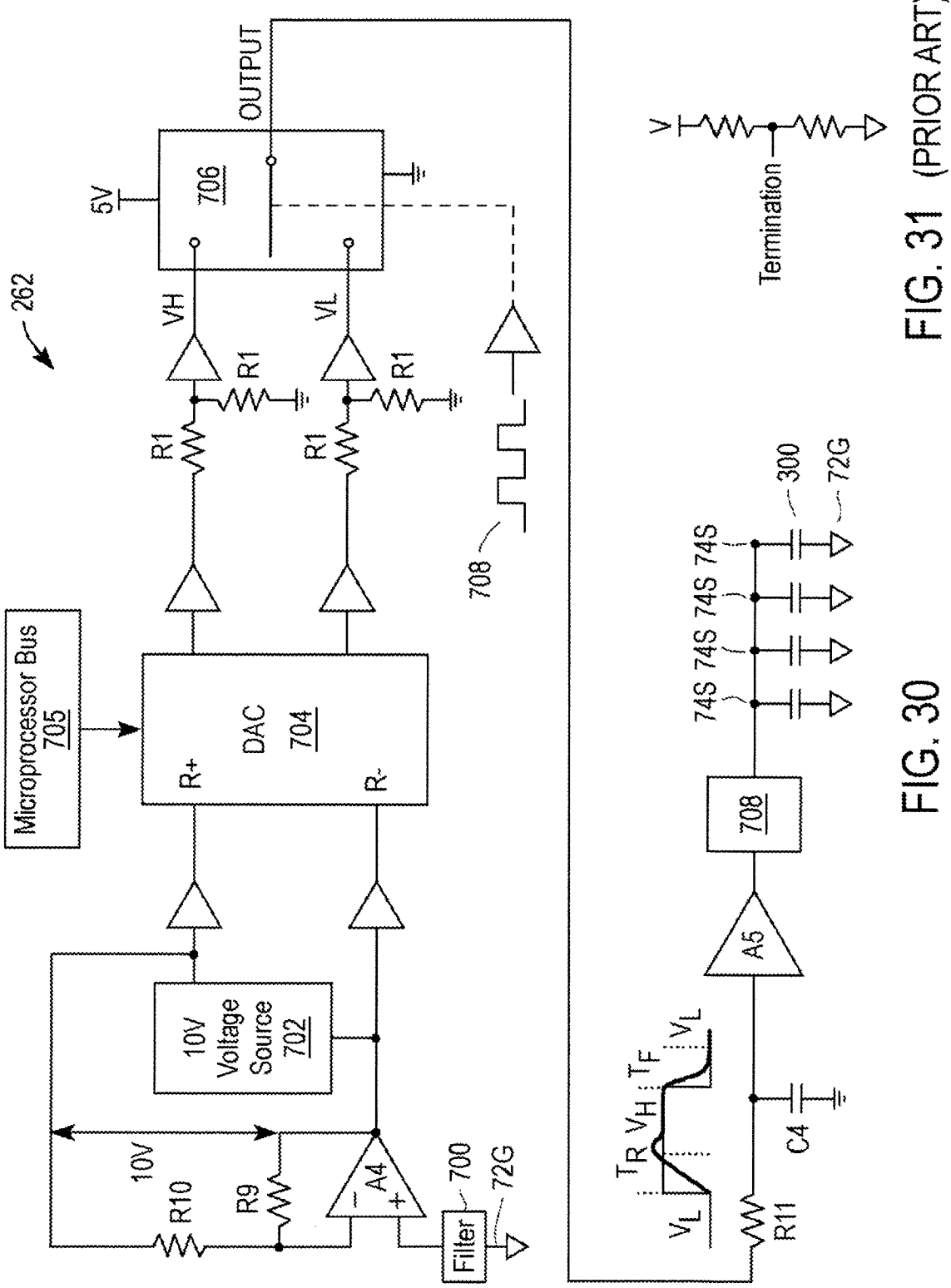

FIG. 30

FIG. 31 (PRIOR ART)

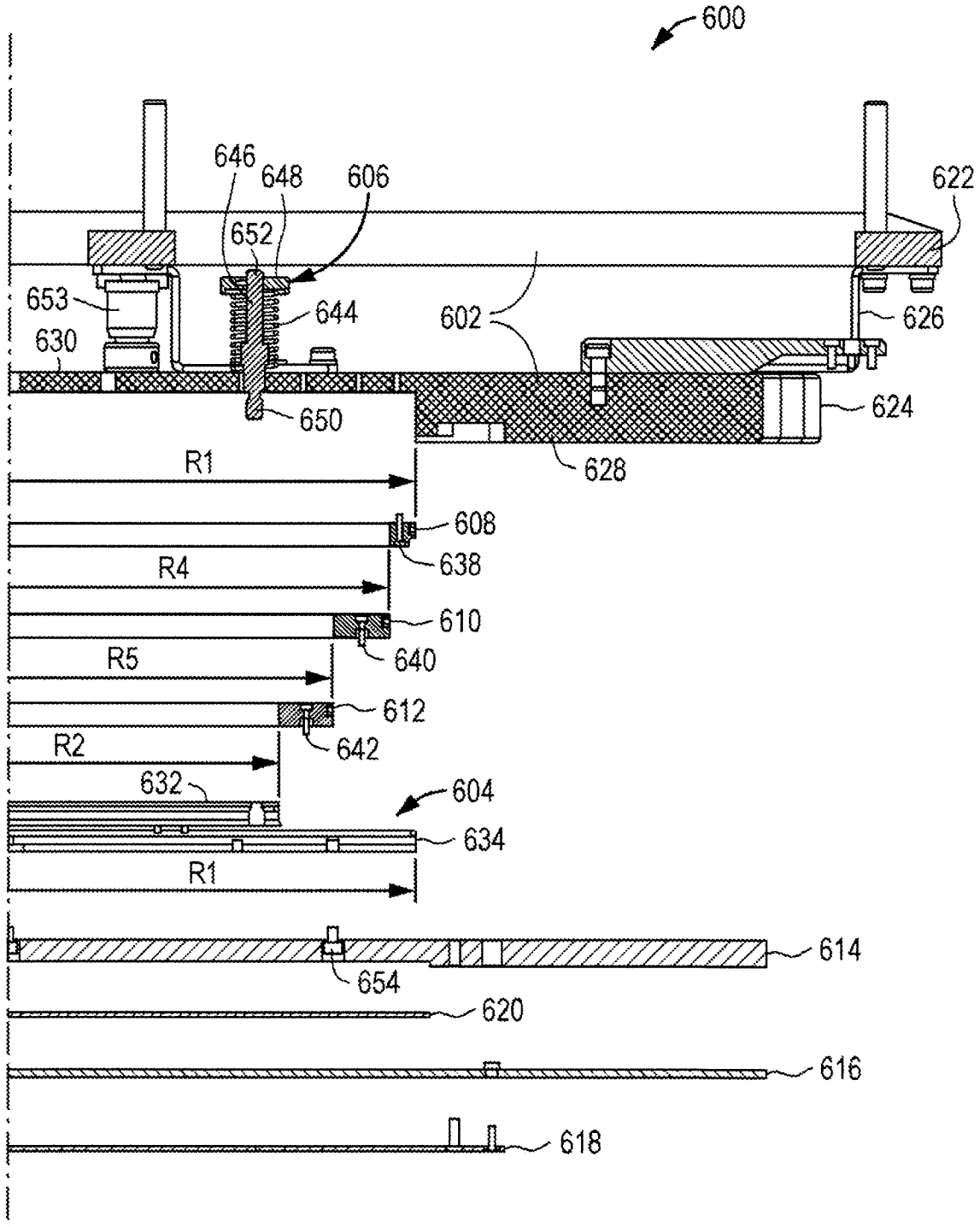
600
646
648
606
652
622
653
644
602
626
630
650
624
628
R1
608
638
R4
610
640
R5
612
642
R2
632
604
634
R1
614
654
620
616
618

FIG. 32

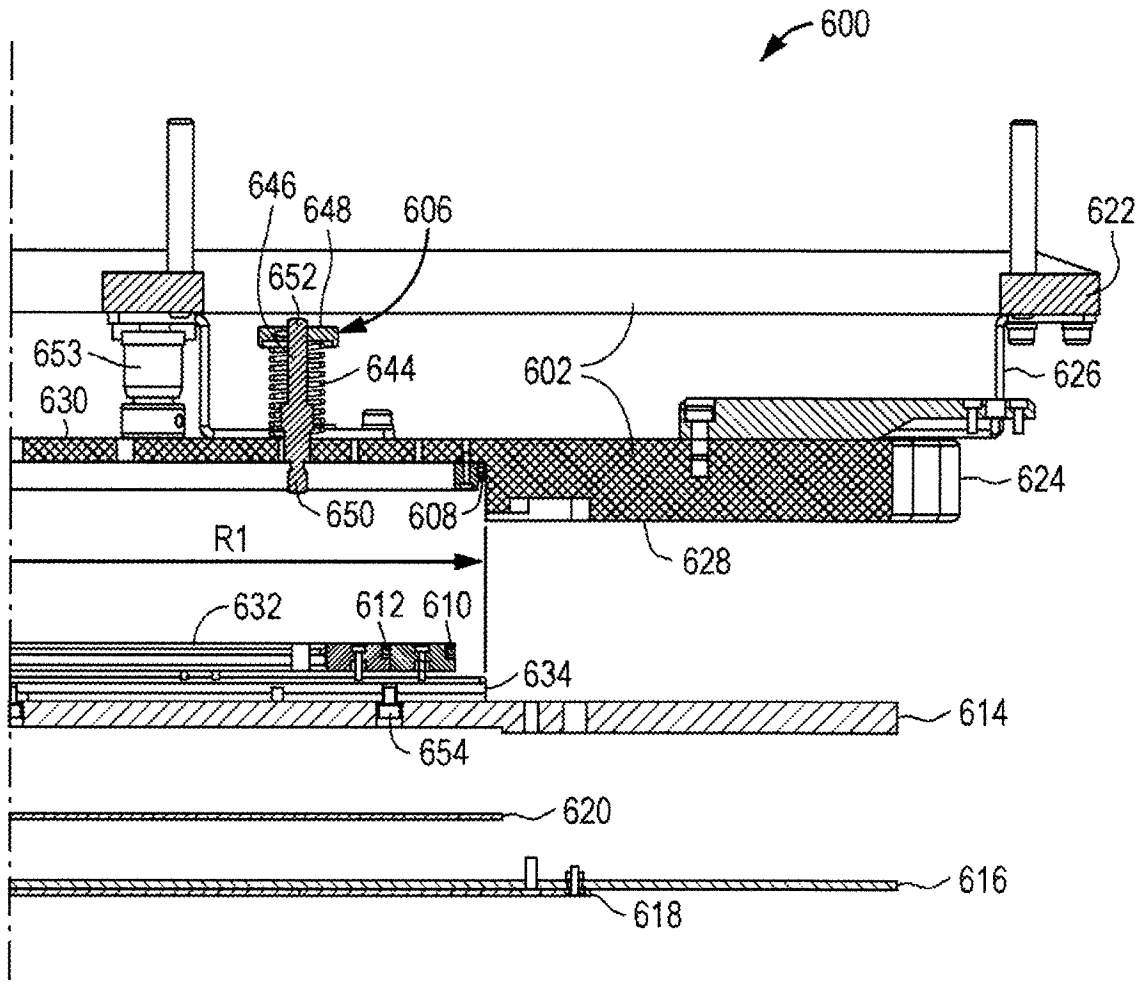
600
646
648
606
652
622
653
644
602
626
630
624
650
608
R1
628
632
612
610
634
614
654
620
616
618

FIG. 33

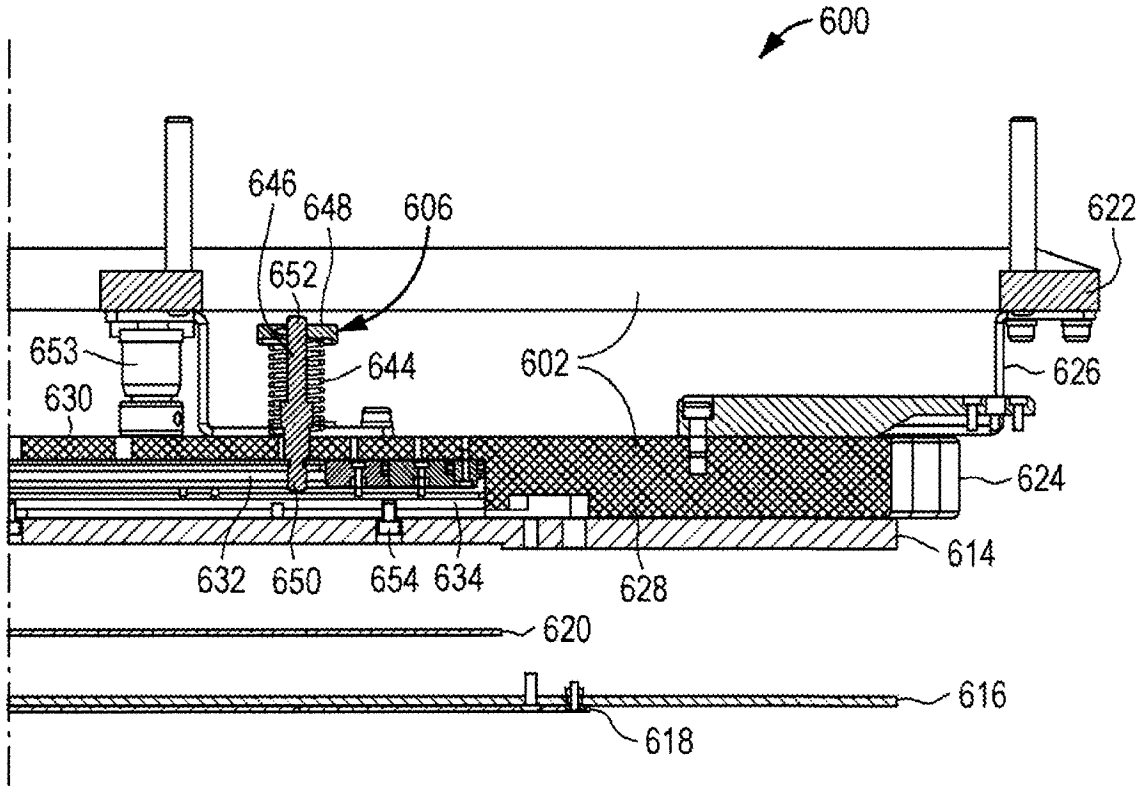
600
646
648
606
622
652
653
644
602
626
630
624
614
632
650
654
634
628
620
616
618

FIG. 34

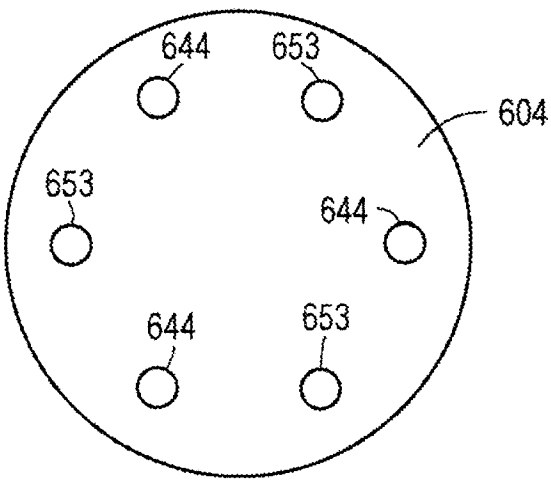
644
653
604
653
644
644
653

FIG. 35

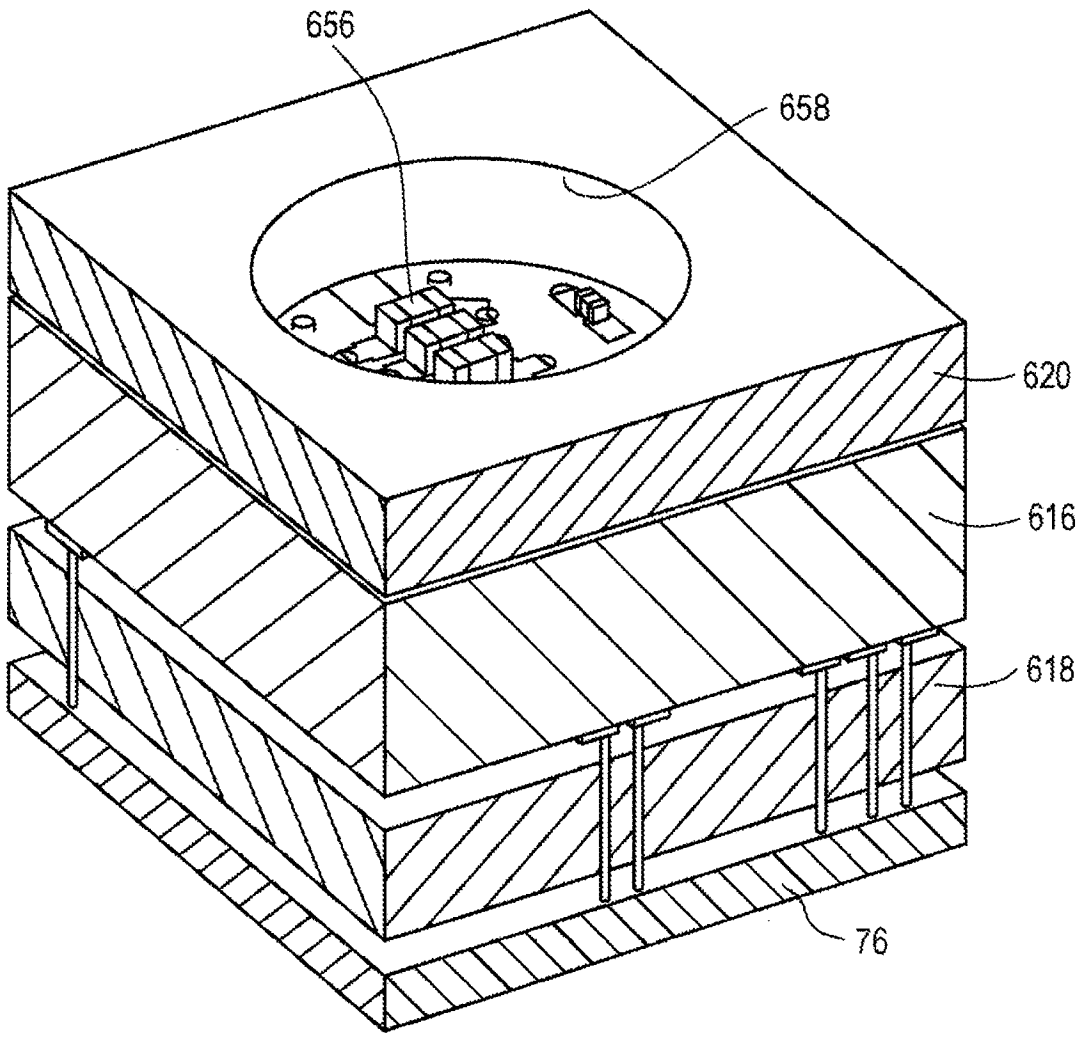

FIG. 36

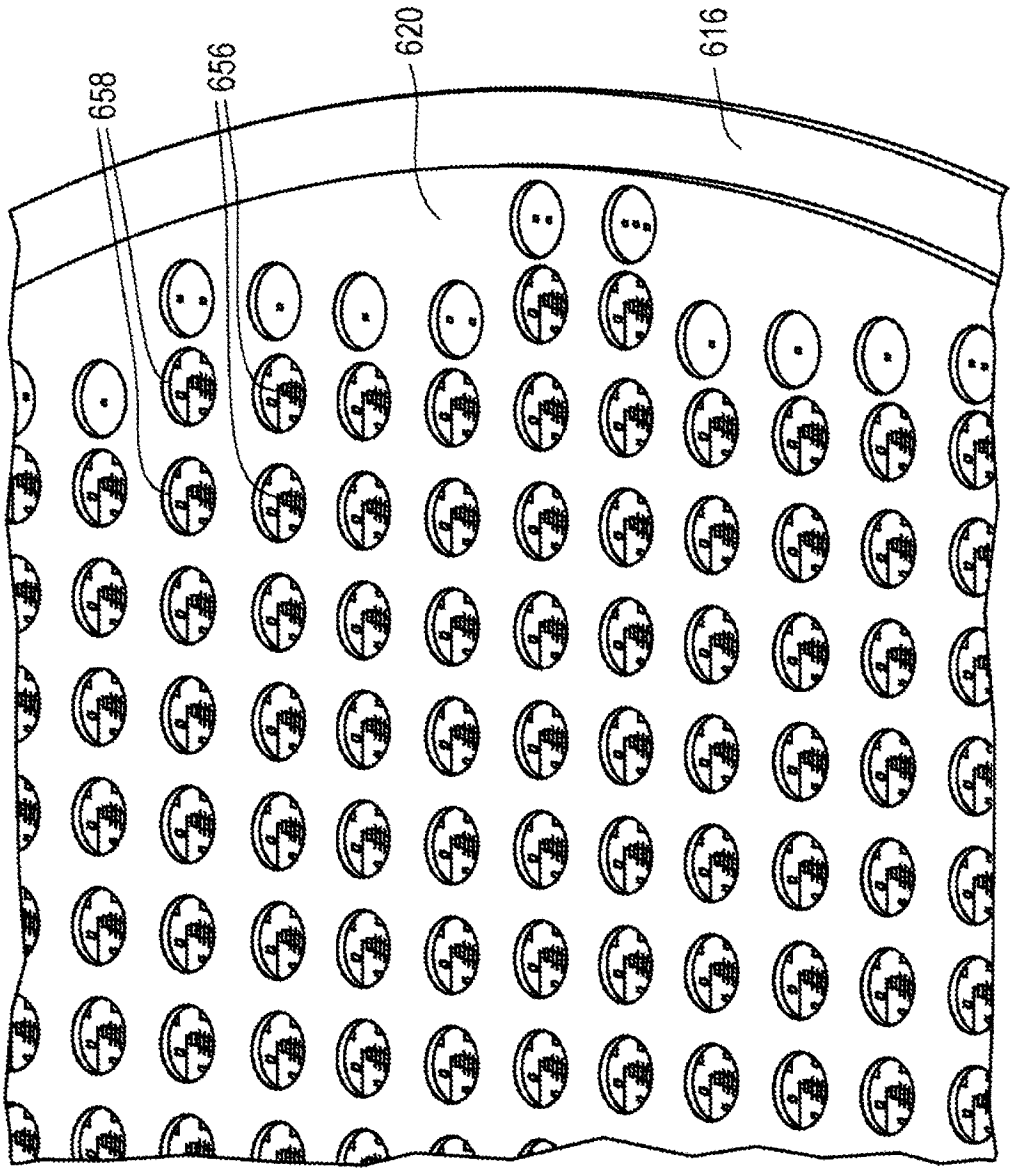

FIG. 37

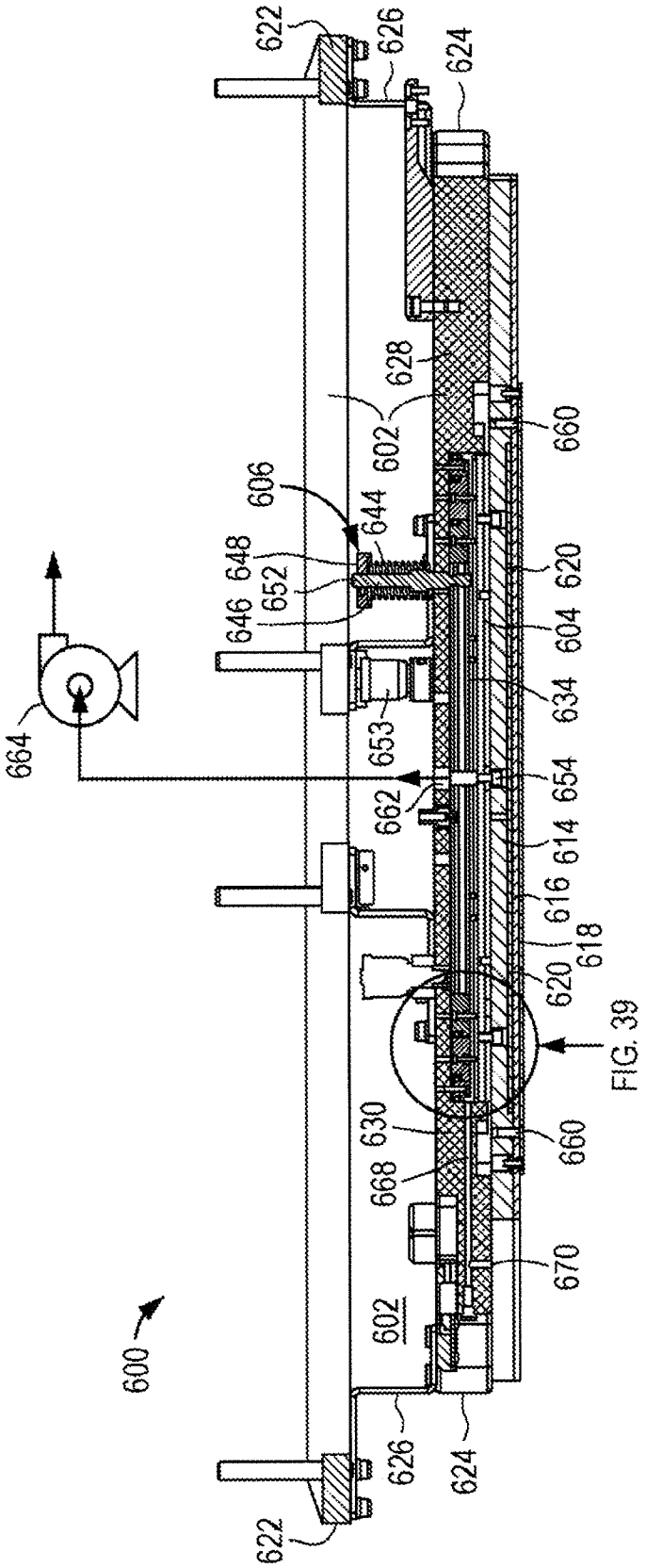
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FIG. 39
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FIG. 38

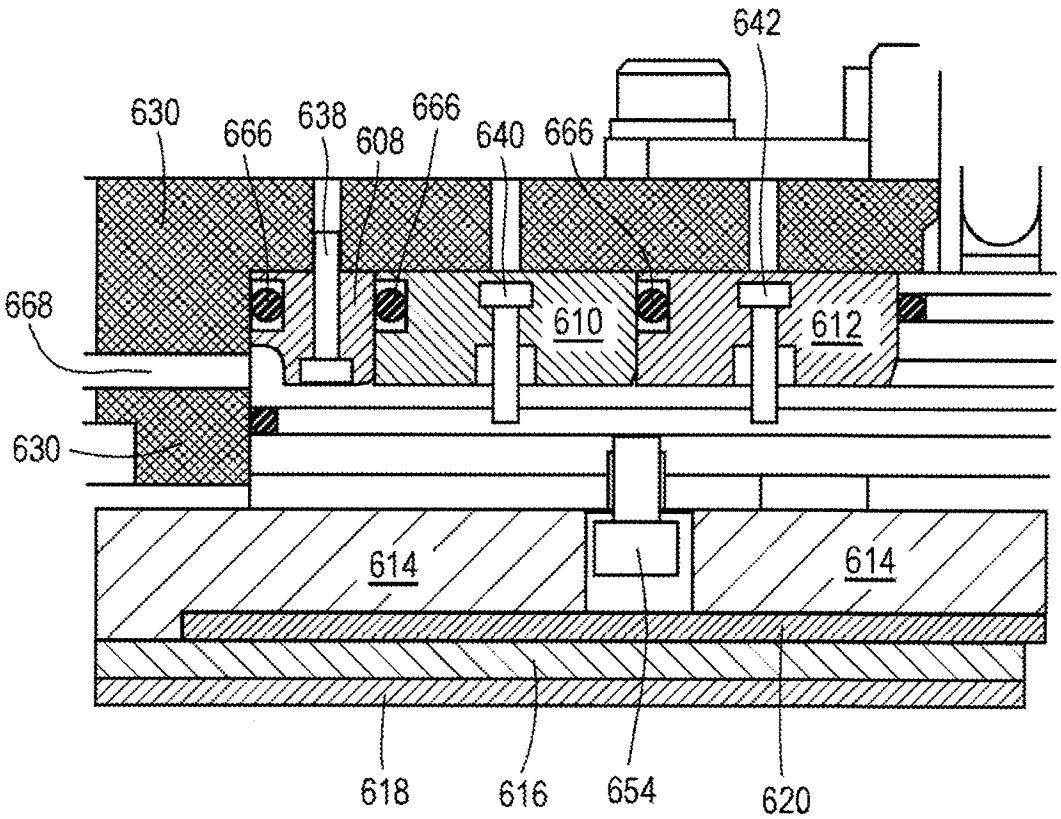
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FIG. 39

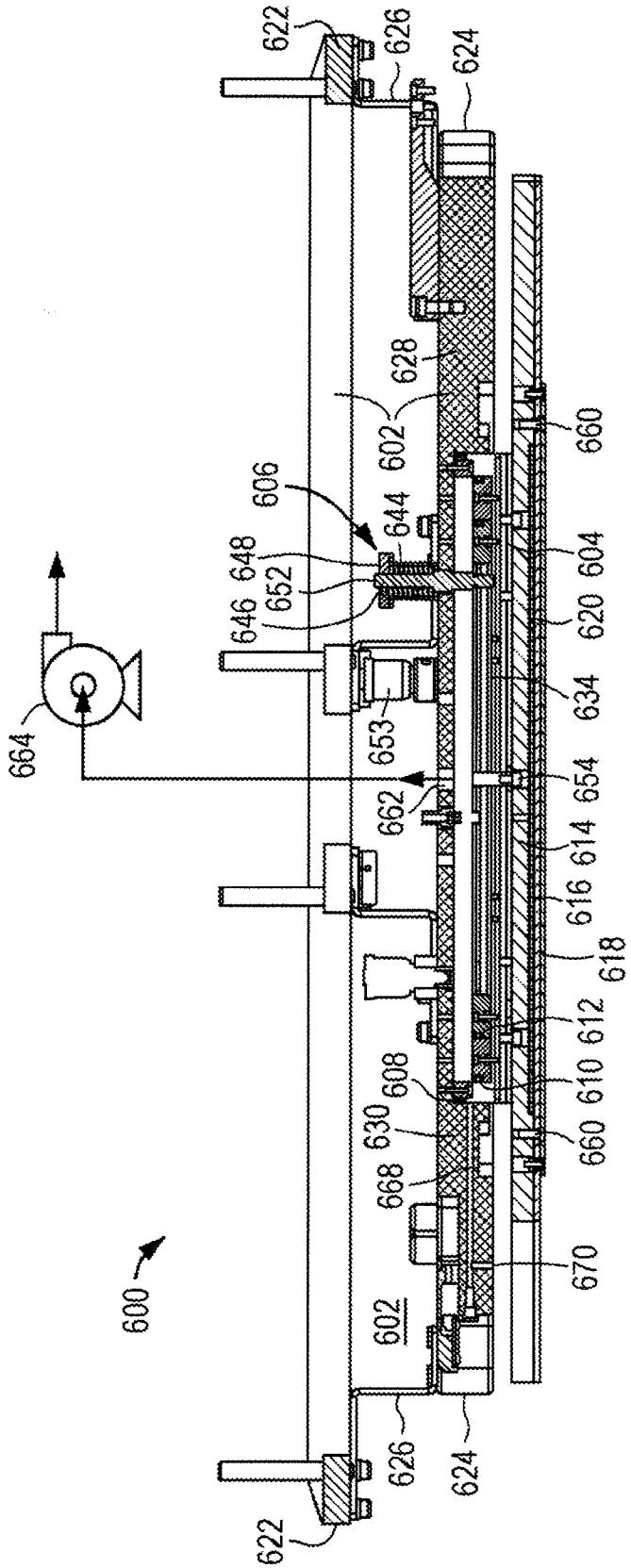
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FIG. 40

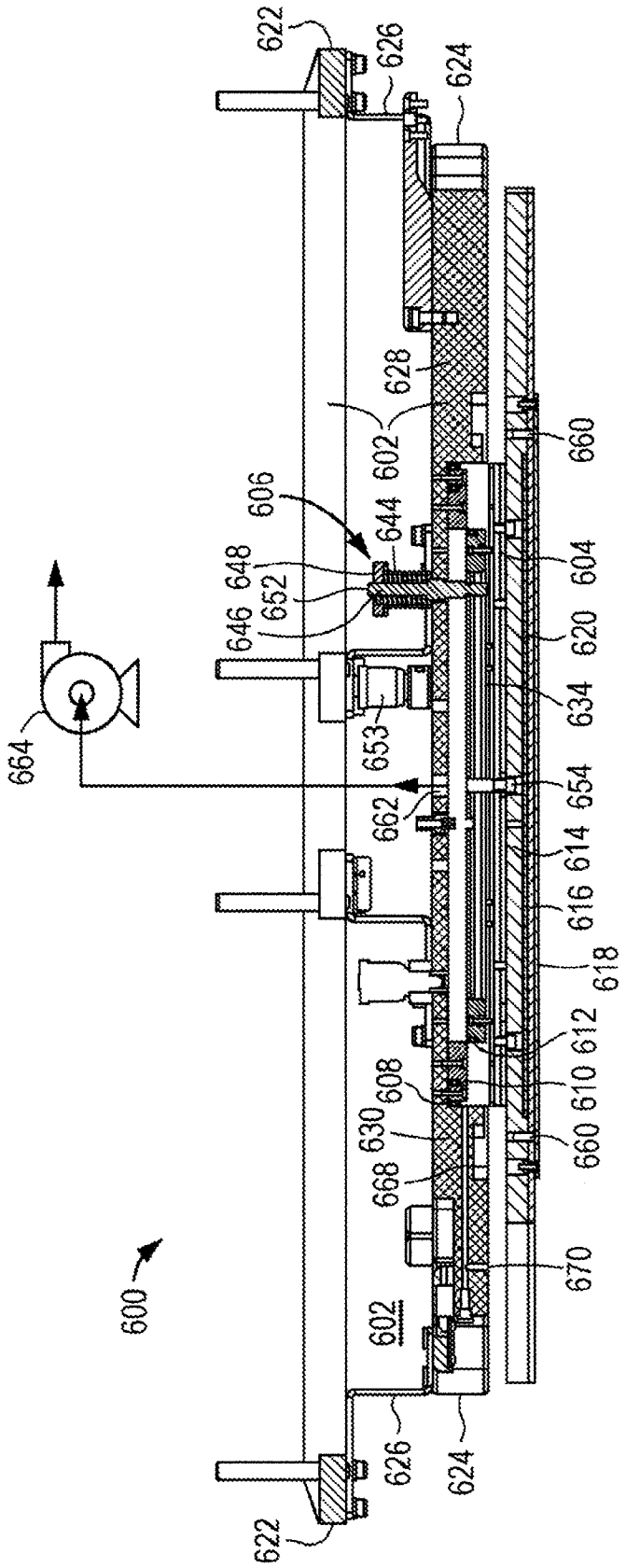
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FIG. 41

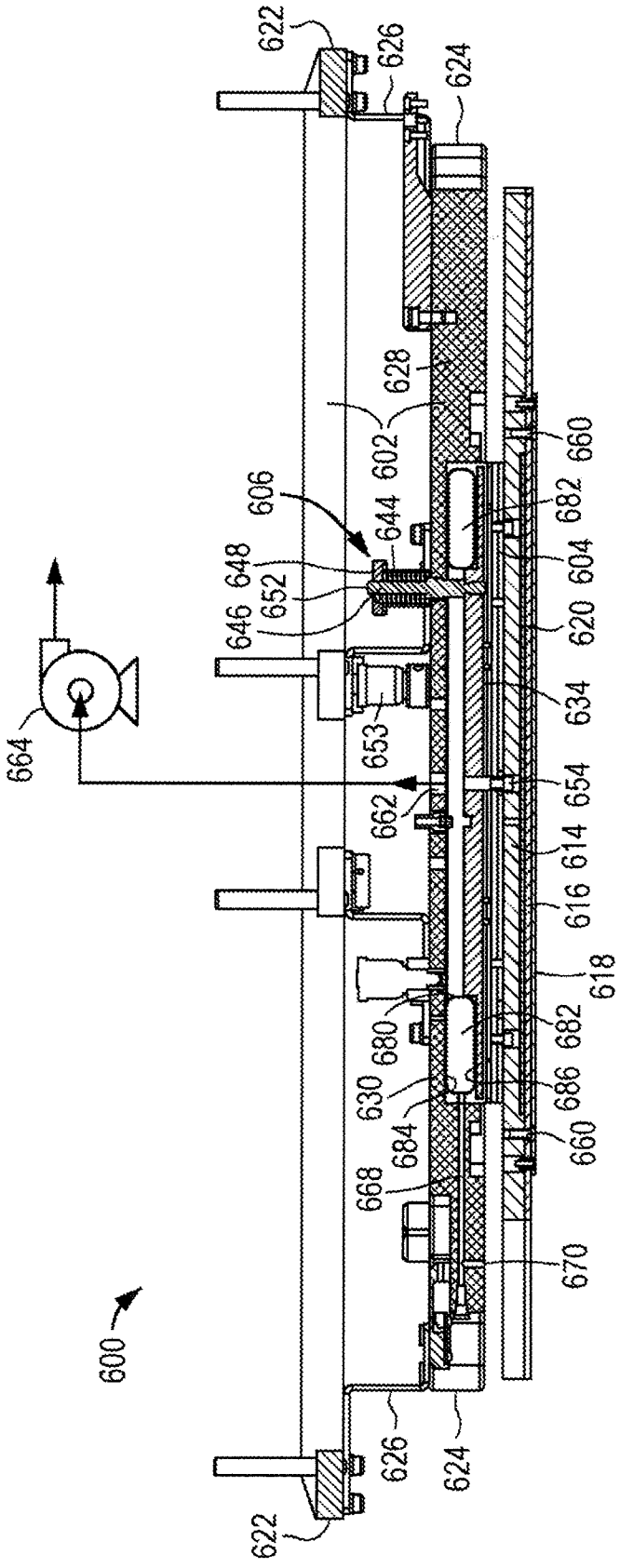
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FIG. 42

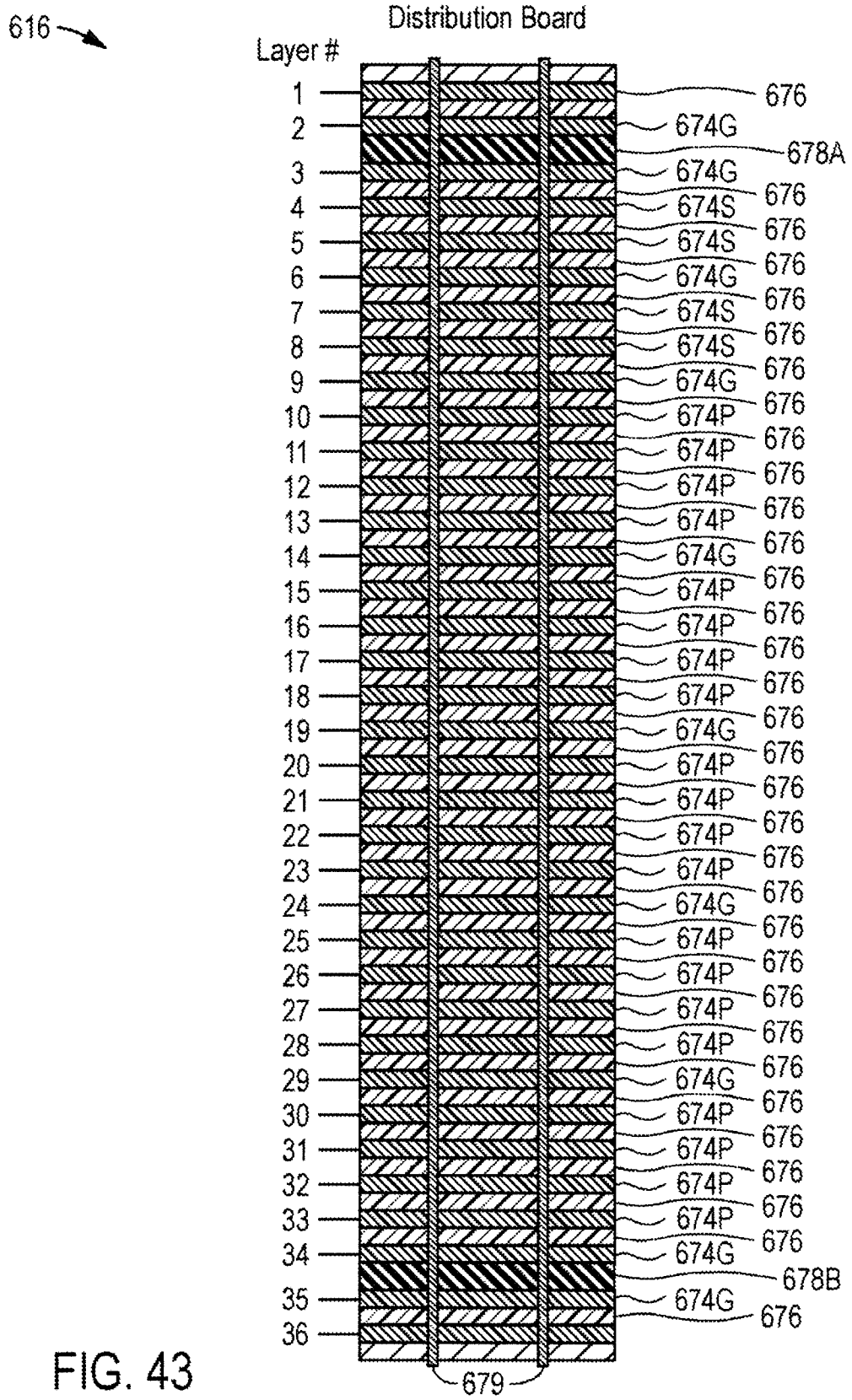
616
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FIG. 43

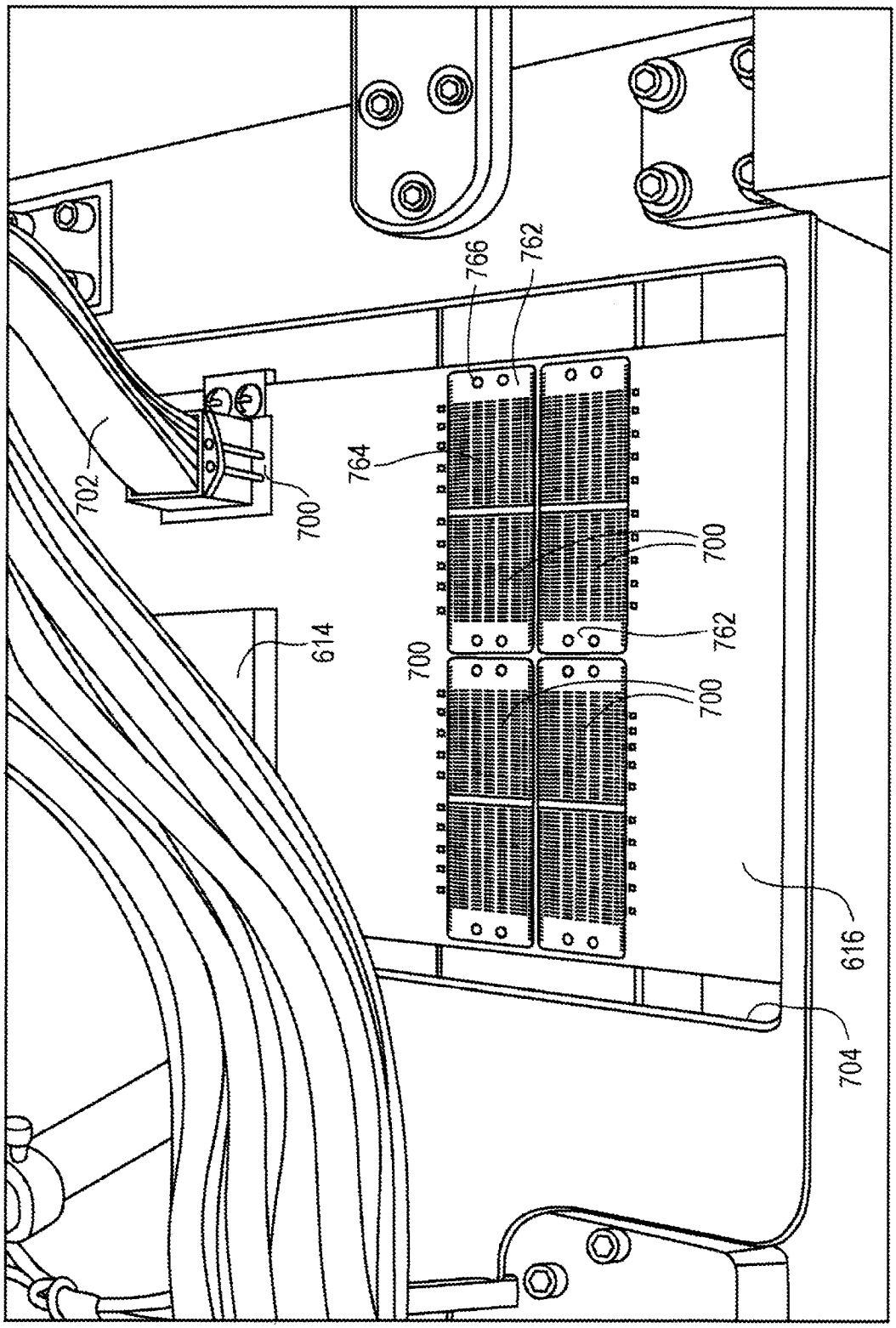

FIG. 44

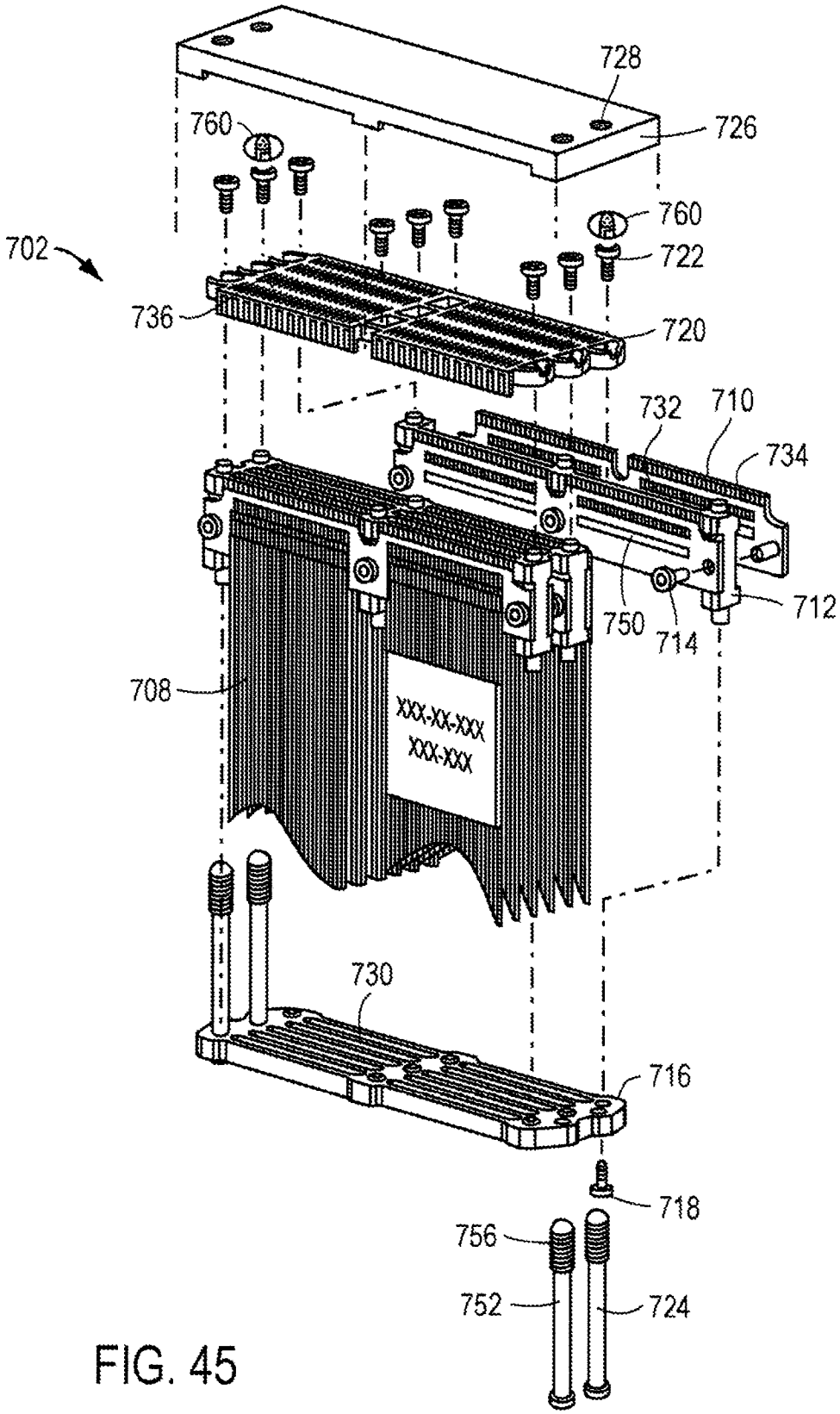
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FIG. 45

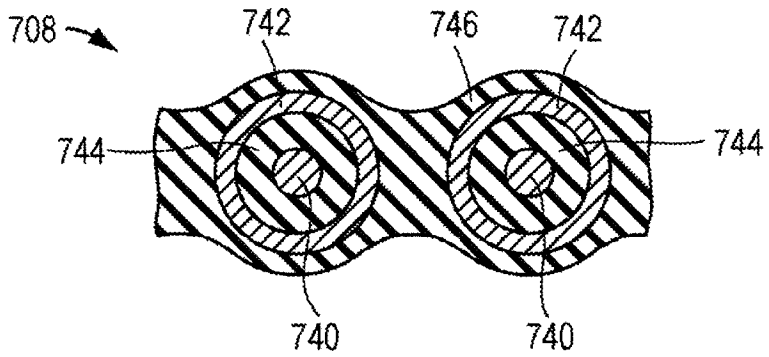
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FIG. 46

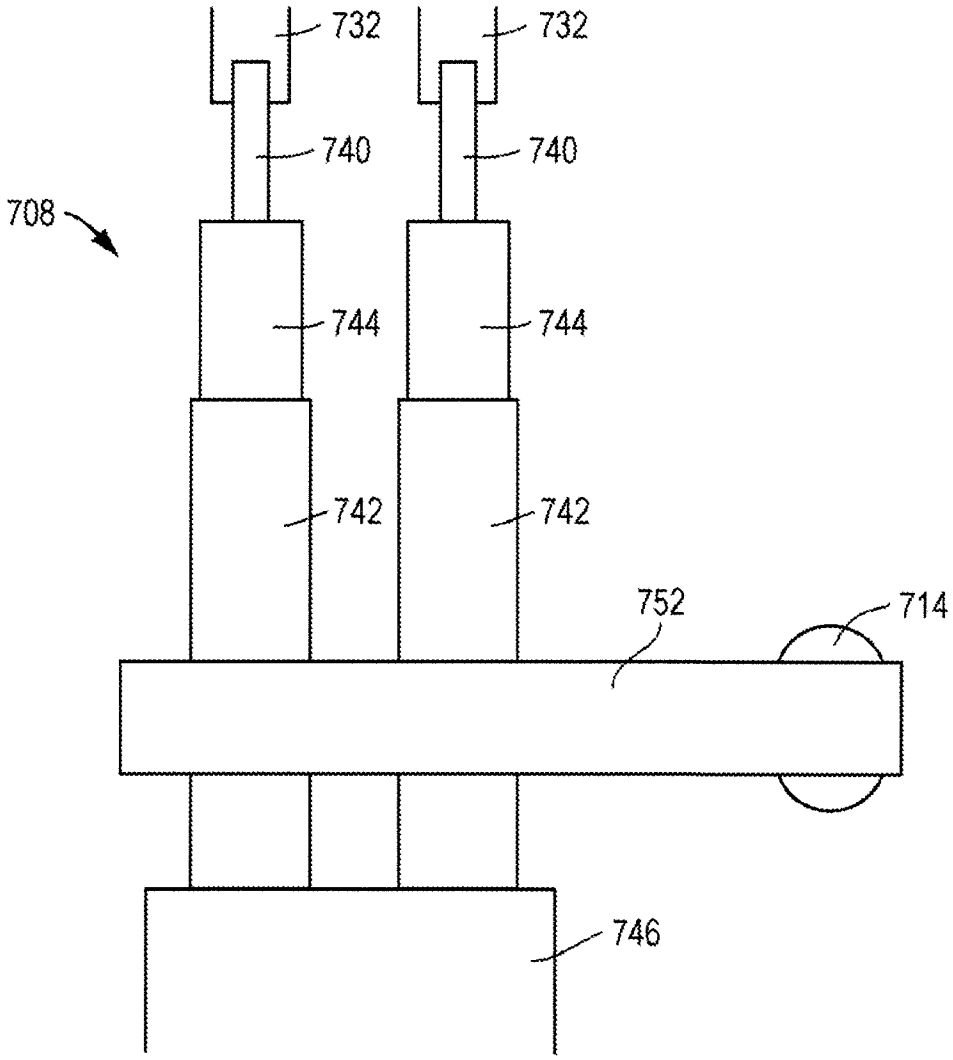
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FIG. 47

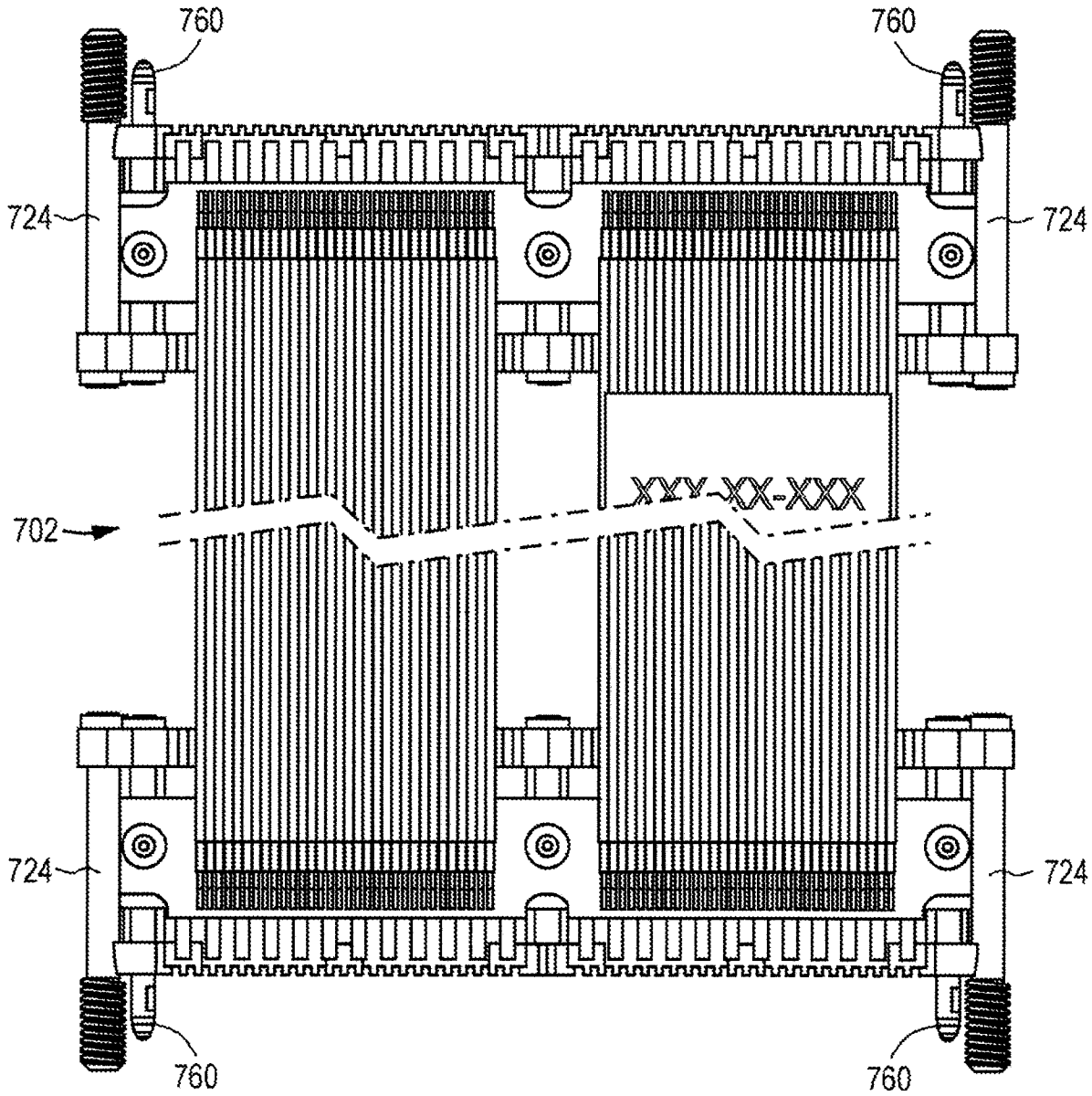

FIG. 48