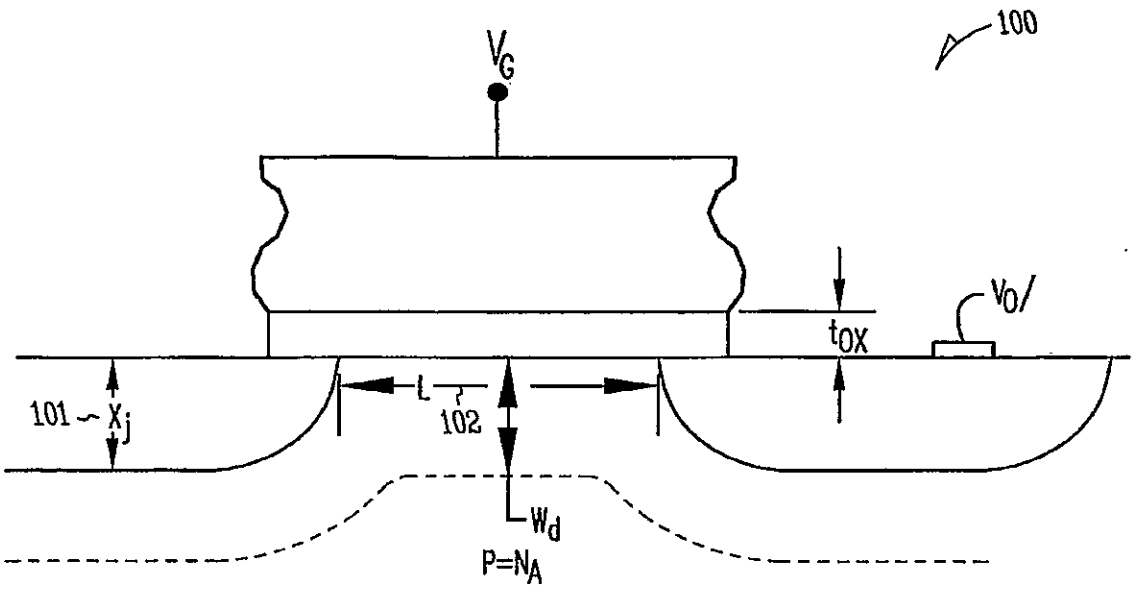


$V_G \longrightarrow V_G/k$ $\quad V_O \longrightarrow V_O/k$

$t_{OX} \longrightarrow t_{OX}/k$

$L \longrightarrow L/k$

$X_j \longrightarrow X_j/k$ JUNCTION DEPTH DECREASED

$W_d \longrightarrow W_d/k$

$N_A \longrightarrow k\ N_A$ SUBSTRATE DOPING INCREASED

FIG. 1

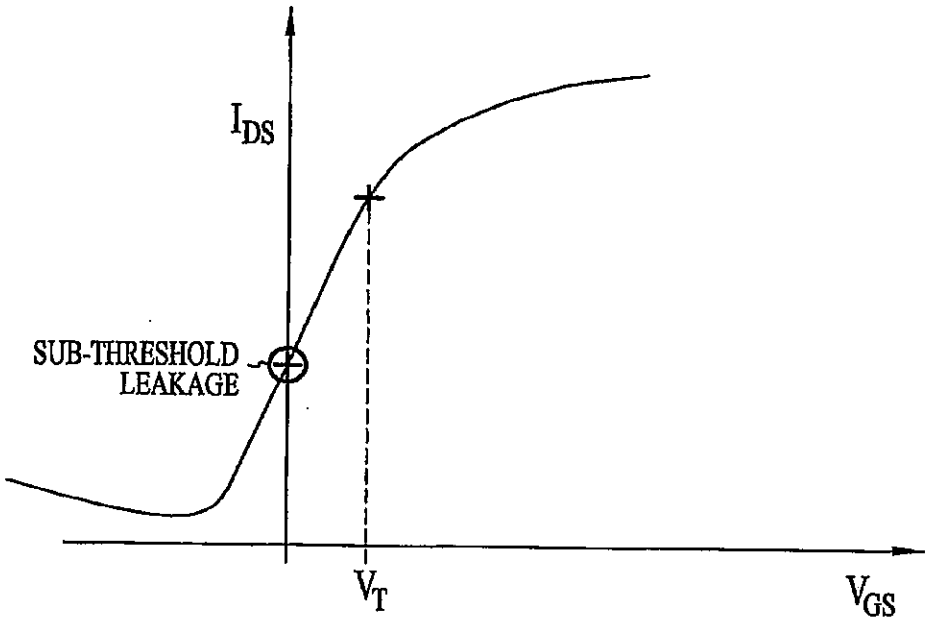

I_{DS}
SUB-THRESHOLD LEAKAGE
V_T
V_{GS}

FIG. 2

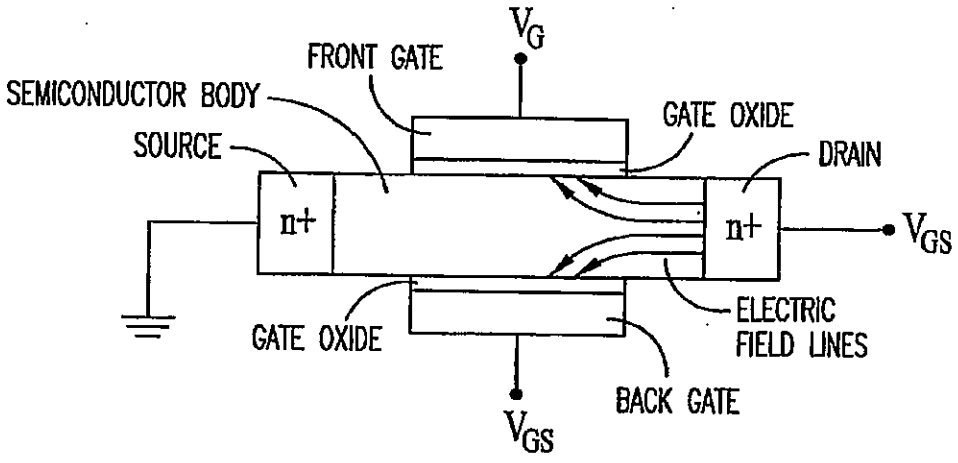

V_G
FRONT GATE
SEMICONDUCTOR BODY
SOURCE
GATE OXIDE
DRAIN
n+
n+
V_{GS}
GATE OXIDE
ELECTRIC FIELD LINES
BACK GATE
V_{GS}

FIG. 3

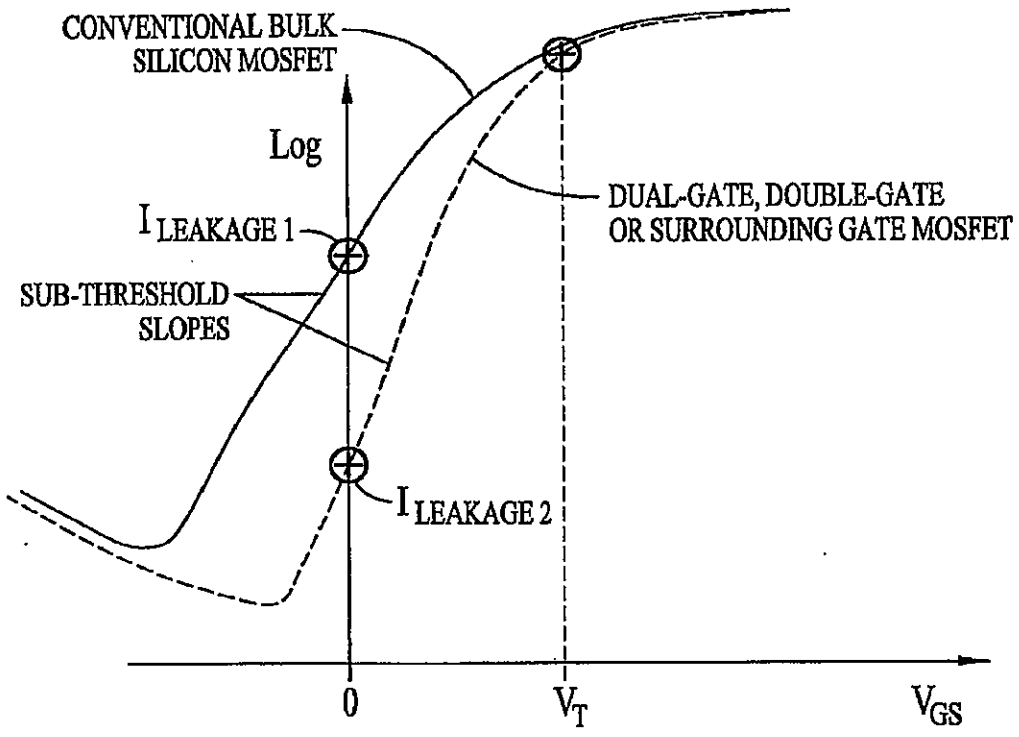

CONVENTIONAL BULK
SILICON MOSFET
Log
I LEAKAGE 1
SUB-THRESHOLD
SLOPES
DUAL-GATE, DOUBLE-GATE
OR SURROUNDING GATE MOSFET
I LEAKAGE 2
0
V_T
V_{GS}

FIG. 4

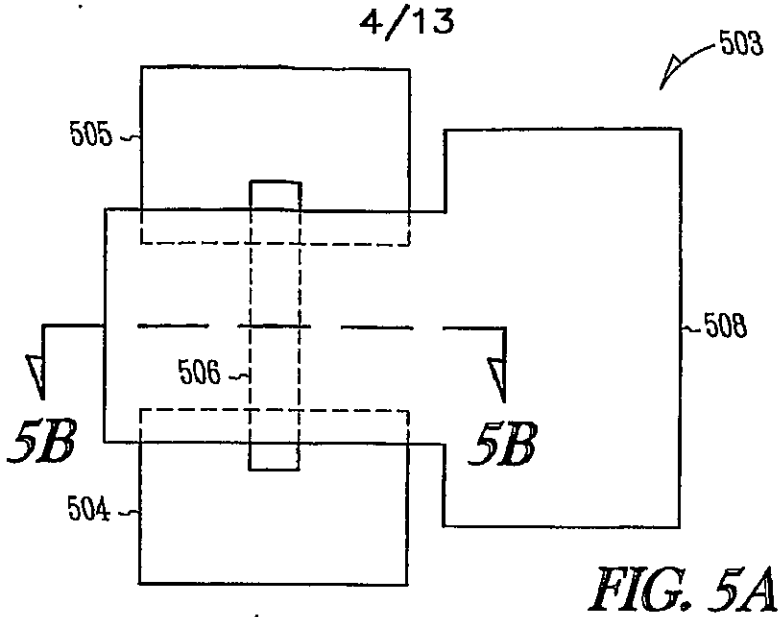


FIG. 5A
(PRIOR ART)

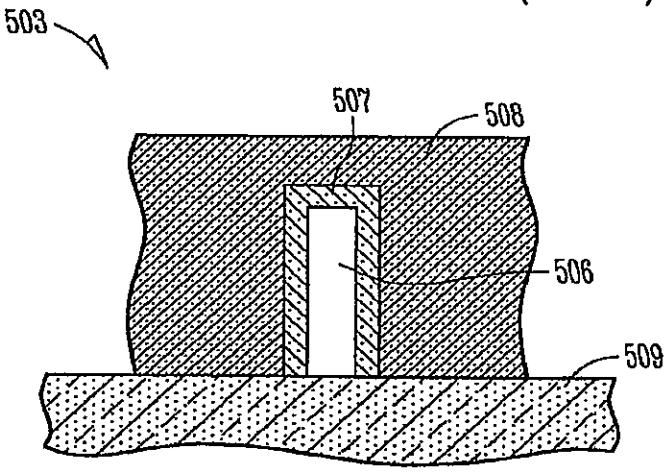


FIG. 5B
(PRIOR ART)

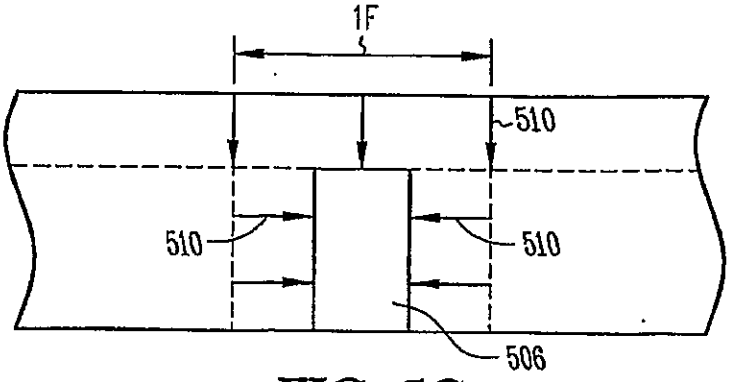


FIG. 5C
(PRIOR ART)

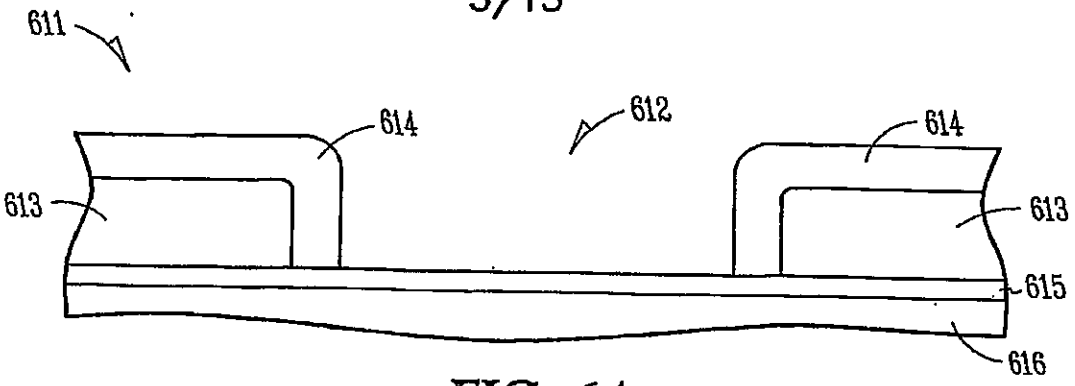


FIG. 6A

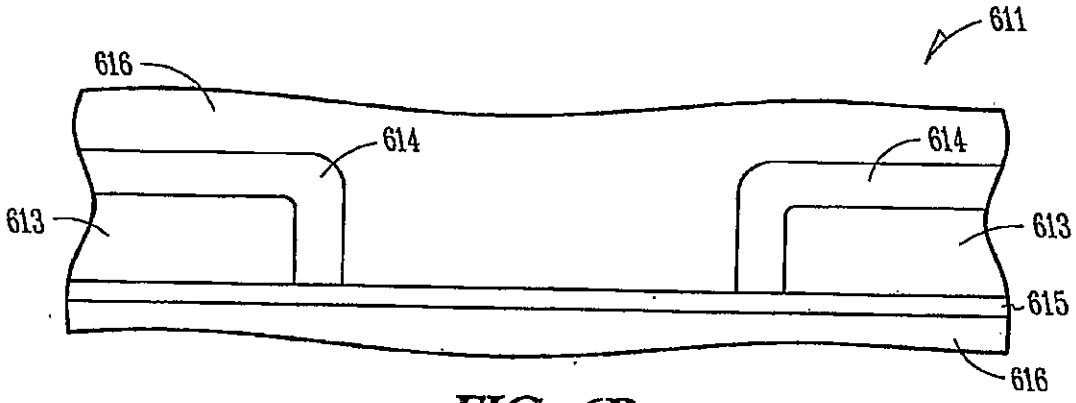


FIG. 6B

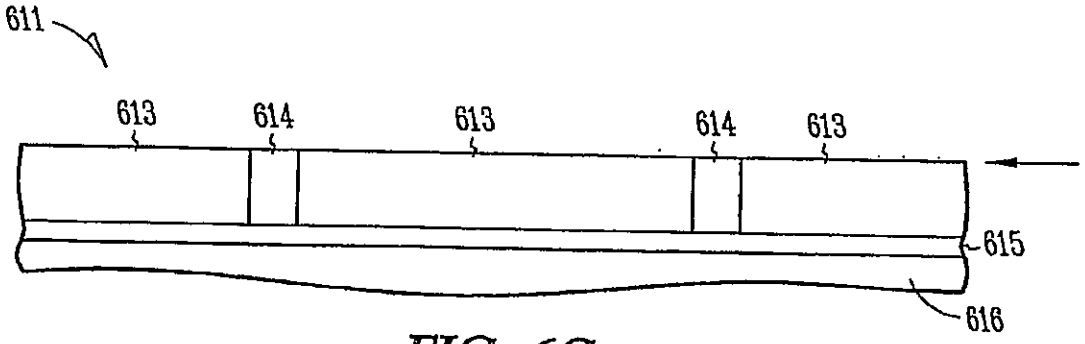


FIG. 6C

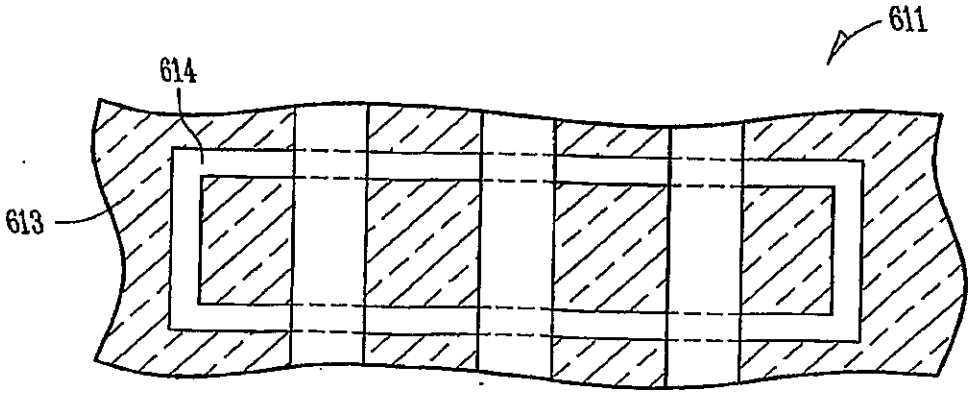


FIG. 6D

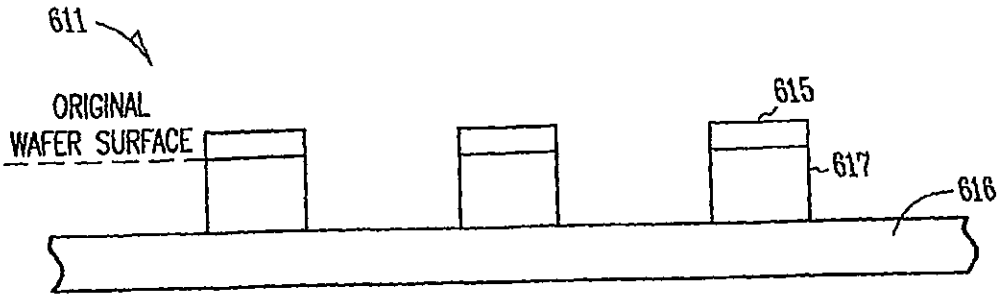


FIG. 6E

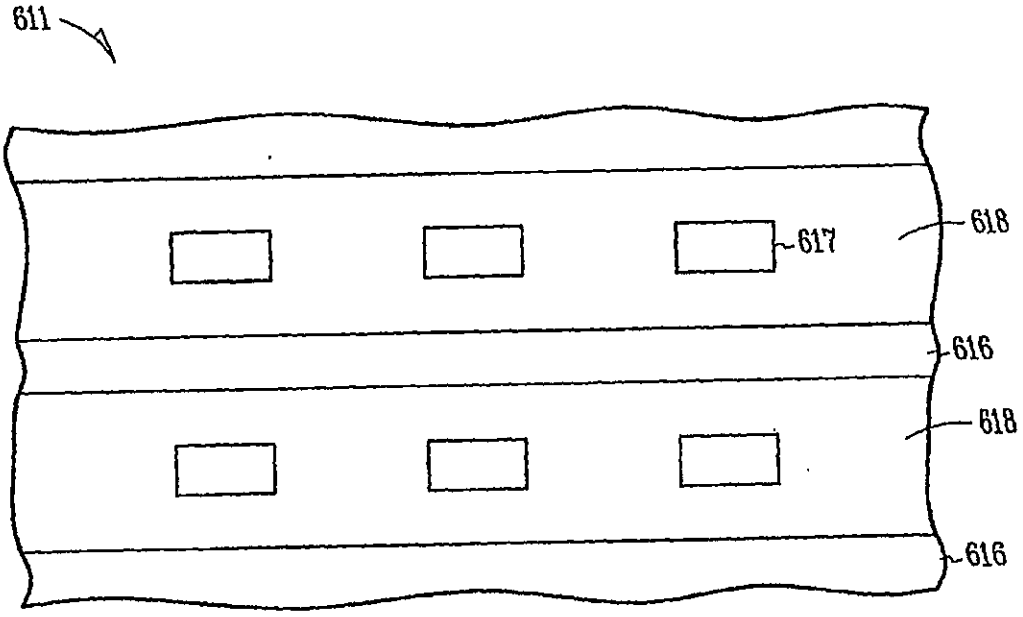


FIG. 6F

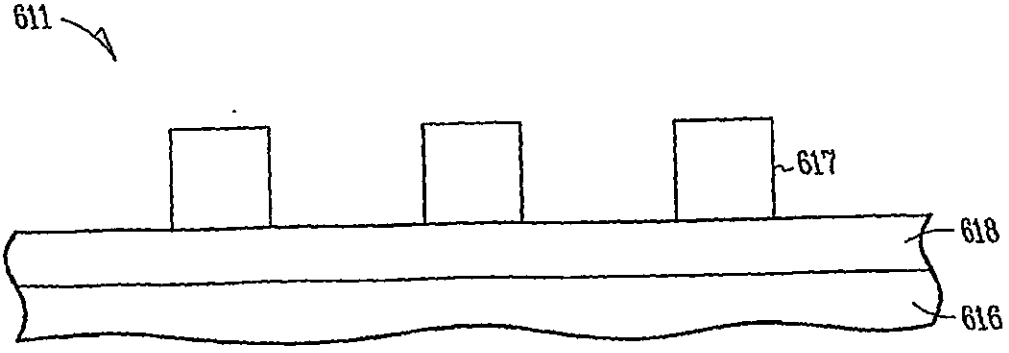


FIG. 6G

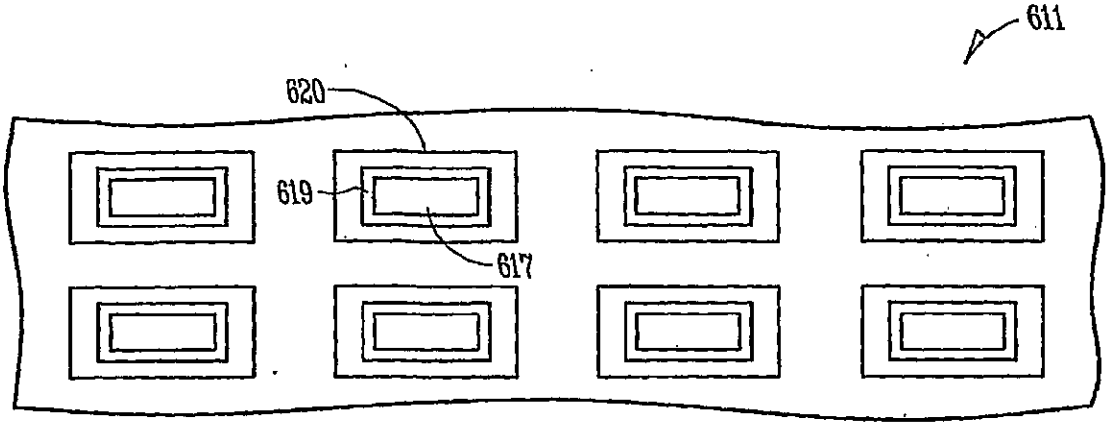


FIG. 6H

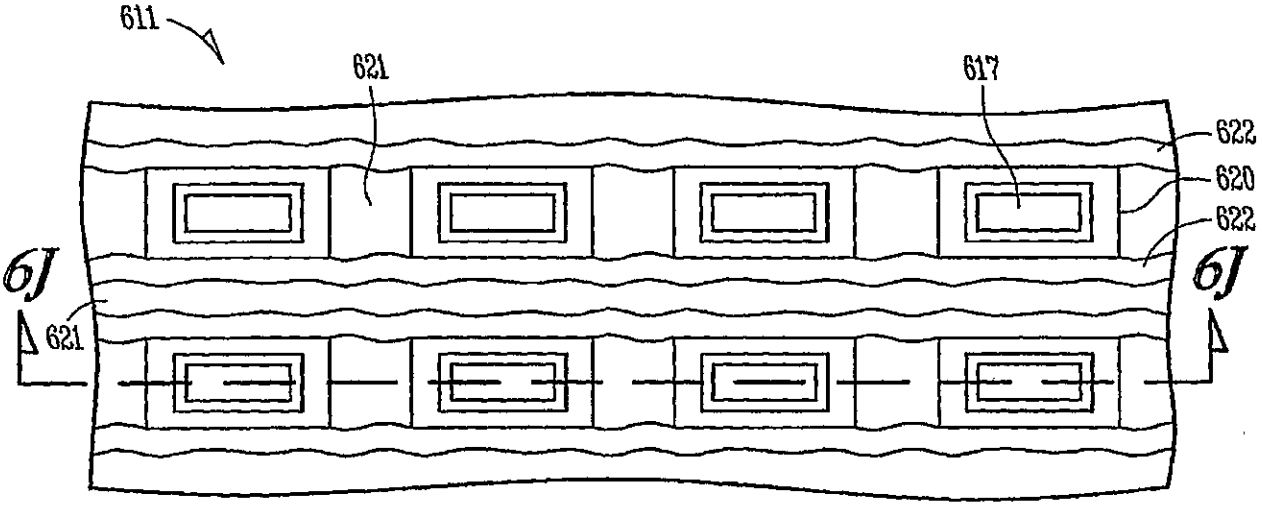


FIG. 6I

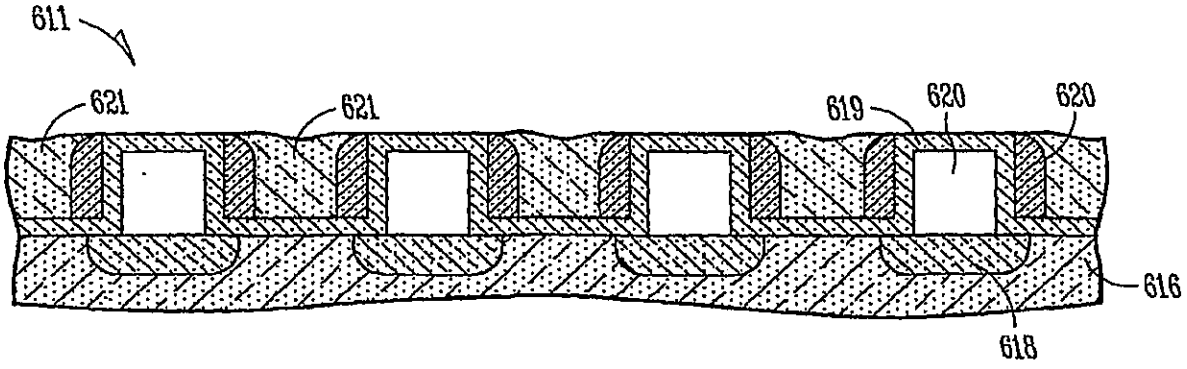


FIG. 6J

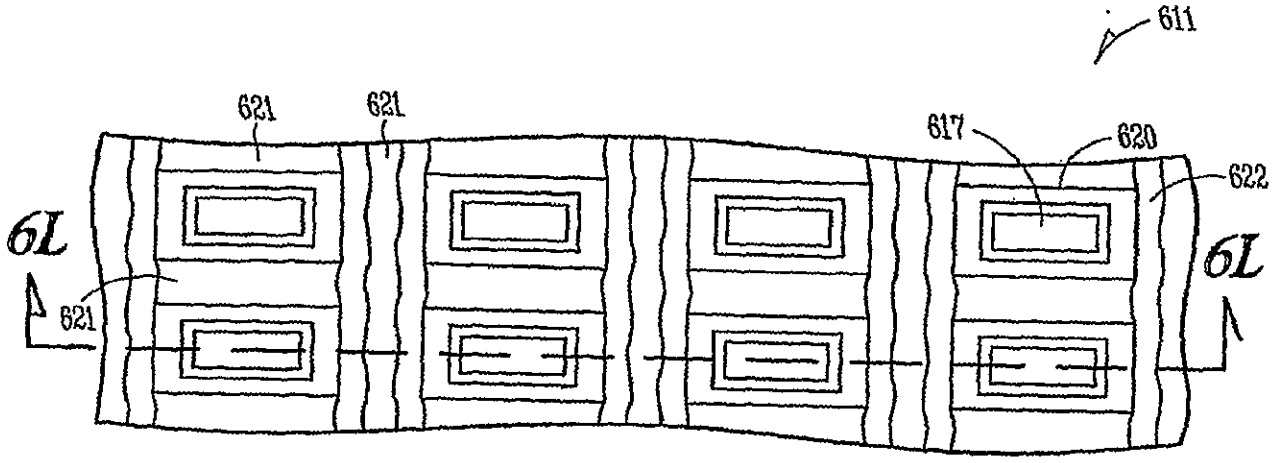


FIG. 6K

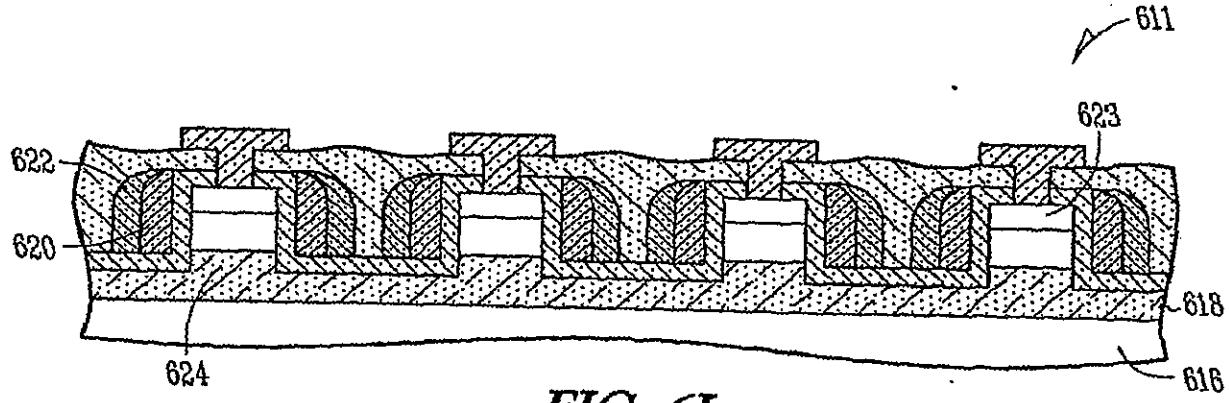


FIG. 6L

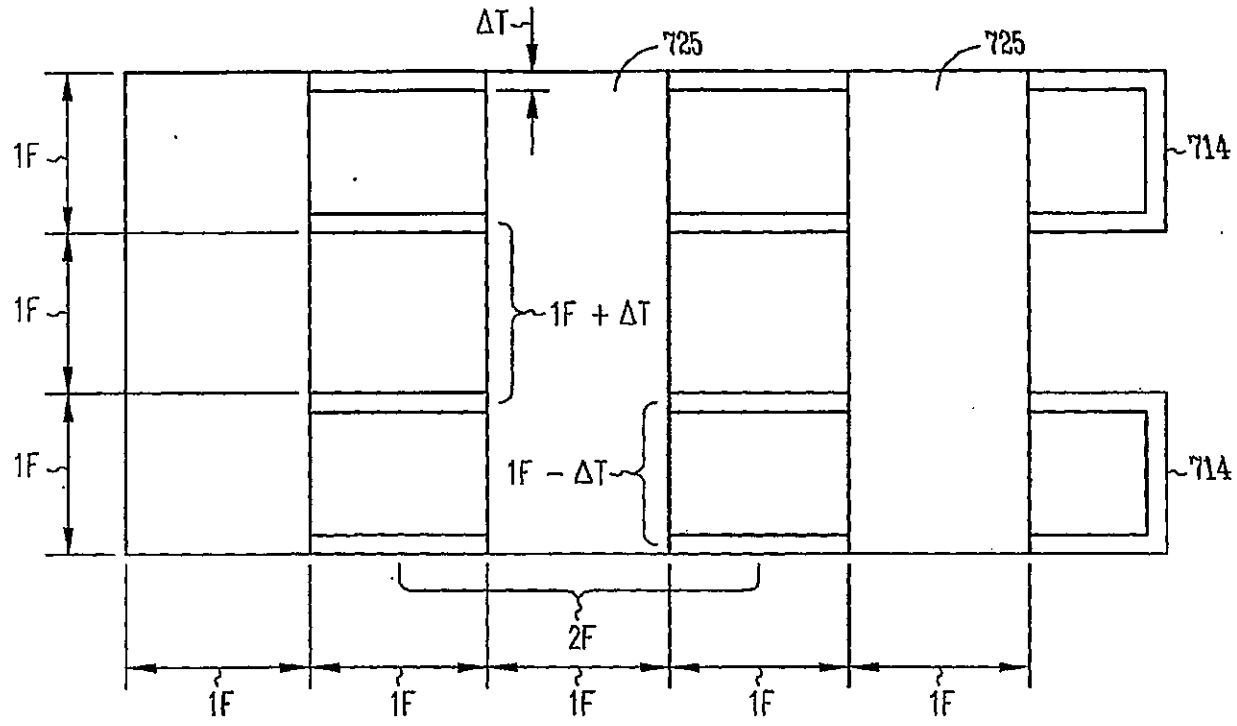


FIG. 7

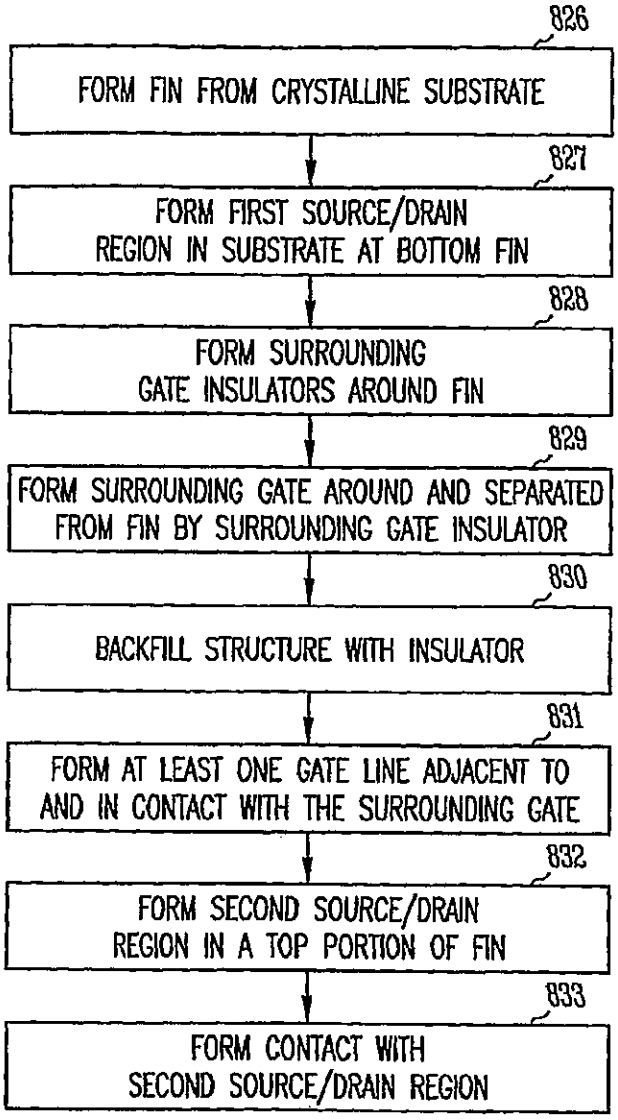

826
FORM FIN FROM CRYSTALLINE SUBSTRATE
827
FORM FIRST SOURCE/DRAIN REGION IN SUBSTRATE AT BOTTOM FIN
828
FORM SURROUNDING GATE INSULATORS AROUND FIN
829
FORM SURROUNDING GATE AROUND AND SEPARATED FROM FIN BY SURROUNDING GATE INSULATOR
830
BACKFILL STRUCTURE WITH INSULATOR
831
FORM AT LEAST ONE GATE LINE ADJACENT TO AND IN CONTACT WITH THE SURROUNDING GATE
832
FORM SECOND SOURCE/DRAIN REGION IN A TOP PORTION OF FIN
833
FORM CONTACT WITH SECOND SOURCE/DRAIN REGION

FIG. 8

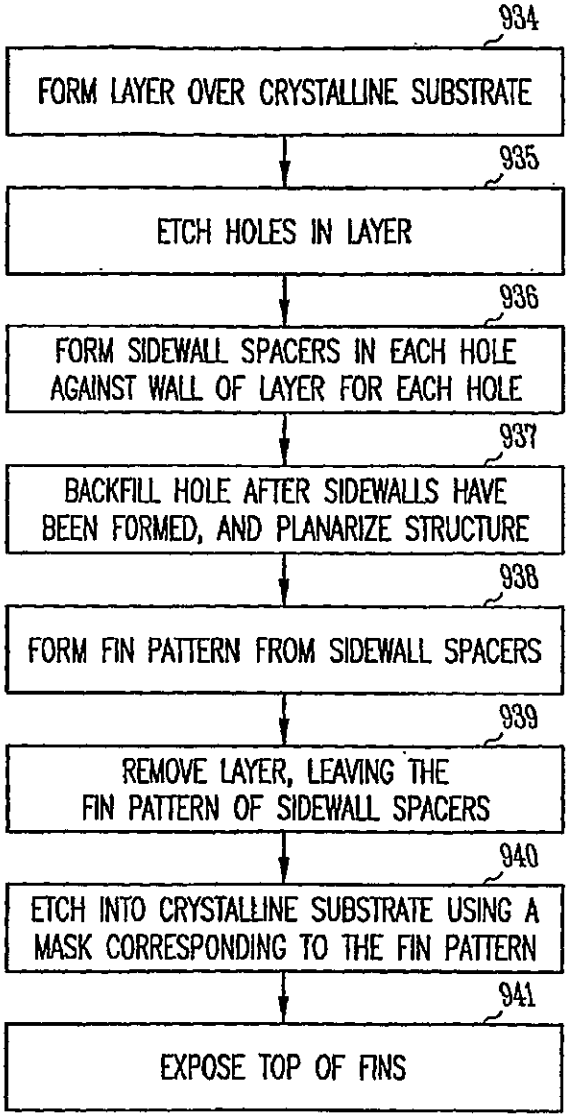

934
FORM LAYER OVER CRYSTALLINE SUBSTRATE
935
ETCH HOLES IN LAYER
936
FORM SIDEWALL SPACERS IN EACH HOLE AGAINST WALL OF LAYER FOR EACH HOLE
937
BACKFILL HOLE AFTER SIDEWALLS HAVE BEEN FORMED, AND PLANARIZE STRUCTURE
938
FORM FIN PATTERN FROM SIDEWALL SPACERS
939
REMOVE LAYER, LEAVING THE FIN PATTERN OF SIDEWALL SPACERS
940
ETCH INTO CRYSTALLINE SUBSTRATE USING A MASK CORRESPONDING TO THE FIN PATTERN
941
EXPOSE TOP OF FINS

FIG. 9

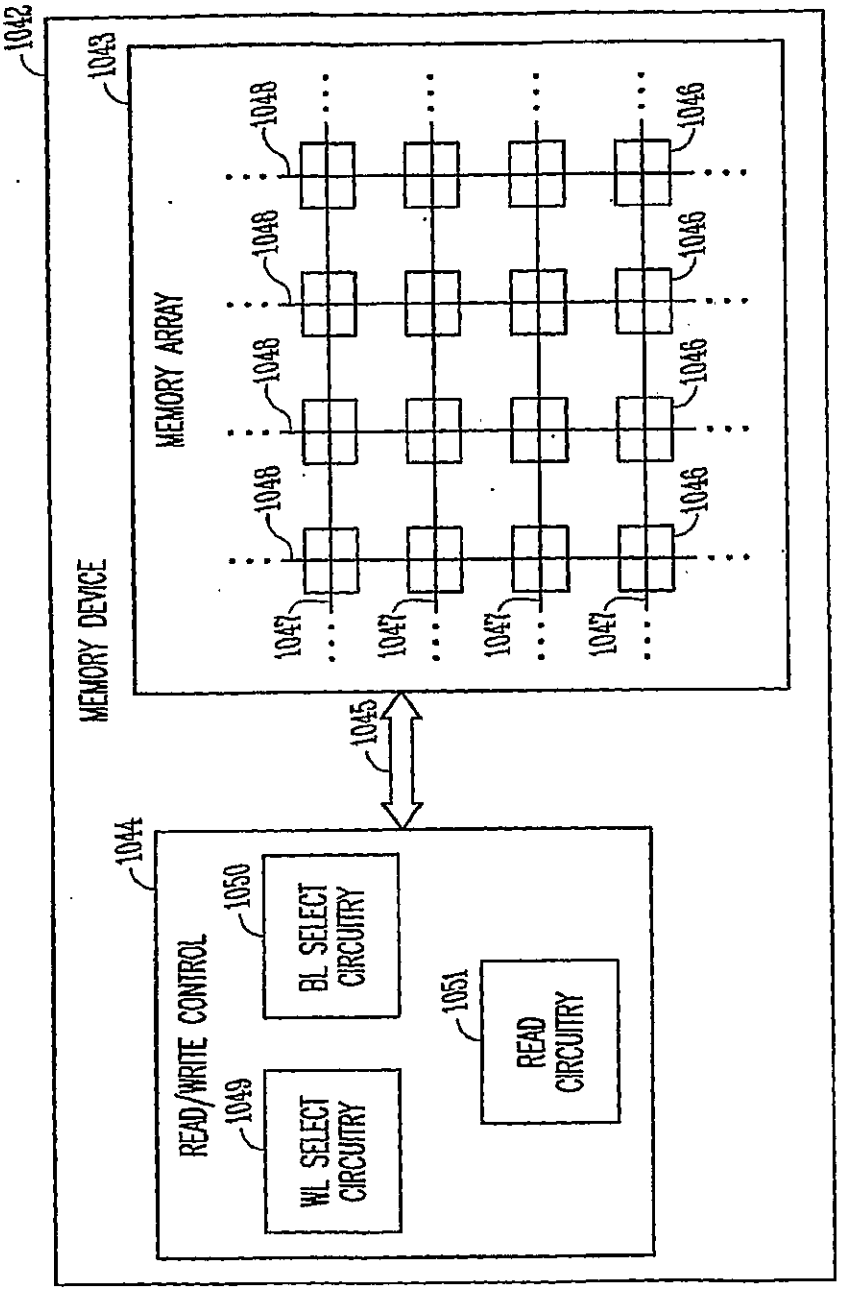

1042
MEMORY DEVICE
1043
MEMORY ARRAY
1048
1046
1047
1045
1044
READ/WRITE CONTROL
1050
BL SELECT CIRCUITRY
1049
WL SELECT CIRCUITRY
1051
READ CIRCUITRY

FIG. 10

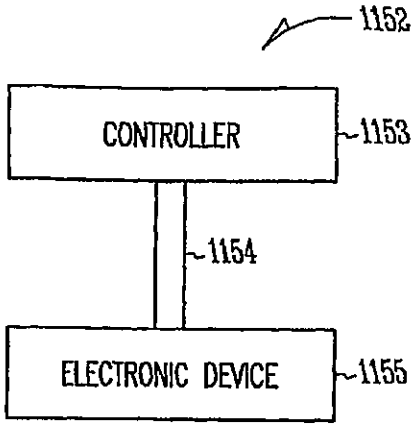

1152
CONTROLLER
1153
1154
ELECTRONIC DEVICE
1155

FIG. 11

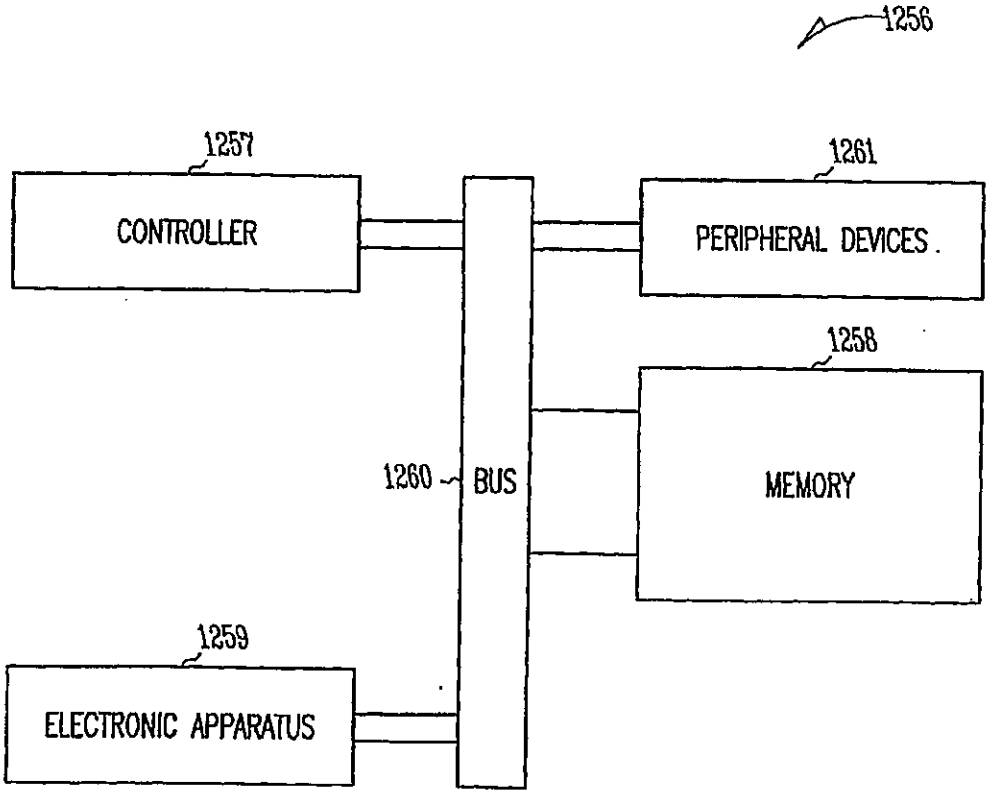

1256
1257
CONTROLLER
1261
PERIPHERAL DEVICES
1258
MEMORY
1260
BUS
1259
ELECTRONIC APPARATUS

FIG. 12