

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO MEMORY APPARATUS

(See Erratum)

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195, Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to memory apparatus.

In many computers and other systems a need exists for large information capacity semiconductor memories in which information can be temporarily stored and then retrieved within a useful period of time. In view of this, it is desirable that each individual memory cell of the array require as little semiconductor area for its implementation as possible and contain as few terminals as possible. It is also necessary to consider the semiconductor area required for the peripheral circuitry associated with the memory.

In the publication *Electronics* of March 1, 1971, an article entitled "Bipolar Memory Cells Strike Back in War with MOS" on page 19, and the copending G.B. application No. 60,662/71 serial no. 1 358 190), a two-terminal memory cell comprising a single junction transistor is described. The described structure requires a fairly small semiconductor area for its implementation and contains only two terminals, but requires avalanche breakdown of one of the junctions of the transistor. In addition, the readout signal from the cell is a transient response that destroys the information stored in the cell.

The copending G.B. application No. 55,826/72 (serial no. 1 393 264) describes a semiconductor memory array comprising a plurality of interconnected two-terminal memory cells, each comprising an NPN and

a PNP transistor. While this memory cell has many desirable electrical characteristics and does not utilize avalanche breakdown, it still produces a transient output signal that destroys the information stored in the cell. Because of the transient output signal, fairly sophisticated detection circuits, which require considerable semiconductor area, are utilized to form a workable memory system.

A memory cell of relatively small size which does not utilize avalanche breakdown or have destructive transient readout would be very desirable for use in large information capacity semiconductor memories.

According to this invention memory apparatus includes a plurality of memory cells each for storing binary information and each including first and second terminals, a junction bipolar transistor and a field effect transistor, the emitter of said bipolar transistor and the source of said field effect transistor comprising said first and second terminals respectively, the base of said bipolar transistor being coupled to the drain of said field effect transistor, the collector of said bipolar transistor being coupled to the gate of said field effect transistor, capacitance being provided at said gate, and an asymmetrically conductive path between said second terminal and said gate for selectively coupling said capacitance to said second terminal, said apparatus being such that, in operation, binary information stored in said cells is non-destructively readable.

Said field effect transistor may be of the junction type and said path may be the source-gate junction thereof. Said bipolar transistor may be of the NPN-type and said junction field effect transistor may be of the P-channel type. Alternatively, said bipolar transistor may be of the PNP-type and said junction field effect transistor may be of the N-channel type.

Said field effect transistor may be an

insulated gate field effect transistor and said path may comprise an asymmetrically conductive device coupled between the source and the gate thereof.

- 5 First and second control means may be coupled to the first and second terminals of each said cell respectively. Said first and second control means may each comprise voltage pulse circuits.
- 10 Said first and second control means may be adapted to cooperate for selectively (i) forward biasing said path of a selected cell while inhibiting conduction of the bipolar transistor of said selected cell in order to establish a first potential level, representative of one binary value, at the gate of the field effect transistor of said selected cell, (ii) forward biasing said path of a selected cell while causing conduction of the bipolar transistor of said selected cell in order to establish a second potential level, representative of the other binary value, at the gate of the field effect transistor of said selected cell, and (iii) causing the binary value represented by a said first or a said second potential level in a selected cell to be non-destructively read out.

Means may be coupled to the first terminal of each said cell for detecting conduction of the bipolar transistor of each said cell.

The invention will now be described with reference to the accompanying drawings in which:

- 35 FIG. 1 illustrates in block circuit form a memory system embodying the invention; FIG. 2 illustrates a schematic circuit of a memory cell suitable for use in the memory system of FIG. 1;
- 40 FIGS. 3 and 4 graphically illustrate the potentials applied to the terminals of the memory cell of FIG. 2 as a function of time; and

FIGS. 5 and 6 illustrate the corresponding potential of the gate of the JFET as a function of time and conduction through the NPN transistor as a function of time.

- The basic elements of a word-organised memory system 10, of Fig. 1 includes a plurality of individual memory cells 12 arranged in a two-dimensional array of N rows and M columns to form a memory having MXN memory cells. Each of the memory cells 12 which has two terminals, 14 and 16, is capable of storing bit information for a useful period of time. Terminal 16 is connected to a word line 18 and terminal 14 is connected to a digit line 20. All of the word lines 18 are connected to word line voltage control circuits 22 and all of the digit lines 20 are connected to digit line voltage control circuits 24 and conduction detectors 26.

Referring to Fig. 2, the cell shown inside the broken line rectangle 12 comprises a

preferred embodiment of the inner structure of cell 12 of FIG. 1. As illustrated, the cell comprises a P-channel JFET 30 and an NPN junction transistor 32. The gate and drain of the JFET 30 are respectively coupled to the collector and the base of NPN transistor 32. The common node of the gate and the collector is denoted as "34". The common node of the drain and the base is denoted as "35". The emitter of NPN transistor 32 constitutes terminal 14 and the source of JFET 30 constitutes terminal 16 of the memory cell. Capacitance C represents the equivalent parasitic capacitance associated with the gate of JFET 30 and the collector of NPN transistor 32.

The typical operation of the memory cell of FIG. 2 can be easily seen from the voltage and current graphs of FIGS. 3, 4, 5 and 6. FIGS 3 and 4 illustrate the potentials which are a function of time, applied to terminals 16 and 14 by the word line control circuits 22 through word line 18, and the digit line control circuits 24, through digit line 20, respectively. FIG. 5 illustrates the corresponding potential of the node 34 as a function of time. FIG. 6 illustrates the current flowing through transistor 32 as a function of time. In order to simplify the discussion of the operation of a single memory cell, the dashed-line waveforms of FIGS. 3, 4 and 6 will be ignored for the present. They will be discussed later in connection with the memory array of FIG. 1.

As illustrated in FIGS. 3 and 4 at $T = t_1$ the terminals 14 and 16 are held at a reference potential which is typically ground potential. FIG. 5 illustrates that the potential of node 34 is assumed to be at a potential close to the reference potential which is defined at a "0" level. Typically the "0" potential is 0.2 volt. FIG. 6 illustrates that there is no conduction in transistor 32 at $T = t_1$.

In order to write a "1" into cell 12, a positive polarity voltage pulse, the amplitude of which is greater than the pinchoff voltage of JFET 30, is applied to node 16 by the word line control circuits 22 through word line 18 between $T = t_1$ and t_2 . At the same time a positive polarity voltage pulse of approximately the same amplitude as that applied to node 16 is applied to terminal 14 by digit line control circuits 24 through digit line 20. The voltage pulse applied to terminal 16 causes the source gate junction of JFET 30 to be forward-biased and consequently for node 34 to be charged to a value close to that of the amplitude of the applied pulse. This value is defined as a "1". The voltage pulse applied to terminal 14 prevents NPN transistor 32 from conducting. Typically the amplitude of the write pulse applied to ter-

terminal 16 is +5 volts and a "1" potential level is 4.6 volts.

At $T = t_1$ the word line voltage and the digit line voltage both return to the reference potential. Capacitance C maintains the potential on node 34 at approximately the potential attained during the period from $T = t_2$ to t_4 .

At $T = t_5$ a positive polarity read voltage pulse is applied to terminal 16 while terminal 14 is held at the reference potential. The amplitude of this read pulse is less than that of the write pulse. Typically the amplitude of the read pulse is +1 volt. If the cell stores a "1" the source gate potential is above the pinchoff voltage and consequently neither the JFET or the NPN transistor turns on. As is illustrated in FIG. 6, during the time from $T = t_5$ to t_6 , there is substantially no flow of current through NPN transistor 32. This corresponds to the existence of a "1" stored in memory cell 12. It is to be noted that at $T = t_{6+}$ the potential of node 34 remains at the "1" level. This means that the readout of a "1" has not destroyed the stored "1".

In order to write a "0" into a cell which stores a "1", the same pulse applied to terminal 16 to write a "1" into the cell is again applied, but terminal 14 is now held at the reference potential. This causes the source gate junction of JFET 30 to be forward biased and the gate potential to be above the pinchoff voltage, thereby causing conduction in JFET 30 and transistor 32. Transistor 32 conducts in a saturation mode, and, therefore, the collector (node 34) potential is at just a few tenths of a volt above the reference potential. This means, as is illustrated in FIG. 5 at $T = t_{6+}$, that the potential of node 34 is typically +0.2 of a volt, which is defined as a "0" level. Capacitance C maintains this potential after the write pulse subsides and until another read pulse is applied to the cell.

In order to read out the "0" now stored in the cell, a positive polarity voltage pulse is applied to terminal 16 between $T = t_{11}$ and t_{12} . This pulse is substantially the same as the read pulse applied during $T = t_5$ and t_6 . During the time from $T = t_{11}$ to t_{12} , terminal 14 is held at the reference potential. As a consequence of the potentials applied to terminals 14 and 16 and the fact that node 34 is at the "0" level there is steady state d.c. conduction established in transistor 32 in the time period between $T = t_{11}$ and t_{12} , as is illustrated in FIG. 6. This conduction is indicative of a "0" stored in the cell. It is to be noted that at $T = t_{12+}$ the potential of node 34 is still at the "0" potential. This means that the readout of a "0", like the readout of a "1", does not destroy the information stored in the cell. Typically the time duration between

$T = t_x$ and $T = t_{x+1}$, where $1 \leq x \leq 11$, is 20 nanoseconds.

As has been discussed, the reading out of stored information from a memory cell does not destroy the information stored in the cell. In addition, the readout of a "0" causes d.c. current to flow between the word line and the digit line. The existence of this d.c. readout makes possible the use of relatively simple detection circuits. Consequently, these detection circuits can be fabricated in a relatively small area of silicon, thereby making the total memory system relatively compact.

The memory cell of FIG. 2 may be fabricated in approximately 3 mils square of semiconductor area. Starting with a p-type semiconductive substrate, an (n+)-type buried layer is selectively deposited into the substrate. A p-type epitaxial layer is then grown and converted to silicon dioxide except in the area overlying the (n+)-type diffusion. Two separate (n+)-type diffusions are then made into the remaining p-type epitaxial layer. A contact made to the p-type epitaxial layer serves as the source terminal of the cell and a contact made to one of the two n+ diffusions in the p-type epitaxial layer serves as the emitter terminal. The second n+ diffusion serves as the collector and gate of the memory cell while the portion of the epitaxial layer between the two (n+)-type diffusions serves as the drain and base. The capacitance associated with the gate and collector is enhanced by the (n+)-type buried layer.

One major advantage of the memory cell of FIG. 2 is that the physical size of the cell can be reduced without any loss in output signal. This is because charge stored in C of FIG. 2 does not become part of the output signal as is true in other dynamic memory cells.

In order to utilize the cell of FIG. 2 in a word organized memory, like the memory of FIG. 1, several minor changes are made in the waveforms of FIGS. 3 and 4. The dashed line voltage pulses of FIG. 3 applied between the times $T = t_1$ and t_2 and $T = t_7$ and t_8 are similar to the read pulses applied between $T = t_5$ and t_6 and $T = t_{11}$ and t_{12} . These dashed line pulses, like the read pulses, cause information stored in the cells to be read out and detected. Prior to writing into a selected cell of a particular word line, it is necessary to know what information is stored in all of the cells coupled to that word line, such that during the time information is written into the selected cell, information stored in these cells may be maintained.

Normally the digit line potentials are left at the reference potential except during the time a "1" is written into a particular cell. If it is determined, after the application of 130

the first dashed line read pulse of FIG. 3 that a cell coupled to the same word line as the selected cell contains a "1", then the digit line control circuits cause a voltage pulse to be applied to the digit line corresponding to that cell during the time ($T = t_2$ to t_3) a "1" is written into the selected cell in order to ensure that the "1" stored in this other cell is maintained. If this other cell contains a "0", then the corresponding digit line potential is kept at the reference potential to ensure that the stored "0" is maintained.

The dashed line voltage pulse of FIG. 4 which appears between $T = t_2$ and t_3 is utilized to ensure that proper "1"s are maintained in memory cells coupled to the word line corresponding to the selected cell during the time information is written into the selected cell. If it were not for this pulse and like pulses applied to the other digit lines, there could be an initial relatively large flow of current from the word line circuits which could tend to load down the word line circuits and lower the amplitude of the write voltage pulse, thereby decreasing the potentials of the "1"s stored in memory cells coupled to the selected word line.

As is illustrated in FIG. 6, there is substantially no current flow in the selected cell between $T = t_2$ and t_3 if the dashed pulse of FIG. 4 is utilized. This is to be contrasted with the d.c. type of current flow illustrated during the same period of time if the dashed pulse of FIG. 4 is not utilized.

Various modifications are possible for example, an N-channel JFET and a PNP transistor may be substituted for the P-channel JFET and the NPN transistor provided the relevant voltages are reversed. Still further, an insulated gate field effect transistor with a diode coupled between the source and gate could be substituted for the JFET, the anode of the diode being coupled to the source and the cathode being coupled to the gate.

WHAT WE CLAIM IS:—

1. Memory apparatus including a plurality of memory cells each for storing binary information and each including first and second terminals, a junction bipolar transistor and a field effect transistor, the emitter of said bipolar transistor and the source of said field effect transistor comprising said first and second terminals respectively, the base of said bipolar transistor being coupled to the drain of said field effect transistor, the collector of said bipolar transistor being coupled to the gate of said field effect transistor, capacitance being provided at said gate, and an asymmetrically conductive path between said second terminal and said gate for selectively coupling

said capacitance to said second terminal, said apparatus being such that, in operation, binary information stored in said cells is non-destructively readable.

2. Memory apparatus as claimed in claim 1 wherein said field effect transistor is of the junction type and said path is the source-gate junction thereof.

3. Memory apparatus as claimed in claim 2 wherein said bipolar transistor is of the NPN-type and said junction field effect transistor is of the P-channel type.

4. Memory apparatus as claimed in claim 2 wherein said bipolar transistor is of the PNP-type and said junction field effect transistor is of the N-channel type.

5. Memory apparatus as claimed in claim 1, wherein said field effect transistor is an insulated gate field effect transistor and said path comprises an asymmetrically conductive device coupled between the source and the gate thereof.

6. Memory apparatus as claimed in any one preceding claim including first and second control means coupled to the first and second terminals of each said cell respectively.

7. Memory apparatus as claimed in claim 6 wherein said first and second control means each comprises voltage pulse circuits.

8. Memory apparatus as claimed in claim 6 or 7 wherein said first and second control means are adapted to cooperate for selectively (i) forward biasing said path of a selected cell while inhibiting conduction of the bipolar transistor of said selected cell in order to establish a first potential level, representative of one binary value, at the gate of the field effect transistor of said selected cell, (ii) forward biasing said path of a selected cell while causing conduction of the bipolar transistor of said selected cell in order to establish a second potential level, representative of the other binary value, at the gate of the field effect transistor of said selected cell, and (iii) causing the binary value represented by a said first or a said second potential level in a selected cell to be non-destructively read out.

9. Memory apparatus as claimed in claim 8 including means coupled to the first terminal of each said cell for detecting conduction of the bipolar transistor of each said cell.

10. Memory apparatus adapted and arranged to operate substantially as herein described with reference to the accompanying drawings.

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