

ABSTRACT

Embodiments of the present application provide an integrated circuit and a layout method thereof. First, a first pitch of a first standard cell having a maximum gate length in multiple standard cells in an integrated circuit is determined. The first pitch
5 is a distance between a central axis of a polysilicon gate in the first standard cell and central axes of virtual polysilicon gates in the first standard cell. Then, a distance between a polysilicon gate and virtual polysilicon gates in each of the standard cells is adjusted by using the first pitch and a gate length of each of the standard cells. After the adjustment, a distance between a central axis of the polysilicon gate in each of the
10 standard cells and central axes of the virtual polysilicon gates in each of the standard cells is the same as the first pitch. In this way, after standard cells having different gate lengths are integrated, a size of a space occupied by each of the standard cells is not affected by the gate length, thereby effectively reducing errors in key graphic dimensions during integrated circuit production and improving performance of the
15 integrated circuit.

FIG. 3