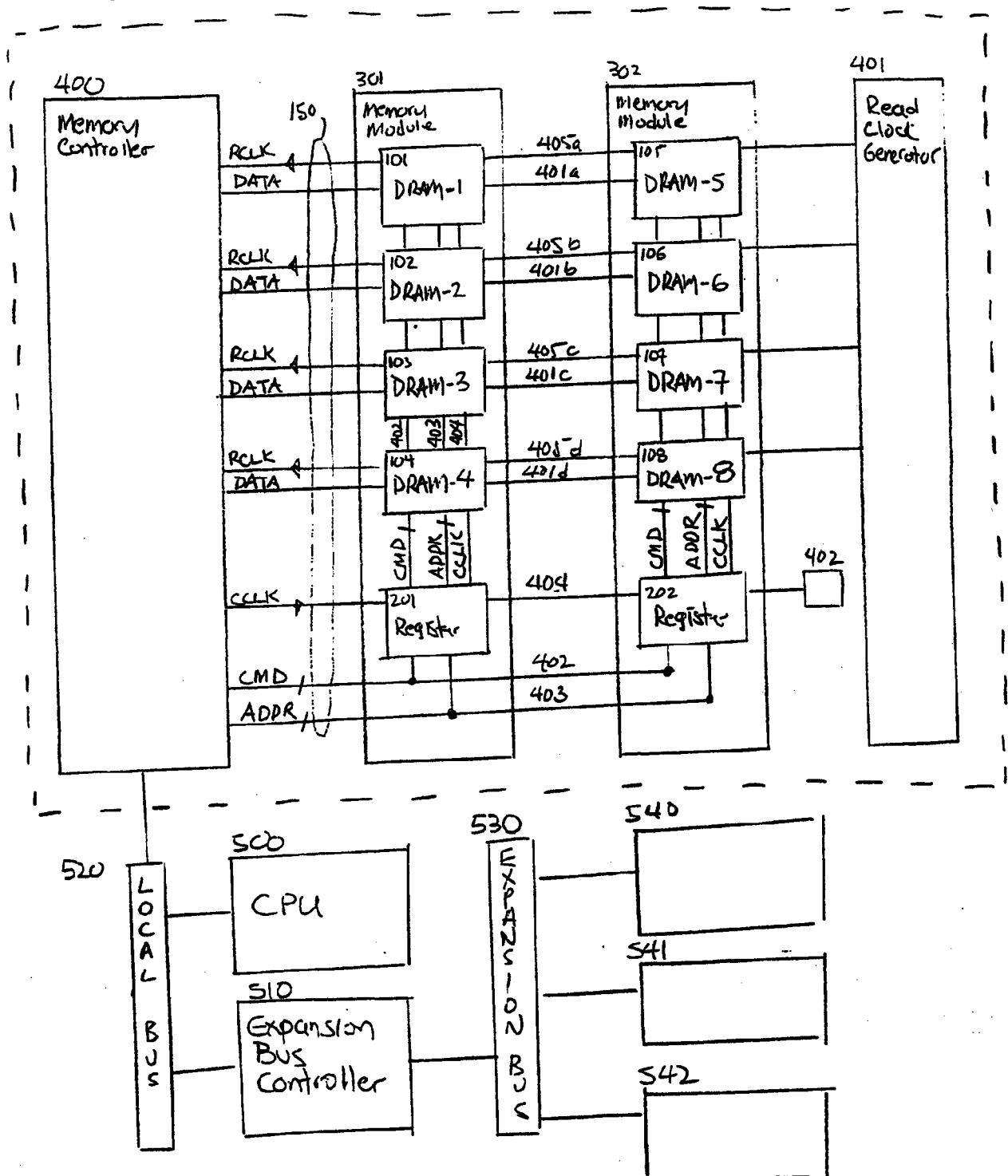


100



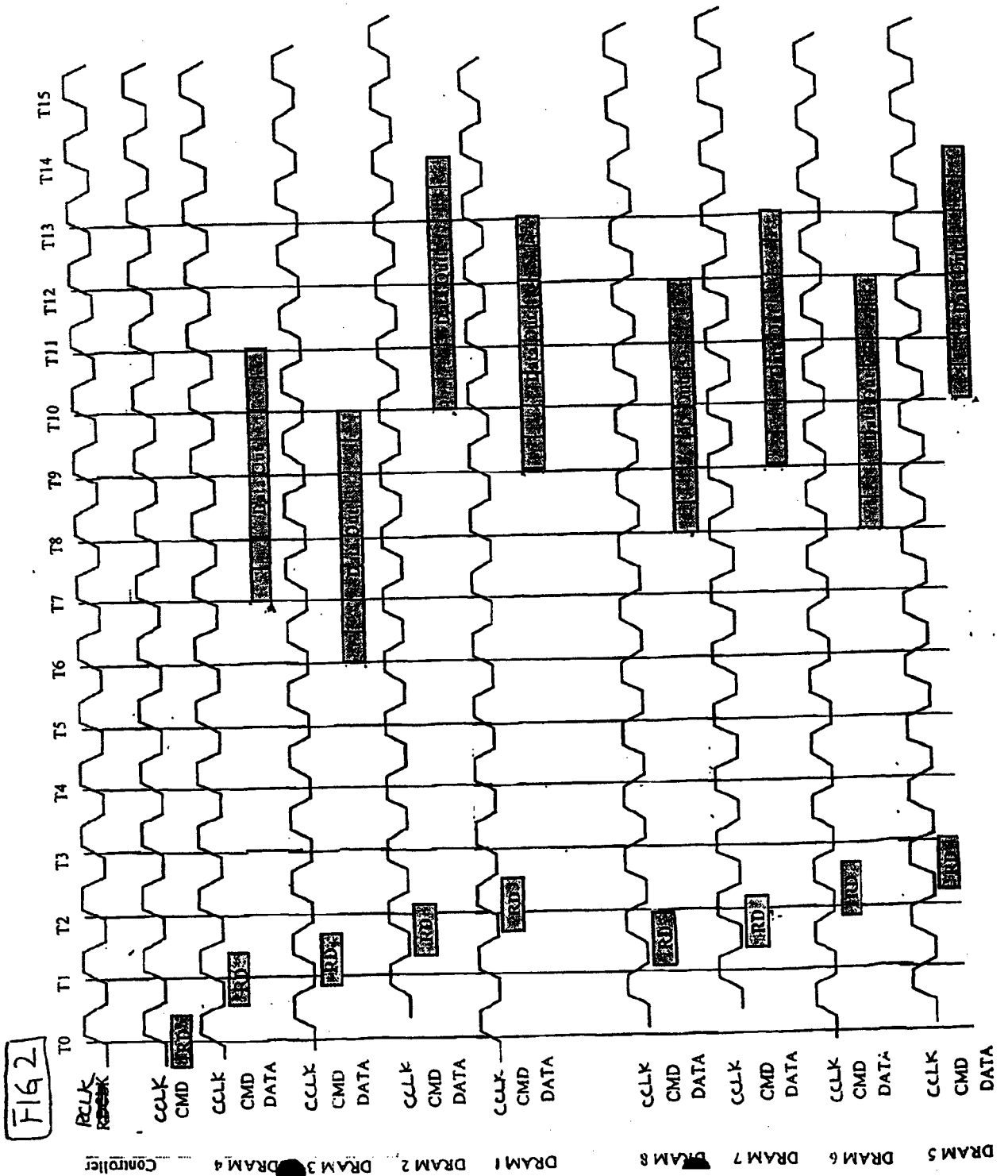


FIG. 3A

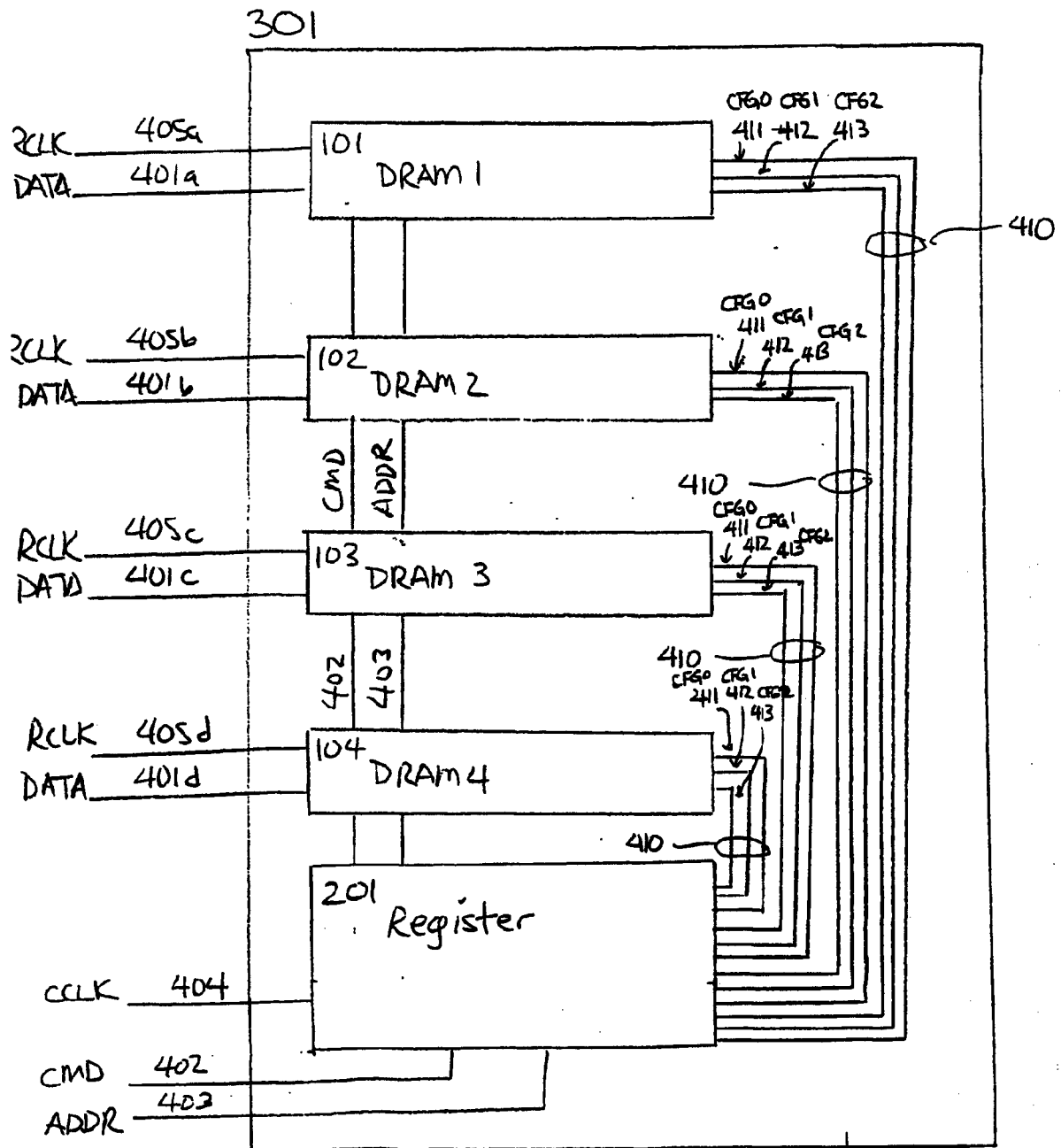


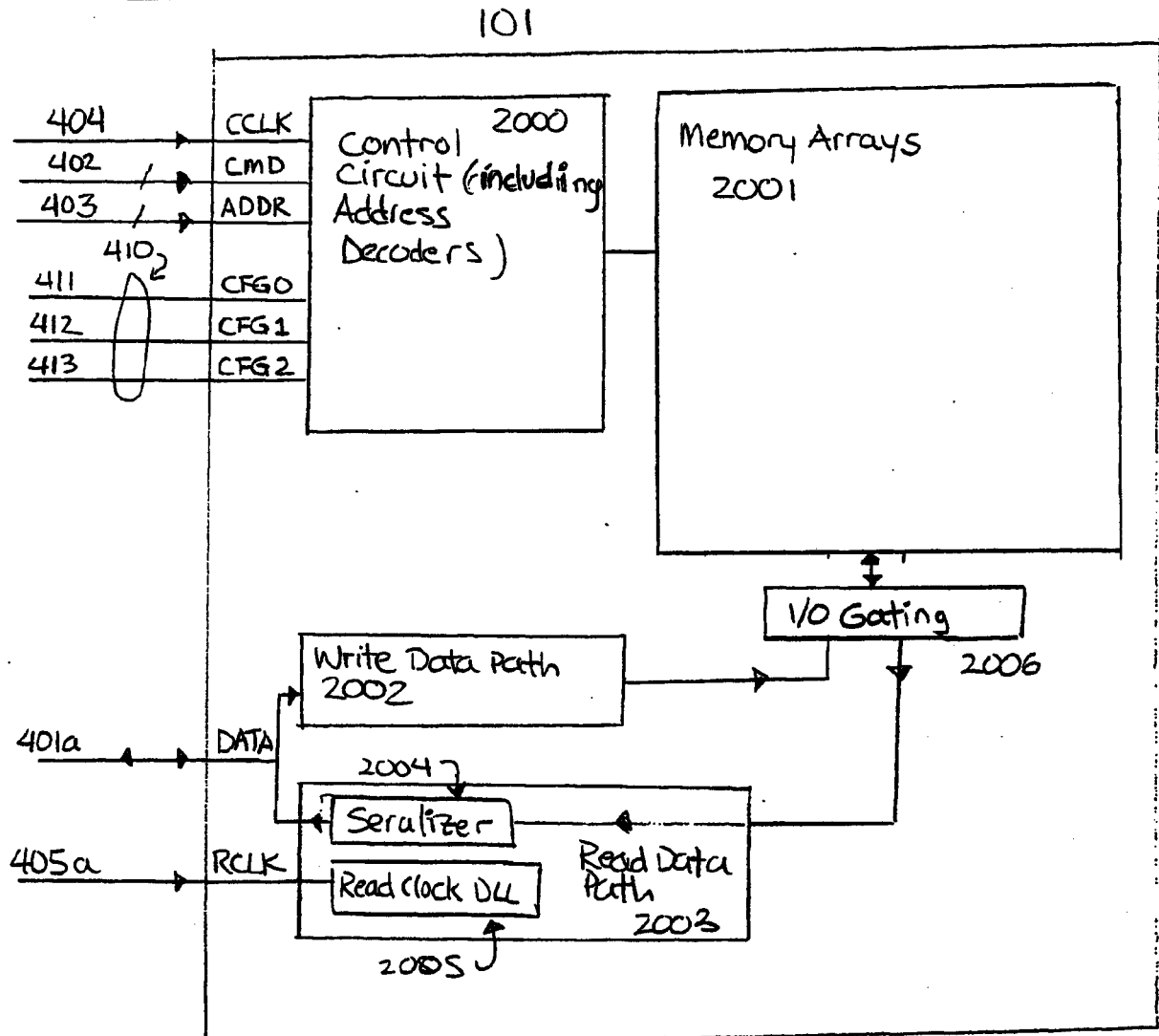
FIG 3B

FIG. 4

Device Read Latency	CFG2	CFG1	CFG0
Minimum Device Read Latency	0	0	0
Minimum Device Read Latency + 1 clock cycle	0	0	1
Minimum Device Read Latency + 2 clock cycles	0	1	0
Minimum Device Read Latency + 3 clock cycles	0	1	1
Minimum Device Read Latency + 4 clock cycles	1	0	0
Minimum Device Read Latency + 5 clock cycles	1	0	1
Minimum Device Read Latency + 6 clock cycles	1	1	0
Minimum Device Read Latency + 7 clock cycles	1	1	1

FIG. 5

