ABSTRACT

A synchronous LSI memory device, comprises memory cell array sections (BK1, BK2) each having a plurality of memory cells; a timing generating section (CLOCK MASKED SECT) for generating a first basic signal (CPOR) synchronous with a clock signal (CLK) and masked according to the status of a control signal (CKE); a signal generating section (SERIAL SYS CONTROL) for generating a second signal (CP) in synchronism with the first basic signal (CPOR) and stopping generating the second signal after a predetermined number of accesses or in response to a stop signal (MRRST, MWSTP, LADA, BSTP); and a control section (SHIFT REGISTER) for controlling the cell array sections (BK1, BK2) on the basis of outputs of the timing signal generating section and the signal generating section. In the synchronous LSI memory device, it is possible to operate the memory device whose access speed is lower than the CPU on the basis of a single high speed clock signal suitable for the CPU, so that the it is possible to simplify the clock control so as to be correspond to the higher speed CPU without complicating the system configuration.

(Fig. 4)

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