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IMPROVED DRAM CHIP FABRICATION METHOD

ABSTRACT OF THE DISCLOSURE

An improved method for forming a DRAM chip (10) is disclosed. According to this method, a memory cell gate (26) is deposited in a memory cell array area (12) of the DRAM chip (10). The memory cell gate (26) overlies a first channel area of a substrate. A peripheral gate (32) is deposited in a peripheral area of the DRAM chip. The peripheral gate overlies a second channel area of the substrate. A first dopant is implanted with a first concentration in a first plurality of source and drain regions (30) of the substrate lying predominantly outside the first and second channel areas of the substrate. A sidewall is then formed adjacent to the peripheral gate (32). Simultaneously, an insulating layer (28) is formed over the memory cell array area of the DRAM chip (10). A second dopant is implanted with a second concentration in a second plurality of source and drain regions (36) of the substrate within the peripheral area (14) of the DRAM chip (10). The implant of the second dopant is blocked by the sidewall and the insulating layer. In one embodiment, the first and second dopants are the same, and the dopant concentration in the second plurality of regions is greater than the dopant concentration in the first plurality of regions. This method allows the formation of more heavily doped source and drain regions (36) in the peripheral area of the DRAM chip while keeping the heavily doped regions separated from the channel regions. This reduces diffusion into the channel regions and allows a smaller design rule to be used.

Figure 1

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