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Stacked Wafer for 3D Integration

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Field of the Invention

The invention relates to stacked wafers for the integration of multiple wafer platforms into a single scaled package. In particular, the invention relates to a method for creating said packages so as to combine multiple components within a single integrated structure.

Background

The semiconductor industry has been searching for a viable solution for wafer level integration for years, for it allows IC design on a monolithic substrate to be partitioned and recombined using large numbers of very short vertical interconnections. The IC's thus fabricated offer higher density and speed due to smaller die size and correspondingly shorter RC delays. Processes that are not compatible e.g., analog and digital can be fabricated using fully optimized processes on separate wafers (without compromising function) and then re-combined to generate a 3 dimensional (3D) IC. As a consequence, heterogeneous substrate integration at wafer level for ultra high performance will be achievable (e.g., Si and SiGe for digital and RF components respectively).

3D integration involves the integration of specific components such as memory, sensors and the like. Said components are fabricated on individual substrates and then

bonded to form a single package containing several devices. To maintain the package at a size that is usable within state-of-the-art applications, it is necessary to thin the wafers upon which the individual devices are located so that the overall size of the 3D integrated package is comparable with the size of a single device as currently used.

Apart from the size benefits of containing multiple devices within a single package, 3D integration also provides for combining incompatible technologies whilst improving speed performance and functionality of the package devices. Thus, whereas without 3D integration, multiple devices may be separated by larger distances requiring additional wiring or further for completely incompatible technologies said devices may rely on external wiring further diminishing the performance of the combined system.

A 3D integrated package or system-in-a-package (SIP) can reduce or eliminate the external wiring associated with non-integrated devices leading to a reduction in manufacturing cost whilst improving performance and so keeping abreast of the requirements of new end-product applications.

Thus, any attempt to combine multiple devices at the chip level requires external wiring and therefore seriously affect the performance of the device. Alternatively, attempts to create a 3D integration have been attempted at the transistor level, whereby multiple devices are connected through transistors whilst still in the same stack. Whilst achieving better results in terms of size than at the chip level, integration at the transistor level has limited effect on the speed of the integrated device. In any event, the construction of such a stacked device involves considerably greater levels of

manufacturing cost as connectivity between devices require a more complex connection in order to achieve the desired result.

Summary of Invention

Therefore, the object of the invention is to provide a method of forming an integrated package without having the problems of the prior art.

In a first aspect, the invention provides a method of forming a stacked wafer device comprising the steps of providing a first wafer; forming a plurality of copper pads in a first surface of the first wafer; forming at least one embedded vertical connector in the first wafer in isolation from the copper pads of the first wafer; providing a second wafer; forming a plurality of copper pads in a first surface of the second wafer, the placement of the copper pads to coincide with the location of the copper pads of the first wafer; forming at least one embedded vertical connector in the second wafer in isolation from the copper pads of the second wafer; bringing the first surfaces of the wafers into contact, so as to contact the copper pads; applying a force to the wafers at a pre-determined pressure and at a pre-determined temperature until the copper pads are bonded, and so forming the stacked wafer device from the bonded first and second wafer.

Thus, the wafers are brought into contact at the pads, and subjected to heat and pressure for a specified period in order to achieve thermal diffusion of the pads, and consequently the wafers.

Integration is a critical aspect of technology development. Whilst there has been considerable development through monolithic integration, there comes a point where further development is limited because of the need for a wide range of different material systems that must be used in a single device. The present invention provides for polylithic integration allowing each material to carry out the task to which it is best suited. By achieving true polylithic integration, a device constructed according to the present invention provides increased performance through greater speed, density, reliability, and power consumption.

As compared to other methods of construction such as Multi-Chip-Module (MCM), Multi-Chip-Package (MCP) or System-In-Package (SIP), where interconnections between layers may be limited to a few hundred or a few thousand inter-die connections, a device formed according to the present invention is capable of having several orders of magnitude more (of the order of a million).

Further, ULSI designs can be fractured into smaller components and recombined to generate higher yields. By having shorter connections, through greater integration, RC delays may be reduced resulting in lower power consumption and higher speed.

In a preferred embodiment, the embedded vertical connector may be separated from the substrate by a barrier layer.

In a preferred embodiment, the barrier layer may include a metal barrier layer comprising any one or a combination of: Ti, TiN, $Ti_xSi_yN_z$, Ta, TaN, $Ta_xSi_yN_z$, W, WN, and WN_2. In a further embodiment, the barrier layer may include an oxide layer. In a still further embodiment, the barrier layer may include a nitride layer.

In a preferred embodiment, the plurality of copper pads, which may be electrically connecting two joining wafers as well as bonding purpose, may be placed on the same plane with the dummy copper pads, which do not electrically connecting two joining wafers and only served for joining purpose.

In a preferred embodiment, the plurality of copper pads may be formed with more than two shapes of bonding pads on the same plane simultaneously.

In a preferred embodiment, the at least one embedded vertical connector may be formed by dry etch process utilizing fluorine based plasma. In a more preferred embodiment, the embedded vertical connector may extend into Si substrate from the IMD (inter-metal dielectric layer).

In a preferred embodiment, the embedded vertical connection depth embedded in Si substrate may be in the range of 4 – 10 μm deep. Further, the embedded vertical connector diameter size may be the range of 0.2 – 10μm.

In a preferred embodiment, the embedded vertical connector may be isolated by PECVD deposition of dielectric barrier layers, said layers may be composed of undoped-SiO2, tetraethyl-orthosilicate (TEOS), SiON, phosphosilicate glass (PSG),

fluorosilicate glass (FSG), SiOC, borophosphosilicate glass (BPSG) and SiN.

In a preferred embodiment, the thickness of the dielectric barrier layer may be in the range of 0.05μm to 0.3μm.

In a preferred embodiment, the ertical connector When Copper, tungsten, aluminum and their alloy are used for the embedded vertical connector claimed in 1.

In a preferred embodiment, the metallization of vertical connector may be formed by a dry etch process or a CMP process.

In a preferred embodiment, lithographic alignment targets such as stepper alignment targets may be formed simultaneously. Further, the dimension of alignment targets may be modified to have dimensions compatible with the diameters of the vertical connectors.

In a preferred embodiment, the Si etch stop layer, which may be relatively larger than vertical connector, may be formed simultaneously. Further, the dimension of the Si etch stop layer may be in the range of 1 μm to 100μm.

In a preferred embodiment, the protrusion of copper bonding pads surface from the dielectric surface may be formed by lowering the dielectric surface using a wet (or dry) etch process. Further, BOE (buffered oxide enchants) may be used for this process.

In a preferred embodiment, the copper surface may be wet cleaned using acetic acid with ammonium fluoride solution. Further, a 1:1:1 ratio of acetic acid: ammonium fluoride: DI water solution may be used. Further still, a 1:10:40 ratio of hydrogen peroxide: ethylenediamine: DI water solution may be used as a combined process.

In a more preferred embodiment, diluted ethylenediamine may be used as a combined process. Further, BAT (Benzene Triazole) may be used as a combined process.

In a preferred embodiment, fluorine based plasma may be used to project the copper pads above the wafer surface. Further, the surface of copper may be cleaned using Hydrogen plasma or Nitrogen plasma after or during the process.

In a preferred embodiment, thinning of the outer surfaces of the stacked (bonded) wafer may be formed either by grinding, CMP and wet/dry etch processes or combination of these.

In a preferred embodiment, the bottom surface of the embedded vertical connector may be used as a Si etch stop layer during thinning process.

In a preferred embodiment, Si may be thinned by wet etch using KOH base, TMAH base, EDP etching solution during the thinning. Alternatively, Si may be thinned by fluorine based plasma dry etch process. In a further alternative embodiment, Si may be thinned by CMP process.

In a preferred embodiment, laser or white light sources may be used to detect etch stop layer, which could be dielectric layer at the bottom of vertical connection via.

In a preferred embodiment, resistance measurement method on the polishing pad may be used to detect etch stop layer, which could be dielectric layer at the bottom of vertical connection via.

In a preferred embodiment, temperature measurement method on the polishing pad is used to detect etch stop layer which could be dielectric layer at the bottom of vertical connection via.

In a preferred embodiment, the Si may be further etched after bottom of vertical connection via has been detected. Further, the thickness of further etched Si may be in the range of 0.2μm to 2μm.

In a preferred embodiment, the etch stop layer detection signal may be captured from the big etch stop layer formed simultaneously during vertical connection via formation.

In a preferred embodiment, the dielectric layer may be planarized by dielectric CMP process. Alternatively, the dielectric layer may be planarized by blanket photo-resist etch-back process.

Brief Description of Drawings

It will be convenient to further describe the present invention with respect to the accompanying drawings that illustrate possible arrangements of the invention. Other arrangements of the invention are possible and consequently, the particularity of the accompanying drawings is not to be understood as superceding the generality of the preceding description of the invention.

Figure 1a is an elevation view of a CMOS wafers according to a first embodiment of the present invention;

Figure 1b is an elevation view of a CMOS wafers according to a second embodiment of the present invention;

Figure 2 is an elevation view of an embedded vertical connector according to an embodiment of the present invention;

Figure 3a is an elevation view of a CMOS wafer of Figure 1a following planarization;

Figure 3b is an elevation view of the CMOS wafer of Figure 3a following etching to expose the vertical connector;

Figure 3c is an elevation view of a CMOS wafer of Figure 1a stacked with the CMOS wafer of Figure 3b according to a third embodiment of the present invention;

Figure 4 is an elevation view of a CMOS wafer of Figure 1a stacked with a CMOS wafer of Figure 3b following placement of copper pads;

Figure 5 is an elevation view of a further CMOS wafer of Figure 1a stacked upon the CMOS wafers of Figure 4;

Figure 6 is an elevation view of an I/O pad stacked upon the CMOS wafers of Figure 5.

Description of the Preferred Embodiment

Figures 1a and 1b show two embodiments of the invention both involving IC layered CMOS process wafers. The IC layers 15, 20 have been formed within dielectric layers 41, 42 and together formed on silicon substrates 40, 45. An outer surface of the wafer 5, 10 has copper pads 35, 38 embedded in the surface of the dielectric.

The major point of differentiation between the embodiments of Figures 1a and 1b is the placement of the vertical connectors 25, 30. In the case of Figure 1a, the vertical connector has been embedded in the wafer 5 prior to the first IC layer 46 (metal-1) being formed. Figure 1b has the vertical connector 30 embedded in the wafer 10 following the placement of the integrated circuit layers 20, but prior to the placement of copper pads 38. In fact, the invention does not rely on any specific location or stage of formation of the vertical connectors 25, 30 that may be placed prior to any of the IC metal layers, such as metal-1 to metal-6 of Figure 1.

A feature of the invention differentiating the embodiments of Figure 1a and 1b is the connection of the vertical connectors 25, 30 to the copper pads 35, 38. In Figure 1a, the connection is hidden in that the copper pad 35 is connected from the vertical connector 25 through several IC layers 15. The IC layers 15 may be constructed in any conventional manner, with the precise nature and structure of these integrated circuit

elements being well known to the person skilled in the art. In Figure 1b, the connection is direct that the vertical connector 30 is connected to the copper pad 38 by forming simultaneously these two element using copper dual-damascene processes, or in two steps, making connector, 30 followed by copper pads 38.

Figure 2 shows a detail view of the vertical connector 25 according to the embodiment of Figure 1a.

This embodiment, shows the vertical connector 25 embedded in a silicon substrate 40 and dielectric layer 42, for instance silicon dioxide. It should be noted that the substrate 40 may be of several different materials, as would be understood by the skilled addressee, including Si, SeGe or GaAs. The process commences with a via etched into the dielectric layer 42 and silicon substrate 40. Next is deposited a nitride layer 70 followed by an oxide layer 65 and then a metal barrier 60 prior to the via being filled with the metal 55.

The nitride layer 70 has a dual function to, firstly, act as a diffusion barrier to prevent the diffusion of metal 55 from the via into the surrounding substrate. It has a further secondary function to act as an etch stop layer during the wet etch process for thinning backside of the stacked wafer. The nitride layer 70 may be of a thickness in the range 0.05 to 0.1 μm, and may be of SiN.

The oxide layer 65, which may be a silicon dioxide layer, possibly in the range of 0.05 to 0.3 microns, acts as an electrical insulator between the surrounding substrate

and the vertical connector. It also has a secondary function to act as an etch stop layer during the dry etch process for thinning backside of the stacked wafer.

A metal diffusion barrier 60 is placed over the oxide layer 65 to further prevent diffusion of the metal 55 from diffusing into the wafer. Preferably, the diffusion barrier 60 will be of a thickness in the range 200 to 1,000 angstroms and comprise metals such as Ti, TiN, $Ti_xSi_yN_z$, Ta, TaN, $Ta_xSi_yN_z$, W, WN and WN_2. It also has a secondary function to act as an erosion stop layer during the CMP process for thinning backside of the stacked wafer. Preferably, the barrier metal for Cu may be Ta as a connector conducting material, Ti/TiN as under layer for Al or W conducting materials.

The via is then filled with a metal 55 such as tungsten, aluminium and copper, or alloys thereof, to complete the vertical connector 25. The benefits provided by such a vertical connector 25 include very short inter-wafer interconnections, shorter than 15μm, for layer to layer (wafer to wafer connectivity). Importantly, it will provide white-light alignment targets for subsequent lithographic processes on the reverse side of the thinned wafer of the wafer stack. The vertical connector may be in the range of 1 to 10 um in diameter and 4 – 6 um deep into the substrate.

The formation of the vertical connector 30 may be of similar construction to that of the embodiment of Figure 1a and in fact other embodiments falling within the broader invention. Vertical connector, 30 can also be constructed as an integral part of copper pad 38 using conventional dual-damascene processes.

With reference to Figures 3a to 3c, the stacked wafer 72 is formed by combining two wafers 5, 75 so as to bring the plurality of copper pads 90, 95 into contact at an interface 85. The contact of copper pads 90, 95 at interface 85 is ensured by recessing the neighboring oxide field (0.03 ~ 0.1um, using wet/dry etch) around the pads. Because of the exposure of the pre-cleaned copper pads 90, 95 a high degree of thermal inter-diffusion of the copper pads may be achieved and certainly within the tolerances required for fabrication of the stacked wafer 72. The copper pads are then prepared for bonding, such as cleaning the pads and surrounding surface recess process. Preferably, the protrusion of copper bonding pads surface can be achieved by recessing surrounding dielectric surface by either wet or dry etch processes followed by Cu pad surface cleaning process utilizing wet or dry etch techniques. However, BOE (mixture of Ammonium Fluoride, Hydrofluoric acid and water) can simultaneously clean Cu bonding pad surfaces and recess the surrounding dielectric surface provided the surrounding dielectric surface is composed of SiO2.

Whilst in contact, the wafers are subjected to sufficient pressure and temperature conditions to force the copper pads into thermal diffusion and thus bonding the wafers 5, 75 at the interface 85 between the copper pads 90, 95. Conditions to achieve thermal diffusion of the copper may be at a pressure within the range 20 to 60 psi at a temperature in the range 300 to 450°C in a oxygen free (nitrogen, inert gases or vacuum) environment for a residence time of 5 to 50 minutes.

Having achieved the bonding at the interface 85, two wafers stacked devices can be made by thinning the bottom wafer on which I/O pads needs to be constructed. Backside surface of the bottom wafer may be thinned by coarse and fine grinding followed by CMP and then subjecting it to wet/dry etch process until the bottom surface 100 of the vertical connector 102 appeared at the thinned surface. Thus, by bonding the wafers 5, 75 to form a stacked wafer 72, an individual wafer 5 may be thinned without risk of rupturing of thinned wafer during the process, or later handling, due to the added robustness by virtue of stacked top wafer 75. Exposed surface 100 is recessed by 0.2~ 2um utilizing dry or wet etch process ensuring a protrusion of vertical connector 102 over surrounding surface 103 as shown in Figure 3a and 3b. A 0.3 ~ 2um thick SiO2 layer 81 is then deposited over surface 100 and 103. Layer 81 is then planarized using standard techniques namely, oxide CMP or selective Oxide etch-back processes to ensure the surface of the vertical electrical connector 102 is exposed. A layer of I/O pads metal 140 consisting of Ti/TiN and Al alloy is sputter deposited. I/O pad metal mask can be aligned with great accuracy using alignment targets visible on exposed surface 100 (bottom of connector 102). I/O pad metal is finally defined by etching process using conventional methods.

In order to form more complex stacked wafer (3 and more) a thinning process will be performed on the backside of top wafer of two-wafer stack as shown in Figure 4. Having reached the upper surface 100 of the vertical connector 102, Si is further recessed as described above. A 0.3 ~ 2um SiO2 layer is deposited on the recessed Si surface and followed by planarization process. The new surface 80 can then be patterned utilizing white-light exposure tool to eventually create copper pad 105 using

conventional single copper damascene process steps. After recessing neighboring oxide surface 80 the two-wafer stack is ready for combination with a further wafer. It should be noted that the copper pads may include both electrically connecting pads for connecting the two or more wafer devices and dummy pads on the same plane with the electrically connecting pads. In this arrangement, the dummy pads promote the bonding strength of adjoining wafers.

Figure 5 shows the addition of a further wafer 115 to form a more complex stacked wafer 110. As with the previous bonding step, the corresponding arrays of pads 120, 125 are into alignment to form an interface 130, whereupon the pads bond through thermal diffusion whilst having applied there to pressure at a certain temperature for a specified residence time. To construct a more complex stacked wafer, the process can be continued until the desired device has been formed.

I/O pads in Figure 6 can be generated after thinning down bottom wafer 5, followed by process steps to form I/O pads as described above with reference to Figure 3a. Back-side processes for I/O and the other for Cu, include a 0.3– 2um thick dielectric, preferably PECVD TEOS deposited below 400C. All I/O pads formation on back-side of the wafer for the first time in IC fabrication. Elimination of passivation mask (since the circuit is buried under the Si surface containing I/O pads) for IC fabrication.

Other features of the invention may include alignment targets (for white light and IR alignment) utilizing backside of embedded vertical connectors (preferably placed in between scribe lines) that permit standard aligners to recognize vendor

recommended and/or modified fiducials. Further, thinning control may include composite materials on side walls of vertical connectors, having thicknesses in the range of 0.05 – 0.1 um for SiN, 0.05 – 0.3um for SiO2 and 0.025 – 0.1 for Ta or Ti/TiN.

Claims:

1. A method of forming a stacked wafer device comprising the steps of :

providing a first wafer;

forming a plurality of copper pads in a first surface of the first wafer;

forming at least one embedded vertical connector in the first wafer in isolation from the copper pads of the first wafer;

providing a second wafer;

forming a plurality of copper pads in a first surface of the second wafer, the placement of the copper pads to coincide with the location of the copper pads of the first wafer;

forming at least one embedded vertical connector in the second wafer in isolation from the copper pads of the second wafer;

bringing the first surfaces of the wafers into contact, so as to contact the copper pads;

applying a force to the wafers at a pre-determined pressure and at a pre-determined temperature until the copper pads are bonded, and so forming the stacked wafer device from the bonded first and second wafer.

2. The method according to claim 1, wherein the step of forming the plurality of copper pads comprises any one of : a single-damascene process utilizing CMP process, a dual-damascene process utilizing CMP process, a dry etch process, a wet etch process or both a wet and a dry etch process.

3. The method according to claim 1 or 2, wherein the step of forming the plurality of copper pads is preceded by the step of placing a barrier layer for separating the plurality of copper pads from the wafer said layer comprising any one or a combination of : Ti, TiN, $Ti_xSi_yN_z$, Ta, TaN, $Ta_xSi_yN_z$, W, WN and WN_2.

4. The method according to any one of the preceding claims, wherein the step of providing said wafers comprises forming the wafers by Plasma Enhanced Chemical Vapor Deposition.

5. The method according to claim 4 wherein the wafers comprise undoped-SiO_2, tetraethyl-orthosilicate (TEOS), SiON, phosphosilicate glass (PSG), fluorosilicate glass (FSG), SiOC, borophosphosilicate glass (BPSG).

6. The method according to claim 1 wherein the step of providing said wafers comprises forming the wafers by SOG (Spin-On-Glass) method.

7. The method according to claim 6 wherein the wafers comprise SOG, SiLK (Spin-on low-k dielectrics).

8. The method according to any one of the preceding claims, wherein the step of forming at least one embedded vertical connector is achieved by a dry etch process utilizing fluorine based plasma.

9. The method according to any one of the preceding claims, wherein the embedded vertical connector is extends into the wafer substrate from an inter-metal dielectric layer.

10. The method according to claim 9, wherein the vertical connector is embedded in the wafer at a depth in the range of 4 to 10 μm.

11. The method according to claim 1, wherein the vertical connector has a diameter in the range of 0.2 – 10μm.

12. The method according to any one of the preceding claims, further comprising the step of exposing the copper pads so as to project said pads from the surface of the wafer by lowering the dielectric surface using either or both of a wet and dry etch process.

13. The method according to claim 12 wherein the exposed copper pads project from the surface in the range 0.2 um to 2um.

14. The method according to any one of the preceding claims, wherein a material of at least one of the embedded vertical connectors is more resistant to CMP than the material of the corresponding wafer.

15. The method according to claim 12 or 13, further including the steps of depositing a dielectric layer using conventional CVD technique and;

processing the dielectric layer using a CMP process to provide a planar surface;

16. The method according to claim 15, wherein the dielectric layer thickness is in the range of 1 to 2um.

17. The method according to claim 15, further including the step of forming I/O pads on a second side of the first wafer.

18. The method according to any one of the preceding claims, further including the step of grinding outer surfaces of the stacked wafer device, then applying CMP to expose at least a portion of the embedded vertical connectors of either or both the first and second wafer.

19. The method according to any one of the preceding claims,, further including the steps of :

providing a third wafer;

forming a plurality of copper pads in a first surface of the third wafer;

forming at least one embedded vertical connector in the third wafer in isolation from the copper pads of the third wafer;

bringing the first surface of the third wafer into contact with an outer surface of the stacked wafer device, so as to contact the copper pads;

applying a force to the third wafer and stacked wafer device at a pre-determined pressure and at a pre-determined temperature until the copper pads are bonded.

20. The method according to claim 19, wherein the step of bringing the first surface of the third wafer into contact the outer surface of the stacked wafer includes the step of :
utilizing visible back-side surface of vertical connectors as white-light alignment fiducials.

21. The method according to any one of the preceding claims, further including the steps of :
printing I/O metal layer utilizing visible back-side surface of vertical connectors as white-light alignment fiducials and;
defining I/O pads by conventional metal etch process to generate electrically active stacked wafer device

22. The method according to any one of the preceding claims, wherein the material used for forming any of the individual embedded vertical connectors comprise any one or alloys of titanium, tungsten, aluminium and copper.

23. The method according to claim 22, wherein the embedded vertical connector is isolated from the substrate by a barrier layer.

24. The method according to claim 23, wherein the barrier layer includes a metal barrier layer comprising any one or a combination of : Ti, TiN, $Ti_xSi_yN_z$, Ta, TaN, $Ta_xSi_yN_z$, W, WN, and WN2.

25. The method according to claim 23, wherein the barrier layer includes an oxide layer.

26. The method according to claim 23, wherein the barrier layer includes a nitride layer.

27. The method according to claim 1, wherein at least one wafer includes a substrate comprising Si, SeGe or GaAs.

28. The method according to claim 1, wherein the plurality of copper pads include electrically connecting pads for connecting two or more wafer devices, and dummy pads on the same plane with the electrically connecting pads, said dummy pads for promoting bonding strength of adjoining wafers.