

A B S T R A C T

A semiconductor memory device includes a first and second substrates; and a first and second element layers respectively provided on an upper surface of the first and the second substrates. The first and second substrates respectively include a first and second vias. The first and second element layers respectively includes a first and second pads respectively electrically coupled to the first and second vias, and respectively provided on an upper surface of the first and second element layers. The upper surface of the second element layer is arranged so as to be opposed to the upper surface of the first element layer. The first and second pads are electrically coupled and symmetrically arranged with respect to a surface where the first and second element layers are opposed to each other.