CLAIMS

1. A thermal conduction structure (400, 420) for an integrated circuit transistor device (402), including:
   (a) a silicon island (422) formed within a field oxide region (424) of a semiconductor wafer structure;
   (b) a transistor device (402) formed within a portion of the silicon island (422);
   (c) at least one electrically isolating structure (428) formed within the silicon island (422), each electrically isolating structure (428) positioned so as to electrically isolate the portion of the silicon island (422) containing the transistor device (402) from an edge portion (422a,422b) of the silicon island, each edge portion (422a,422b) located in a lateral direction from the transistor device (402) but thermally coupled through a respective electrically isolating structure (428) to the portion of the silicon island (422) containing the transistor device (402);
   (d) an interlevel dielectric layer formed over at least one of the at least one electrically isolating structure (428);
   (e) at least one thermal path (404) having a first portion (404a) in thermal contact, through the interlevel dielectric layer, with a respective edge portion (422a,422b) of the silicon island (422), and a second portion (404b) spaced away from the respective edge portion (422a,422b) of the silicon island (422) in a lateral direction from the transistor device (402) so that the second portion (404b) may be coupled to a generally orthogonal thermal pathway (440) without the generally orthogonal thermal pathway (440) being blocked by or interfering with the transistor device (402), each thermal path (404) being substantially electrically isolated from the transistor device (402);
   (f) a handle wafer affixed to the semiconductor wafer structure such that a gate of the transistor device (402) is oriented towards the handle wafer; and
   (g) at least one generally orthogonal thermal pathway (440) thermally coupled to the second portion (404b) of a respective one of the at least one thermal path (404) and configured to convey heat from the respective one of the at least one thermal path (404) to at least one of (i) at least one externally accessible thermal pad (406), or (ii) the handle wafer.

2. The invention of claim 1, wherein the at least one electrically isolating structure (428) is formed by a shallow trench isolation process.

3. The invention of claim 1, wherein at least one thermal path (404) is formed at least in part by at least one metallization layer.

4. The invention of claim 1, wherein the handle wafer is spaced from the transistor device (402) by a passivation layer, and the at least one generally orthogonal thermal pathway (440) includes at least one thermal via (502) formed through the passivation layer so as to be thermally coupled to the handle wafer.

5. A thermal conduction structure (700) for an integrated circuit transistor device (701), including:
   (a) a silicon island (602) formed within a field oxide region of a semiconductor wafer structure;
   (b) an insulating gate oxide (612) formed over the silicon island (602);
   (c) a transistor device (701) including a gate (608) formed on the insulating gate oxide (612) and a source and a drain formed within a portion of the silicon island (602);
   (d) at least one dummy gate (610) formed on the insulating gate oxide (612) over the silicon island (602) and having a portion extending beyond at least one edge of the silicon island (602), the at least one dummy gate (610) being electrically isolated from the transistor device (701) and in thermal contact with the transistor device (701) through the insulating gate oxide (612);
   (e) at least one thermally conductive structure (702) formed in thermal contact with the portion of at least one of the at least one dummy gate (610) extending beyond the at least one edge of the silicon island (602), and electrically isolated from the transistor device (701);
   (f) a handle wafer affixed to the semiconductor wafer structure such that the gate of the transistor device (701) is oriented towards the handle wafer; and
   (g) at least one generally orthogonal thermal pathway thermally coupled to a respective one of the at least one thermally conductive structure (702) and configured to convey heat from the respective thermally conductive structure (702) to at least one of (i) at least one externally accessible thermal pad (406), or (ii) the handle wafer.

6. The invention of claim 5, wherein the at least one dummy gate (610) comprises polysilicon.

7. The invention of claim 6, wherein at least one of the at least one thermally conductive structure (710) extends over at least a portion of a length of a respective dummy gate (610).

8. A method of making a thermal conduction structure for an integrated circuit transistor device formed within a portion of a silicon island formed within a field oxide region of a semiconductor wafer structure and mounted on a handle wafer such that a gate of the transistor device is oriented towards the handle wafer, including:
   (a) fabricating at least one electrically isolating structure within the silicon island, each electrically isolating structure positioned so as to electrically isolate the portion of the silicon island containing the transistor device from an edge portion of the silicon island, each edge portion located in a lateral direction from the transistor device but thermally coupled through a respective electrically isolating structure to the portion of the silicon island containing the transistor device;
   (b) fabricating an interlevel dielectric layer over at least one of the at least one electrically isolating structure;
   (c) fabricating at least one thermal path having a first portion in thermal contact, through the interlevel dielectric layer, with a respective edge portion of the silicon island, and a second portion spaced away from the respective edge portion of the silicon island in a lateral direction from the transistor device so that the second portion may be coupled to a generally orthogonal thermal pathway without the generally orthogonal thermal pathway being blocked by or interfering with the transistor device, each thermal path being substantially electrically isolated from the transistor device; and
   (d) fabricating at least one generally orthogonal thermal pathway thermally coupled to the second portion of a respective one of the at least one thermal path and configured to convey heat from the respective one of the at least one thermal path to at least one of (i) at least one externally accessible thermal pad, or (ii) the handle wafer.

9. The method of claim 8, further including fabricating the at least one electrically isolating structure by a shallow trench isolation process.

10. The method of claim 8, further including fabricating the at least one thermal path at least in part out of a metallization layer.

11. The method of claim 8, further including spacing the handle wafer from the transistor device by a passivation layer, and forming at least one thermal via through the passivation layer so as to be thermally coupled to the handle wafer and to a respective one of the at least one generally orthogonal thermal pathway.

12. A method of making a thermal conduction structure for an integrated circuit transistor device formed within a portion of a silicon island formed within a field oxide region of a semiconductor wafer structure and mounted on a handle wafer such that a gate of the transistor device is oriented towards the handle wafer, including:
    (a) fabricating at least one dummy gate on an insulating gate oxide over the silicon island and extending beyond at least one edge of the silicon island, the at least one dummy gate being electrically isolated from the transistor device and in thermal contact with the transistor device through the insulating gate oxide;
    (b) fabricating at least one thermally conductive structure in thermal contact with at least one of the at least one dummy gate and electrically isolated from the transistor device; and
    (c) fabricating at least one generally orthogonal thermal pathway thermally coupled to a respective one of the at least one thermally conductive structure and configured to convey heat from the respective thermally conductive structure to at least one of (i) at least one externally accessible thermal pad, or (ii) the handle wafer.

13. The method of claim 12, wherein the at least one dummy gate comprises polysilicon.

14. The method of claim 13, further including fabricating at least one of the at least one thermally conductive structure at least in part by fabricating at least one metallization layer extending over at least a portion of a length of a respective dummy gate.

15. The invention of claims 1 or 5, wherein the handle wafer is glass.

16. The method of claims 8 or 12, wherein the handle wafer is glass.