

CLAIMS:

1. A semiconductor package, comprising:

a first package substrate having a first side and a second side, the first side opposite the second side, the first package substrate comprising:

a layer comprising a semiconductor material;

a first ground interconnect structure between the first side and the second side of the first package substrate;

a second ground interconnect structure between the first side and the second side of the first package substrate;

a third ground interconnect structure between the first side and the second side of the first package substrate, wherein the first ground interconnect structure, the second ground interconnect structure and the third ground interconnect structure extend through the layer comprising the semiconductor material; and

a ball pad on the second side of the first package substrate, the ball pad comprising copper, wherein the first ground interconnect structure, the second ground interconnect structure and the third ground interconnect structure are in contact with the ball pad; and

a die coupled to the first side of the first package substrate; and

a second package substrate coupled to the second side of the first package substrate.

2. The semiconductor package of claim 1, further comprising an additional ground interconnect structure between the first side and the second side of the first package substrate, the additional ground interconnect structure through the layer comprising the semiconductor material, and the additional ground interconnect structure in contact with the ball pad.

3. A semiconductor package, comprising:

a first package substrate having a first side and a second side, the first side opposite the second side, the first package substrate comprising:

a first package substrate layer comprising a semiconductor material;

a first ball pad on the second side of the first package substrate, the first ball pad comprising copper;

a first interconnect structure between the first side and the second side of the first package substrate and through the first package substrate layer, the first interconnect structure being at least partially directly over the first ball pad of the first package substrate, the first interconnect structure being in electrical contact with the first ball pad;

a second interconnect structure between the first side and the second side of the first package substrate and through the first package substrate layer, the second interconnect structure being at least partially directly over the first ball pad of the first package substrate, the second interconnect structure being spaced laterally from the first interconnect structure, the second interconnect structure being in electrical contact with the first ball pad of the first package substrate;

a third interconnect structure between the first side and the second side of the first package substrate and through the first package substrate layer, the third interconnect structure being at least partially directly over the first ball pad of the first package substrate, the third interconnect structure being spaced laterally from the first interconnect structure and being spaced laterally from the second interconnect structure, the third interconnect structure being in electrical contact with the first ball pad of the first package substrate;

a second ball pad on the second side of the first package substrate, the second ball pad comprising copper;

a fourth interconnect structure between the first side and the second side of the first package substrate and through the first package substrate layer, the fourth interconnect structure being at least partially directly over the second ball pad of

the first package substrate, the fourth interconnect structure being in electrical contact with the second ball pad of the first package substrate;

a die coupled to the first side of the first package substrate; and

a second package substrate coupled to the second side of the first package substrate.

4. The semiconductor package of claim 3, wherein there are fewer interconnect structures between the first side and the second side of the first package substrate and through the first package substrate layer that are at least partially directly over the second ball pad than there are interconnect structures between the first side and the second side of the first package substrate and through the first package substrate layer that are at least partially directly over the first ball pad.

5. The semiconductor package of claim 3, the first package substrate further comprising a second package substrate layer.

6. The semiconductor package of claim 5, the first package substrate further comprising:

a fifth interconnect structure between the first side and the second side of the first package substrate and through the second package substrate layer, the fifth interconnect structure being directly over the first interconnect structure and being in electrical contact with the first interconnect structure;

a sixth interconnect structure between the first side and the second side of the first package substrate and through the second package substrate layer, the sixth interconnect structure being directly over the second interconnect structure and being in electrical contact with the second interconnect structure; and

a seventh interconnect structure between the first side and the second side of the first package substrate and through the second package substrate layer, the seventh interconnect structure being directly over the third interconnect structure and being in electrical contact with the third interconnect structure.

7. The semiconductor package of claim 3, the first interconnect structure, the second interconnect structure, and the third interconnect structure all being in direct contact with the first ball pad.

8. A semiconductor package, comprising:

a package substrate having a first side and a second side, the first side opposite the second side, the package substrate comprising:

a ball pad on the second side of the package substrate; and

a vertical interconnect between the first side and the second side of the package substrate, the vertical interconnect comprising a first ground conductive via laterally adjacent to a second ground conductive via, wherein the first ground conductive via and the second ground conductive via are both in direct contact with the ball pad;

a die coupled to the first side of the package substrate, the die having a footprint; and

a solder ball coupled to the bond pad on the second side of the package substrate, the solder ball outside of the footprint of the die.

9. The semiconductor package of claim 8, wherein the package substrate is a multi-layer package substrate comprising one or more conductive layers, and wherein the first ground conductive via and the second ground conductive via are between the ball pad and one of the one or more conductive layers.

10. The semiconductor package of claim 9, wherein the one of the one or more conductive layers is a layer immediately above the first ground conductive via and the second ground conductive via.

11. The semiconductor package of claim 8, wherein the first ground conductive via and the second ground conductive via extend fully between the first side and the second of the package substrate.

12. The semiconductor package of claim 8, the first ground conductive via and the second ground conductive are coupled to electrical routing in the package substrate, the electrical routing coupled to the die.

13. The semiconductor package of claim 8, further comprising a second die electrically coupled to the first die.

14. The semiconductor package of claim 13, further comprising a second package substrate, the second die attached to the second package substrate, and the second package substrate electrically coupled to the first package substrate.

15. The semiconductor package of claim 8, wherein the vertical interconnect further comprises a third ground conductive via laterally adjacent to the first and second ground conductive vias, wherein the third conductive via is in direct contact with the ball pad.

16. The semiconductor package of claim 15, wherein the vertical interconnect further comprises one or more additional ground conductive via laterally adjacent to the first, second and third ground conductive vias, wherein the one or more additional ground conductive vias are in direct contact with the ball pad.

17. The semiconductor package of claim 8, wherein the ball pad comprises copper.