

Sampled Data Circuit

Introduction

5 This invention relates to sampled data circuits. Sampled data circuits are widely used in, inter alia, analogue filters. Many modern electronic systems use sampled data analogue filters since these are precise and suitable for fabrication in integrated circuit (IC) form.
10 One disadvantage they exhibit is radiation at a multiple of the clock frequency. This tends to be produced because the switches used to control the data transfer must all be simultaneously open during the transitions of the clock. The currents controlling the switches must thus all be low,
15 or high, twice per clock period. The supply current of the system may consequently carry an important component in the form of pulses at twice the clock frequency.

It is the object of this invention to sensibly reduce this undesirable component.

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Statement of the Invention

In accordance with the invention a sampled data circuit having: two or more serially connected sampled data
25 stages each comprising switching means and storage means; and clock means for applying to the switching means of consecutive stages clock signals of respectively first and second phases alternating between first and second levels is characterised in that the clock signals also have a
30 third level intermediate the first and second levels which is occupied simultaneously by the first and second phase clock signals.

Brief Description of the Drawings

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One sampled data circuit in accordance with the invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 shows part of the sampled data circuit;

Figure 2 shows clock waveforms generated in the circuit of Figure 1; and

Figure 3 shows in greater detail the circuit of the clock generator of Figure 1.

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Description of Specific Embodiment of The Invention

Referring now to Figure 1 a sampled data circuit has a number of sampled data stages 2 (only two of which are
10 shown) under the control of a clock generator 4. Each sampled data stage comprises a bipolar switch 6, storage capacitor 10 and buffer amplifier 12. Such an assemblage may constitute the basic building block of a sampled signal processing circuit. The assemblage also contains a current
15 source 14 connected between a positive supply line 16 and the base of an npn transistor 18, said base being also connected to the anode of a Schottky diode 20 and the collector of a driver transistor 22. The cathode of the Schottky diode 20 is connected to the collector of the
20 transistor 18, the transistor-diode combination forming the switch 6, the state of which is controlled by the magnitude of the collector current of the driver transistor 22, which is in turn controlled by a clock signal applied to the base of the driver transistor 22 from the clock generator 4. As
25 will be further explained below clock signals of alternate phases are applied to alternate sampled data stages 2 so that sampled data is transferred sequentially from stage to stage in known manner.

When the clock signal applied to a sampled data stage
30 is low, transistor 22 is rendered non-conducting and the current supplied by current source 14 flows via the Schottky diode 20 and transistor 18 to input node 26 of the stage, which must be designed to absorb said current. In this condition the combination of transistor 18 and
35 Schottky diode 20 presents a low impedance allowing the storage capacitor 10 to be charged to a voltage representative of the signal voltage applied at node 26.

When the clock signal is high transistor 22 is caused to absorb a current higher than that supplied by the current source 14, the excess current in this embodiment being drawn from the circuit 4 providing the clock signal.

5 Transistor 18 is rendered non-conducting and the voltage stored on capacitor 10 remains at a level representative of the signal voltage applied at node 26 at the end of the clock period. This sample of the signal is supplied to the following sampled data stage via the buffer amplifier 12,
10 the output of which is connected to the input node of the following stage.

As mentioned above, a number of such circuits connected in series are used in a signal processing arrangement, e.g. a filter, the even stages being
15 controlled by a clock signal of a first phase and the odd stages by a clock signal of a second phase. It will be clear that the even stage switches may only be conducting while the odd stage switches are non-conducting, and vice versa, since otherwise a signal would be propagated
20 immediately through all the stages instead of being propagated under the control of the clock. There must therefore be periods around each clock transition time when both switches are open, that is all driver transistors 22 are conducting and absorbing currents in excess of those
25 supplied by the current sources 14.

Outside these periods only alternate transistors 22 are conducting. The total supply current will thus be substantially higher during the periods around the clock transition times than otherwise.

30 To eliminate this effect the invention employs three-level clock signals as shown in Figure 2. The intermediate level, occupied simultaneously by both phases of the clock, suffices to open the switches. The high level is such that the total current flow occasioned is the
35 same as that occasioned when the phases are at the intermediate level. The pulses of high current which would flow at the clock transition times with conventional two-level clock signals are thus eliminated.

Referring now to Figure 3, the clock generator circuit 4 for generating clock waveforms of the form shown in Figure 2 has inputs C_1 , $\overline{C_1}$, to which are applied simple overlapping clock inputs.

5 The inputs C_1 , $\overline{C_1}$ of the clock generator 4 are connected respectively to the bases of npn bipolar transistors T_1 , T_1' . These transistors each have their collectors connected to a supply line 28 and their emitters connected via respective resistors and diodes R_1 , D_1 and
10 R_1' , D_1' to ground. The emitters of the transistors T_1 , T_1' are also connected respectively via resistors R_2 , R_2' to outputs of the circuit C_2 , $\overline{C_2}$. The cathodes of the diodes D_1 , D_1' are connected respectively to the bases of transistors T_2 , T_2' . The collectors of the transistors T_2 ,
15 T_2' are connected respectively to the outputs C_2 , $\overline{C_2}$ and the emitters of the transistors are connected to ground.

Operation of the clock generator circuit of Figure 3 will be readily appreciated. If, for example, C_1 is high and $\overline{C_1}$ low, then C_2 is high and $\overline{C_2}$ low. While both C_1 and
20 $\overline{C_1}$ are high, C_2 and $\overline{C_2}$ are reduced to the intermediate level by the cross coupling via R_1 , D_1 , T_2 , R_2' and R_1' , D_1' , T_2' , R_2 . It will be understood that this cross-coupling also serves to generate a pull down current for the low level output.

25 Although the arrangement described above requires almost twice the current that would be needed to operate the switches when using simple two-level clock signals, it will be appreciated that in a more practical circuit the excess of current drawn by transistor 22 over that supplied
30 by current source 14 can be routed to serve as a bias current for the buffer amplifier 12. In this way the current overhead can be reduced to approximately 40%.

It will also be appreciated that although the sampled data circuit above has been described as operating with a
35 two-phase clock, the invention is not limited to use with a two-phase clock but is also applicable to sampled data systems utilising clocks having three or more phases.



Claims

1. A sampled data circuit having: two or more serially connected sampled data stages each comprising switching
5 means and storage means; and clock means for applying to the switching means of consecutive stages clock signals of respectively first and second phases alternating between first and second levels,
characterized in that
10 the clock signals also have a third level intermediate the first and second levels which is occupied simultaneously by the first and second phase clock signals.
2. A sampled data circuit according to claim 1 wherein
15 the clock means includes a clock generator comprising:
a first transistor having a control electrode for receiving a first clock input signal, a first current electrode for connection to a first potential and a second current electrode coupled to a first output node;
20 a first diode coupled between the second current electrode of the first transistor and a datum node for receiving a second potential;
a second transistor having a control electrode for receiving a second clock input signal of opposite polarity
25 to the first clock input signal, a first current electrode for connection to a source of supply potential and a second current electrode coupled to a second output node;
a second diode coupled between the second current electrode of the second transistor and the datum node;
30 a third transistor having a control electrode connected to the first diode at its electrode remote from the datum node, a first current electrode connected to the second output node and an second current electrode connected to the datum node; and
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a fourth transistor having a control electrode connected to the second diode at its electrode remote from the datum node, a first current electrode connected to the first output node and a second current electrode connected
5 to the datum node.

3. A sampled data circuit according to claim 2 wherein the transistors are bipolar transistors, the first current electrodes are collectors and the second current electrodes
10 are emitters.

4. An integrated circuit containing a sampled data circuit according to any preceding claim.

15 5. A sampled data circuit substantially as hereinbefore described with reference to the accompanying drawings.

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