DESCRIPTION

INFORMATION PROCESSING DEVICE

FIELD

[0001] Embodiments described herein relate generally to an information processing device.

BACKGROUND

[0002] For example, an intelligent input/output device is known which includes multiple master MPUs that access for control via a shared memory in a system applied to process control.

Such an intelligent input/output device includes one or more master MPUs that process input/output data from and to corresponding controlled devices, a shared memory for input/output data transfer to and from a master MPU of a host controller, and a circuit that connects the master MPUs processing input/output data and the master MPU of the host controller to the shared memory.

CITATION LIST

Patent Literature

[0003] Patent Literature 1: Japanese Laid-open Patent Publication No. 2000-20491

SUMMARY OF THE INVENTION

Problem to be Solved by the Invention

[0004] In the conventional intelligent input/output device, when two or more master MPUs access the shared memory concurrently, the other or rest of the master MPUs need to wait for access until one of the master MPUs completes the processing.

[0005] This may lead to decreasing an effective

processing speed of the master MPU waiting for the processing. Particularly, as the number of master MPUs increases, the number of master MPUs waiting for the processing also increases, which may cause a significant decrease in the effective processing speed of each master MPU.

[0006] In view of the above, the embodiments aim to provide an information processing device that enables master MPUs of an intelligent input/output device to transfer input/output data via a shared memory without a decrease in the effective processing speed of each master MPU even with an increase in the number of master MPUs.

Means for Solving Problem

[0007] An information processing device according to the embodiments is the information processing device that controls access from n (n being an integer equal to or greater than 2) MPUs to a shared memory.

A control unit analyzes an access pattern to the shared memory based on access requests to the shared memory received in parallel from the n MPUs in a same access phase, and sequentially processes, in the access phase, the received m (m being a natural number equal to or less than n) access requests in order based on the analyzed access pattern.

BRIEF DESCRIPTION OF DRAWINGS

[0008] FIG. 1 is a schematic block diagram of a configuration of a process control system 10 including an information processing device according to an embodiment.

FIG. 2 is a schematic block diagram of a configuration of a host controller 11 and an intelligent input/output

pressure).

[0011] In the following, for the purpose of better understanding, one master MPU 23-1 of the intelligent input/output device 12 will be mainly described. In the following description, it is assumed that read addresses and write addresses in a shared memory 21 are pre-assigned to the controlled devices DEV1 to DEVn, an access order is also designated in advance in a cyclic manner, and the same read address or write address is not redundantly assigned to the controlled devices DEV1 to DEVn.

[0012] FIG. 2 is a schematic block diagram of a configuration of the host controller 11 and the intelligent input/output device 12.

The host controller 11 includes a master MPU 11A that controls the host controller 11 as a whole and includes a clock terminal CLK, a ready terminal RDY to which a first ready signal RDY1 is input, a chip select terminal CS, an address terminal ADR, a read terminal RD, a write terminal WT, and a data terminal DATA.

[0013] The intelligent input/output device 12 includes a shared memory 21 that stores input/output data, a control unit (hereinafter referred to as an arbitration control circuit 22) that arbitrates master MPUs when competing access to the shared memory 21, and master MPUs 23-1 to 23-n that control data input and output to and from the controlled device DEV1 to DEVn.

[0014] The arbitration control circuit 22 includes a first access temporary latching processing unit 31 that temporarily latches access data to the shared memory 21 from the master MPU 11A of the host controller 11, a second access temporary latching processing unit 32 that temporarily latches access data from the master MPUs 23-1 to 23-n to the shared memory 21, and an access pattern

address data output from the address terminal ADR and write data output from the data terminal DATA of the master MPU 11A in the first sub phase A0 of the T2 phase (indicated by T2_A0 in FIG. 4). On the other hand, the second access temporary latching processing unit 32 of the arbitration control circuit 22 latches address data output from the address terminal ADR and write data output from the data terminal DATA of the master MPU 23-1 (Step S11).

[0045] Then, the access pattern analyzer 33 analyzes an access pattern from a combination of the statuses of the chip select terminals CS, the read terminals RD, and the write terminals WT of both the master MPU 11A and the master MPU 23-1 (Step S12).

Subsequently, the access pattern analyzer 33 determines whether the analyzed access pattern is access pattern No. 1 that both the master MPU 11A and the master MPU 23-1 read data from the shared memory 21 (Step S13).

[0046] When determining in Step S13 that the analyzed access pattern is access pattern No. 1 (Yes in Step S13), the access pattern analyzer 33 controls the address switching processing unit 34 to switch an address bus and a data bus to the master MPU 11A in the second sub phase A1 of the T2 phase (indicated by T2_A1 in FIG. 4) (Step S14).

[0047] Thus, the access pattern analyzer 33 issues (outputs) a shared memory read command for the master MPU 11A as a shared memory command output (Step S15). As a result, the first access temporary latching processing unit 31 reads and latches data corresponding to the read address from the shared memory 21 (Step S16).

[0048] Subsequently, the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 23-1 in the third sub phase A2 of the T2 phase (indicated by T2_A2 in FIG. 4)

214 of the master MPU 23-1 for a longer period than the predetermined data read setup time DRS. Thereby, the master MPU 23-1 can surely receive the latched read data 213.

[0066] The processing is now described referring back to FIG. 6.

When determining in Step S13 that the analyzed access pattern is not access pattern No. 1 (No in Step S13), the access pattern analyzer 33 determines whether the analyzed access pattern is access pattern No. 2 that both the master MPU 11A and the master MPU 23-1 write data to the shared memory 21 (Step S21).

[0067] When determining in Step S21 that the analyzed access pattern is access pattern No. 2 (Yes in Step S21), the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 11A in the second sub phase A1 of the T2 phase (Step S22).

[0068] Thus, the access pattern analyzer 33 issues (outputs) a shared memory write command for the master MPU 11A to the shared memory 21 as a shared memory command output (Step S23).

As a result, the first access temporary latching processing unit 31 writes data of the master MPU 11A to an area of the shared memory 21 corresponding to the write address (Step S24).

Subsequently, the access pattern analyzer 33 controls the address switching processing unit 34 to switch the address bus and the data bus to the master MPU 23-1 in the third sub phase A2 of the T2 phase (Step S25).

[0069] Thus, the access pattern analyzer 33 issues (outputs) a shared memory write command for the master MPU 23-1 to the shared memory 21 as a shared memory command

shared memory, write data corresponding to an access request from any of the n MPUs or that reads, from the shared memory, read data corresponding to an access request from any of the n MPUs, based on the result of the analysis of the access pattern.

4. The information processing device according to any one of claims 1 to 3, wherein

the access phase includes at least (n+1) sub phases, and

the control unit analyzes the access pattern in the first sub phase of the access phase and sequentially processes the m access requests in the remaining n sub phases.

5. The information processing device according to any one of claims 1 to 4, wherein

at least one of the n MPUs constitutes a host controller, and

the MPUs other than the MPU constituting the host controller among the n MPUs constitute the information processing device, and control corresponding controlled devices under control of the host controller.