

Description

The present invention relates generally to a system wherein timing information is conveyed from a first environment to a second environment through the use of a multilevel pulse train of a so-called "sandcastle" type. More particularly, the invention relates to an encoding/decoding system for sandcastle pulses of a trilevel form which advantageously establishes tracking between one or more pulse levels of the sandcastle pulses formed by the encoder and a plurality of reference levels utilized for comparison purposes in the decoder.

Often a multiplicity of keying functions with different timing requirements are subject to performance within a common integrated circuit. A savings in terminal count may be realized by externally forming a composite, multilevel keying waveform for delivery to a single input terminal of the integrated circuit. Within the integrated circuit, level-sensitive decoder circuits are included for extracting respective keying waves of different timing from the delivered composite waveform (which is viewable as having a sandcastle-like profile).

An example of encoder circuitry suitable for use in the formation of a sandcastle pulse train with pulse components of two different levels (above a base level) is shown in US-A-4,313,130 Yost. An example of decoder circuitry suitable for use in separating the pulse components of bilevel sandcastle pulses of the type generated by the Yost encoder is presented in an article entitled "Integrated NTSC Chrominance/Luminance Processor", by L. Harwood, et al, appearing on pages 693-706 of the IEEE Transactions on Consumer Electronics, Volume CE-26 (November 1980).

In the example of the above-discussed Harwood, et al. decoder, a retrace blanking waveform and a burst gating waveform, for use in luminance/chrominance signal processing circuits of a color television receiver, are separately derived from bilevel sandcastle pulses. The bilevel sandcastle pulses exhibit a first level during initial and concluding portions of the recurring periods when retrace blanking is desired. The pulses exhibit a second higher level during intermediate ("backporch") portions of the recurring periods, which intermediate portions coincide in timing with recurring intervals during which the burst gating function is to be performed. In this instance of sandcastle pulse use, there is an overlap of the keying functions to be performed. That is, retrace blanking continues through each burst gating period. Some color television receivers incorporate apparatus for automatic control of color kinescope biasing. In such receivers, a set of keying functions, inclusive of non-overlapping as well as overlapping functions, is desirably associated with the luminance/chrominance signal processing circuits. This is explained in our co-filed Application EP-A-0146343, equivalent to US-A-4554588 of R. Shanley.

An illustrative arrangement for automatic control of color kinescope biasing in a color television receiver is that described in US-A-4,263,622-Hinn. In the Hinn arrangement, a control period, occupying a period of several successive line intervals within each vertical blanking interval, is set aside for monitoring a black level current produced by an electron gun under reference signal conditions. During this control period, departures from a desired current level are detected and the gun bias readjusted to oppose the undesired departures. During a portion of the control period, the color kinescope grid receives a conduction-enhancing pulse. Bias control is based upon information derived as indicative of the change in cathode current level introduced by the grid pulsing. An advantageous system for utilization of the above-described Hinn approach in maintenance of an appropriate bias relationship among the color kinescope's gun trio (in the face of aging and other parameter variations) is described in US-A-4484228 of R. P. Parker.

For successful use of automatic kinescope bias (AKB) control in the manner exemplified by the structures of the aforementioned Hinn patent and Parker patent, it is recognized in the aforementioned Shanley patent that the luminance/chrominance signal processing circuits require some suitable form of manipulation during the kinescope bias control intervals to avoid undesirable disturbance or contamination of the current monitoring and bias adjustment functions. These signal processing circuits process signal information for delivery to the color kinescope during the time periods intervening the periodically recurring kinescope bias control intervals.

To convey, to a single chip input terminal, timing information identifying the recurring kinescope bias control intervals, in addition to the timing information conveyed by the bilevel sandcastle pulses discussed above, it is proposed herein to employ sandcastle pulses of a trilevel form, i.e., with three different levels (above a base level) for the respective pulse components.

In a preferred embodiment of a trilevel sandcastle pulse encoding/decoding system constructed in accordance with the principles of the present invention, an on-chip decoder arrangement is employed which in a manner similar to the arrangement disclosed in Figure 7 of US-A-4227181 utilizes a trio of voltage comparators to compare incoming trilevel sandcastle pulses with respectively different reference voltages derived from different intermediate points on a common, on-chip voltage divider coupled across the terminals of a DC voltage supply. The level of one of the reference voltages is selected to lie between the base level of the train of trilevel sandcastle pulses developed by the encoder and the lowest of the pulse levels exhibited by the trilevel sandcastle pulse train. The level of a second of the reference voltages is selected to lie between said lowest pulse level and the middle one of the pulse levels exhibited by the trilevel sandcastle pulse

train. The level of the third reference voltage is selected to lie between said middle pulse level and the highest of the pulse levels exhibited by the trilevel sandcastle pulse train. In accordance with the invention, there is provided in the encoder (external to the integrated circuit bearing the decoder), a keyed circuit which determines the middle pulse level exhibited by the trilevel sandcastle pulse train in accordance with a fourth reference voltage derived from the output terminal of an external voltage divider, which is coupled across the same DC voltage supply as the first (on-chip) voltage divider. Even though the output voltage of the supply may vary with loading changes, temperature variations, etc., tracking of the middle pulse level of the delivered trilevel sandcastle pulse train with the reference voltages supplied to the comparators is ensured, enhancing the reliability of the level discrimination obtained in the decoder.

In accordance with an illustrative embodiment of the present invention, the external encoder also includes a third, selectively enabled, voltage divider connected across the same DC voltage supply as the first and second voltage dividers, with the lowest of said pulse levels determined in accordance with the output of the third voltage divider. During appropriately timed periods, the third voltage divider is effectively disabled in a manner causing the highest pulse level to be responsive to the output of said DC voltage supply without the dividing effect of the third voltage divider. During periods of absence of all of the pulse components of the trilevel sandcastle pulse train, the third voltage divider is subject to modification of its voltage division ratio, with the base level of the trilevel sandcastle pulse train determined in accordance with a modified output of the third voltage divider during said periods of divider modification. With the above-described utilization of the third voltage divider, tracking between the comparator reference voltages of the decoder and the base level of the pulse train, as well as the lowest and highest pulse levels thereof, is also ensured, to further enhance the reliability of the level discrimination obtained in the decoder.

In the accompanying drawing:

Figure 1 illustrates, partially schematically and partially by block representation, a portion of a color television receiver incorporating a trilevel sandcastle pulse encoding/decoding system in accordance with an embodiment of the present invention;

Figure 2 shows a schematic of illustrative circuits for implementing certain of the functions of the system of Figure 1; and

Figure 3 illustrates graphically waveforms of aid in explaining the operation of the Figure 1 system.

In the color television receiver portion illustrated in Figure 1, a plurality of resistors, 21, 22, 23 and 24, are connected in the order named between the positive terminal (+V_s) and the grounded negative terminal of a DC voltage supply 11 to form a voltage divider 20. The resistors (21, 22, 23, 24) are formed on an integrated circuit 13, with the

connection from divider 20 to terminal +V_s of the supply 11 (formed external to the IC) being effected via an interface terminal VI of IC 13. Integrated circuit 13 additionally bears luminance/chrominance signal processing circuits (not illustrated) of the color television receiver, which circuits are illustratively of the form disclosed in the aforementioned U.S. Patent of R. Shanley.

Respective reference voltages, of successively descending magnitudes, appear at the junction of resistors 21 and 22, at the junction of resistors 22 and 23, and at the junction of resistors 23 and 24. These reference voltages are supplied as reference inputs to respective voltage comparators 31, 33 and 35, also realized on the integrated circuit 13. Signals comprising a train of trilevel sandcastle pulses (formed in a manner to be described subsequently) are delivered to the interface terminal SC of integrated circuit 13 and supplied therefrom as signal inputs to the respective comparators 31, 33 and 35. Outputs of the respective comparators 31, 33, 35, indicative of the results of comparison of the voltage level of the incoming signals with the respective reference voltages from divider 20, are delivered to on-chip keying circuits 37 to cause development of a plurality of keying signal outputs used to control various elements of the on-chip luminance/chrominance signal processing circuits.

Voltage divider 20, the comparators (31, 33, 35) and the keying circuits 37 form a sandcastle pulse decoder, which may desirably be of the particular form disclosed in our co-filed Application EP-A-0148606, equivalent to US-A-4555722 of L. Harwood et al. In a decoder form shown in the Harwood, et al. application, the operation of the mid-level voltage comparator 33 is illustratively responsive to an output of the high-level voltage comparator 35 for pulse component discrimination purposes explained in greater detail in said Harwood, et al. application; in reflection of such an operation, Figure 1 shows voltage comparator 33 as accepting an additional input from an element of the keying circuits 37 that respond to the respective comparator outputs.

A trilevel sandcastle pulse train, exhibiting a waveform shown by curve "sc" of Figure 3, is delivered to terminal SC by a trilevel sandcastle pulse former 60, which receives inputs from (a) terminal +V_s of the DC supply 11, (b) the output terminal (G) of a burst gating pulse generator 41, (c) the output terminal (CB) of a retrace blanking pulse generator 43, and (d) the output terminal (B) of an AKB interval pulse generator 53. The sandcastle pulses of waveform "sc" are of a trilevel character, inclusive of retrace blanking pulse components at a first pulse level (V_{RB}) more positive than the base level (V_s) of the pulse train; kinescope bias control interval timing pulse components at a second pulse level (V_{AK}) more positive than the first pulse level; and burst gating pulse components at a third pulse level (V_{BG}) more positive than the second pulse level.

In the arrangement of Figure 1, the burst gating pulse generator 41 and the retrace blanking pulse

generator 43 are realized in integrated circuit form on a second integrated circuit 40, also bearing the receiver's deflection control circuits, which include a horizontal drive pulse generator 45 and a vertical drive pulse generator 47. The output terminals G and CB of the generators 41 and 43 constitute interface terminals of the IC 40. The drive pulse outputs of generators 45 and 47 appear at respective interface terminals H and V of IC 40.

In addition to their delivery to the receiver's horizontal and vertical deflection circuits (not illustrated), the respective drive pulses are coupled via respective resistors 48 and 49 to input terminals H' and V' of logic circuits 51 realized in integrated circuit form on a third integrated circuit 50. The logic circuits 51 function, in response to the inputs from terminals H' and V' to develop a bias control interval timing pulse output at terminal A for delivery as a keying input to the AKB interval pulse generator 53 (also realized in integrated circuit form on IC 50). The integrated circuit 50 desirably also bears the receiver's automatic kinescope bias control circuits not (illustrated), which may advantageously be of the form disclosed in the aforementioned Parker patent (which also shows a suitable arrangement for implementing the function of logic circuits (51).

Illustratively, the keying waves supplied from terminal A to generator 53 have a waveform as shown by curve "a" in Figure 3, and comprise recurring field rate pulses time to occupy a seven-line period within a post-sync portion of the vertical blanking interval of the received signals, which period defines the kinescope bias control interval.

Pursuant to the principles of the present invention, the AKB interval pulse generator 53 cooperates with the trilevel sandcastle pulse former 60 to determine the second (middle) pulse level (V_{AK}) of the trilevel sandcastle pulse train during each of the recurring bias control intervals in accordance with the output of a second voltage divider (65) connected across the output terminals of the DC voltage supply 11. The second voltage divider 65 is formed by resistors 61 and 62, connected in the order named between supply terminal $+V_s$ and ground. A filter capacitor 63 is connected in shunt with divider resistor 62. The voltage division ratio associated with divider 65 is selected to fall between the respective voltage division ratios associated with the outputs of the first voltage divider 20 that appear, respectively, at the junction of resistors 21 and 22, and at the junction of resistors 22 and 23. The output of the second voltage divider 65 is supplied as a reference level input to the AKB interval pulse generator 53 via an interface terminal RL of IC 50.

For an understanding of illustrative techniques that may be employed to achieve the desired control of the V_{AK} level of the trilevel sandcastle pulse train in accordance with the reference level output of divider 65, attention should now be directed to Figure 2, which shows schematic

details for circuits implementing the functions of the trilevel sandcastle pulse former 60 and the AKB interval pulse generator 53 pursuant to a specific embodiment of the present invention.

In Figure 2, the respective output devices of the burst gating pulse generator 41 and the retrace blanking pulse generator 43 of IC 40 of the Figure 1 system are shown as respective NPN transistors 72 and 71, disposed with their emitter electrodes grounded and with their collector electrodes respectively connected to the IC interface terminals G and CB. Terminals G and CB are connected via respective resistors 74 and 73 to a terminal P, linked by a resistor 75 to the positive supply terminal ($+V_s$) of the DC voltage supply 11.

Curve "rb" of Figure 3 illustrates the waveform of a train of negative-going retrace blanking pulses which are applied to the base electrode of transistor 71. Curve "bg" of Figure 3 illustrates the waveform of a train of negative-going burst gating pulses which are applied to the base electrode of transistor 72.

The retrace blanking waveform "rb" includes relatively wide pulse components, recurring at a field rate, which encompass the recurring periods of vertical retrace of the beams of the receiver's color kinescope, and narrower pulse components, recurring at a line rate, which encompass periods of horizontal retrace of said beams lying outside of the vertical retrace blanking intervals. The retrace blanking waveform "rb" is readily subject to formation by combination of suitably timed signals derived from the receiver's horizontal and vertical deflection circuits.

The burst gating waveform "bg" includes pulse components, narrower in width than the horizontal retrace blanking pulse components, which are timed to coincide with "backporch" segments of the horizontal blanking portion of recurring line intervals of the received signals. Illustrative circuitry for developing the burst gating waveform "bg" is disclosed in US-A-4581630 of R. Fernsler et al, which is equivalent to GB-A-2146199.

A resistor 76 (shunted by a speed-up capacitor 77) links terminal P to the output terminal (B) of the circuitry performing the function of the AKB pulse generator 53 of the Figure 1 system, and an additional resistor 78 links terminal B to the sandcastle pulse former output terminal SC.

In the Figure 2 arrangement, the reference level input terminal RL of generator 53 is directly connected to the base electrode of a PNP transistor 81, disposed with its collector electrode grounded. The emitter electrode of transistor 81 is directly connected to the emitter electrode of a first diode-connected NPN transistor 82. The joined base and collector electrodes of transistor 82 are directly connected to the emitter electrode of a second diode-connected transistor 83. The joined base and collector electrodes of transistor 83 are connected via a resistor 84 to the positive terminal ($+V_{cc}$) of an operating potential supply different from that associated with terminal $+V_s$.

Current supplied via resistor 84 forward biases the base-emitter junctions of transistors 81, 82, 83, resulting in development of a potential at terminal R (at the junction of resistor 84 and transistor 83) which is offset in the positive direction from the reference voltage at terminal RL by a voltage ($3V_{be}$) equal to three times the magnitude of the offset potential (V_{be}) exhibited by a forward biased base-emitter junction.

Terminal R is directly connected to the base electrode of an NPN transistor 85 disposed as an emitter-follower, with its collector electrode directly connected to the $+V_{cc}$ supply terminal. An NPN transistor 86, disposed with its collector electrode directly connected to the emitter electrode of transistor 85, and with its emitter electrode grounded, serves as a current source for the emitter-follower transistor 85. The current drawn by the current source transistor 86 is determined by a biasing circuit comprising a resistor 88 connected between the $+V_{cc}$ supply terminal and the base electrode of transistor 86, and a diode-connected NPN transistor 87 shunting the base-emitter path of transistor 86. The diode-connected transistor 87 is disposed with its joined base and collector electrodes directly connected to the base electrode of transistor 86, and with its emitter electrode grounded.

A resistor 89 links the emitter electrode of the emitter-follower transistor 85 to the base electrode of a multiple-emitter NPN transistor 91, disposed with its collector electrode directly connected to the $+V_{cc}$ supply terminal. An NPN control transistor 90 is disposed with its collector electrode directly connected to the base electrode of the multiple-emitter transistor 91, with its emitter electrode grounded, and with its base electrode connected to the keying wave input terminal A.

A first emitter electrode (92) of transistor 91 is directly connected to the base electrode of a first NPN output transistor 94. Output transistor 94 is arranged with its emitter electrode directly connected to the output terminal B, and with its collector electrode directly connected to the $+V_{cc}$ supply terminal.

A second emitter electrode (93) of transistor 91 is directly connected to the base electrode of an NPN emitter-follower transistor 95, disposed with its collector electrode directly connected to the $+V_{cc}$ supply terminal. A resistor 96 links the emitter electrode of emitter-follower transistor 95 to the base electrode of a second NPN output transistor 99, disposed with its collector electrode directly connected to output terminal B. A resistor 100 returns the emitter electrode of output transistor 99 to ground. A diode-connected NPN transistor 97 is arranged with its joined base and collector electrodes directly connected to the base electrode of output transistor 99, and with its emitter electrode returned to ground via a resistor 98.

In operation of the Figure 2 arrangement, when a negative-going AKB control interval timing pulse component of waveform "a" appears at the

keying wave input terminal A, control transistor 90 is cut off. Under these circumstances, the voltage at the base electrode of transistor 91 is elevated sufficiently to enable transistors 91, 94, 95, 97 and 99 to simultaneously conduct. With output transistors 94 and 99 conducting, the generator 53 presents a very low impedance to output terminal B. With the output impedance of generator 53 appreciably lower than the impedance exhibited by resistor 76 during each keying interval, terminal B is effectively clamped to a voltage which is offset in a negative direction from the voltage at terminal R by a $3V_{be}$ amount (neglecting as insignificant the slight voltage drop developed across resistor 89 by the base current of the conducting transistor 91). The negative offset introduced by the voltage drops across the forward-biased base-emitter junctions of transistors 85, 91 and 94 effectively cancels the effects of the positive offset introduced by the voltage drops across the forward-biased base-emitter junctions of transistors 81, 82, and 83. Thus, the output voltage at terminal B during each keying interval is directly determined by (and in this instance, substantially equal to) the reference voltage at the reference level input terminal RL (and is effectively independent of the supply voltage at the operating voltage supply terminal $+V_{cc}$ and any variations to which such supply voltage may be subject).

During periods outside the AKB control interval, when waveform "a" at the keying wave input terminal A exhibits its base level, control transistor 90 is rendered conducting to depress the voltage at the base electrode of transistor 91 sufficiently so as to disable transistors 91, 94, 95, 97 and 99. With output transistors 94 and 99 simultaneously cut off under these circumstances, the output of generator 53 is effectively open-circuited and output terminal B is free to follow the voltage excursions at terminal P.

To appreciate the nature of the voltage excursions at terminal P, one must consider the effects of the keying of transistors 71 and 72. During the appearance of a negative-going retrace blanking pulse component at the base electrode of transistor 71, transistor 71 is cut off. During the periods intervening the successive retrace blanking pulse components, transistor 71 is strongly conducting. During the appearance of a negative-going burst gating pulse component at the base electrode of transistor 72, transistor 72 is cut off. During the periods intervening the successive burst gating pulse components, transistor 72 is strongly conducting.

As a consequence of the above-described operations, a train of sandcastle pulses of bilevel form is developed at terminal P. During periods of coincidence of the base levels of waveforms "rb" and "bg" (e.g., during trace portions of active line intervals), transistors 71 and 72 are simultaneously conducting. Under these circumstances, a voltage divider is formed across the DC voltage supply 11, which divider comprises resistor 75 in series with the parallel combination of

resistors 73 and 74. The voltage division ratio of this voltage divider is such as to establish a base level at terminal P at a relatively low positive voltage.

During appearances of those portions of each retrace blanking pulse component of waveform "rb" which do not coincide with appearances of the burst gating pulse components of waveform "bg", transistor 71 is cut off while transistor 72 is in a conducting state. Under such circumstances, resistor 73 is open-circuited and a modified voltage divider is formed across the supply 11, which modified voltage divider comprises resistor 75 in series with resistor 74 only. The voltage division ratio of the modified voltage divider is such as to elevate the voltage at terminal P to a retrace blanking pulse level more positive than the aforementioned base level.

During appearances of the burst gating pulse components of waveform "bg" (which always coincide with appearances of portions of the retrace blanking pulse components of waveform "rb"), transistors 71 and 72 are simultaneously cut off. Under such circumstances, resistors 73 and 74 are both open-circuited, and the voltage at terminal P rises to a burst gating pulse level, higher than the retrace blanking pulse level, and at, or in the vicinity of, the voltage at supply terminal V_s .

Due to the previously explained clamping effect of the operation of generator 53, the excursions between base, retrace blanking, and burst gating levels at terminal P are not followed at terminal B during each bias control interval. During the intervening periods, however, the voltage at terminal B is free to follow such excursions. As a consequence, the pulse train delivered to terminal SC is of the desired trilevel form shown by waveform "sc".

The middle pulse level (V_{AK}) of the delivered trilevel sandcastle pulse train is determined, as explained above, by the output of the second voltage divider 65 (Figure 1) supplied to terminal RL. The lowest pulse level (V_{RB}) of the delivered trilevel sandcastle pulse train is determined in accordance with the output of an additional voltage divider (75, 74) coupled across the output terminals of supply 11. The resistance values for resistors 75 and 74 are selected so as to associate a voltage division ratio with this additional voltage divider which falls between the respective voltage division ratios associated with the outputs of the first voltage divider 20 (Figure 1) that appear, respectively, at the junction of resistors 22 and 23, and at the junction of resistors 23 and 24.

The base level (V_B) of the delivered trilevel sandcastle pulse is determined in accordance with the output of divider 75, 74 when modified by the effective shunting of resistor 74 by resistor 73. The resistance value for resistor 73 is selected so as to associate a voltage division ratio with the modified voltage divider 75, 74/73 which ensures a base level significantly below the reference voltage developed at the junction of resistors 23 and 24.

The disabling of the additional divider by the concurrent open-circuiting of resistors 73 and 74

permits determination of the highest pulse level (V_{BA}) at, or in the vicinity of, the voltage at the supply terminal $+V_s$. In one contemplated use of the Figure 2 arrangement the associated decoder includes a PNP clamping transistor with its emitter electrode linked to terminal SC, with its collector electrode grounded, and with its base electrode connected to an additional intermediate point on voltage divider 20, located between terminal $+V_s$ and the junction of resistors 21 and 22. With use of such a clamping transistor, the burst gating pulse level of the pulse train delivered to the comparators (31, 33, 35; Figure 1) will be clamped to the reference voltage exhibited at said additional intermediate point of divider 20. In the absence of the clamping transistor, the burst gating pulse level of the delivered sandcastle pulse train effectively corresponds directly to the voltage at terminal $+V_s$. In either instance, a desirable tracking relationship is established between the burst gating pulse level (V_{BA}) and the reference inputs to the comparators.

Thus, in operation of the illustrative embodiment of the present invention, tracking between the various levels of the trilevel sandcastle pulser train and the reference inputs to the decoder's comparators is automatically obtained. This assures reliable discrimination between the respective pulse train levels by the comparators, as desired for accurate decoding, despite the occurrence of supply variations.

One contemplated output of the keying circuits 37 of Figure 1 comprises burst gating pulse components. These components are separated from the trilevel sandcastle pulses at terminal SC, for use in voltage comparator keying in a system for stabilization of the DC levels of the color signal outputs of the luminance/chrominance signal processing circuits on IC 13. In our co-filed Application EP-A-0145490, which is equivalent to US-A-4554577 of R. Shanley et al, it is recognized as desirable, for error reduction purposes, that keying of the stabilization system's comparators should be prevented during at least a portion of each vertical sync interval of the received signal. Moreover, it is proposed therein, to ensure such keying prevention, that the trilevel sandcastle pulses which are delivered to the luminance/chrominance IC should be freed of at least some of the burst gating pulse components during the vertical sync interval. A desirable technique for achieving the selective elimination of the burst gating pulse components is disclosed in our co-filed Application EP-A-0145491 equivalent to US-A-4583121 of T. Yost. In the Yost patent a modification of the burst gating pulse generator circuitry disclosed in the aforementioned Fernsler et al. US-A-4581630 is disclosed in which gating pulse generation is suppressed throughout a selected portion of each vertical sync interval.

Accordingly, in one contemplated embodiment of present invention, the burst gating pulse generator employed to supply an input to transistor 72 in the Figure 2 arrangement desirably incorporates gating pulse generation suppression

during vertical sync intervals in the manner of the aforementioned Yost patent application. In such an arrangement, the pulse train delivered to the base electrode of transistor 72 will exhibit a version of the waveform "bg" in which burst gating pulses are absent during at least a selected portion of the vertical sync interval. The resultant trilevel sandcastle pulse train appearing at terminal SC will conform to a version of the waveform "sc" in which excursions to the V_{BE} level are absent throughout the selected portion of vertical sync interval.

Claims

1. A trilevel sandcastle pulse encoding/decoding system, including signal processing circuits disposed on an integrated circuit chip, comprising:

means (60), external to said integrated circuit chip, for supplying a train of trilevel pulses, inclusive of first pulse components exhibiting a first voltage level (V_{BE}), second pulse components exhibiting a second voltage level (V_{RB}) lower than said first voltage level, and third pulse components exhibiting a third voltage level (V_{AK}) intermediate said first and second voltage levels, to a terminal (SC) of said integrated circuit chip;

a source (11) of DC voltage;

a first voltage divider (20), disposed on said integrated circuit chip and connected across said DC voltage source;

a first voltage comparator (31), disposed on said integrated circuit chip, for comparing the voltage level of said pulse train with the level of a first reference voltage said first voltage comparator having a reference input connected to a first intermediate point (21—22) on said first voltage divider, at which said first reference voltage appears, and a signal input coupled to said chip terminal (SC);

a second voltage comparator (35), disposed on said integrated circuit chip, for comparing the voltage level of said pulse train with the level of a second reference voltage less than said first reference voltage; said second voltage comparator having a reference input connected to a second intermediate point (23—24) on said first voltage divider, at which said second reference voltage appears, and a signal input coupled to said chip terminal;

a third voltage comparator (33), disposed on said integrated circuit chip, for comparing the voltage level of said pulse train with the level of a third reference voltage, intermediate said first and second reference voltages said third voltage comparator having a reference input connected to a third intermediate point (22—23) on said first voltage divider, at which said third reference voltage appears, and a signal input coupled to said chip terminal; and

means (37), disposed on said integrated circuit chip and responsive to outputs of said voltage comparators, for controlling the operation of said signal processing circuits;

said trilevel pulse train supplying means (60) characterized by:

a second voltage divider (65), external to said integrated circuit chip and connected across said DC voltage source; said second voltage divider having a divider output terminal exhibiting a voltage division ratio intermediate the voltage division ratios exhibited at said first and third intermediate points on said first voltage divider; and

means (53), disposed external to said integrated circuit chip, coupled to said second divider output terminal, and operative during appearances of said third pulse components (V_{AK}), for determining the voltage level of said pulse train during said appearances of said third pulse components in accordance with the voltage appearing at said second divider output terminal.

2. A system in accordance with Claim 1 characterized in that it comprises a color television receiver for displaying color images in response to composite video signals inclusive of respective image-representative luminance and chrominance components, said image-representative components being absent during horizontal blanking portions of successive line intervals within periodic field intervals, and also absent during the vertical blanking portion of each field interval, wherein said signal processing circuitry processes said image-representative luminance and chrominance components, and wherein each of said third pulse components (V_{AK}) of said pulse train encompasses a plurality of successive line intervals (7H) within one of said vertical blanking portions.

3. A system in accordance with Claim 2, characterized in that said trilevel pulse train supplying means (60) includes:

a third, selectively enabled, voltage divider (75, 74), external to said integrated circuit chip and connected across said DC voltage source; said third voltage divider having a second divider output terminal (P) normally exhibiting a voltage division ratio intermediate the voltage division ratios exhibited at said second and third intermediate points on said first voltage divider; and

means (43), external to said integrated circuit chip, for determining the voltage level of said pulse train in accordance with the voltage at said second divider output terminal during the appearances of said second pulse components (V_{RB}).

4. A system in accordance with Claim 3, characterized in that said trilevel pulse train supplying means includes:

means (41), external to said integrated circuit chip, for effectively disabling said third voltage divider during appearances of said first pulse components (V_{BE}) in such manner as to cause the voltage level of said pulse train to be responsive to the output of said DC voltage source without the dividing effect of said third voltage divider during said appearances of said first pulse components.

5. A system in accordance with Claim 4, charac-

during vertical sync intervals in the manner of the aforementioned Yost patent application. In such an arrangement, the pulse train delivered to the base electrode of transistor 72 will exhibit a version of the waveform "bg" in which burst gating pulses are absent during at least a selected portion of the vertical sync interval. The resultant trilevel sandcastle pulse train appearing at terminal SC will conform to a version of the waveform "sc" in which excursions to the V_{BG} level are absent throughout the selected portion of vertical sync interval.

Claims

1. A trilevel sandcastle pulse encoding/decoding system, including signal processing circuits disposed on an integrated circuit chip, comprising:

means (60), external to said integrated circuit chip, for supplying a train of trilevel pulses, inclusive of first pulse components exhibiting a first voltage level (V_{BG}), second pulse components exhibiting a second voltage level (V_{RB}), lower than said first voltage level, and third pulse components exhibiting a third voltage level (V_{AK}) intermediate said first and second voltage levels, to a terminal (SC) of said integrated circuit chip;

a source (11) of DC voltage;

a first voltage divider (20), disposed on said integrated circuit chip and connected across said DC voltage source;

a first voltage comparator (31), disposed on said integrated circuit chip, for comparing the voltage level of said pulse train with the level of a first reference voltage said first voltage comparator having a reference input connected to a first intermediate point (21—22) on said first voltage divider, at which said first reference voltage appears, and a signal input coupled to said chip terminal (SC);

a second voltage comparator (35), disposed on said integrated circuit chip, for comparing the voltage level of said pulse train with the level of a second reference voltage less than said first reference voltage; said second voltage comparator having a reference input connected to a second intermediate point (23—24) on said first voltage divider, at which said second reference voltage appears, and a signal input coupled to said chip terminal;

a third voltage comparator (33), disposed on said integrated circuit chip, for comparing the voltage level of said pulse train with the level of a third reference voltage, intermediate said first and second reference voltages said third voltage comparator having a reference input connected to a third intermediate point (22—23) on said first voltage divider, at which said third reference voltage appears, and a signal input coupled to said chip terminal; and

means (37), disposed on said integrated circuit chip and responsive to outputs of said voltage comparators, for controlling the operation of said signal processing circuits;

said trilevel pulse train supplying means (60) characterized by:

a second voltage divider (65), external to said integrated circuit chip and connected across said DC voltage source; said second voltage divider having a divider output terminal exhibiting a voltage division ratio intermediate the voltage division ratios exhibited at said first and third intermediate points on said first voltage divider; and

means (53), disposed external to said integrated circuit chip, coupled to said second divider output terminal, and operative during appearances of said third pulse components (V_{AK}), for determining the voltage level of said pulse train during said appearances of said third pulse components in accordance with the voltage appearing at said second divider output terminal.

2. A system in accordance with Claim 1 characterized in that it comprises a color television receiver for displaying color images in response to composite video signals inclusive of respective image-representative luminance and chrominance components, said image-representative components being absent during horizontal blanking portions of successive line intervals within periodic field intervals, and also absent during the vertical blanking portion of each field interval, wherein said signal processing circuitry processes said image-representative luminance and chrominance components, and wherein each of said third pulse components (V_{AK}) of said pulse train encompasses a plurality of successive line intervals (7H) within one of said vertical blanking portions.

3. A system in accordance with Claim 2, characterized in that said trilevel pulse train supplying means (60) includes:

a third, selectively enabled, voltage divider (75, 74), external to said integrated circuit chip and connected across said DC voltage source; said third voltage divider having a second divider output terminal (P) normally exhibiting a voltage division ratio intermediate the voltage division ratios exhibited at said second and third intermediate points on said first voltage divider; and

means (43), external to said integrated circuit chip, for determining the voltage level of said pulse train in accordance with the voltage at said second divider output terminal during the appearances of said second pulse components (V_{RB}).

4. A system in accordance with Claim 3, characterized in that said trilevel pulse train supplying means includes:

means (41), external to said integrated circuit chip, for effectively disabling said third voltage divider during appearances of said first pulse components (V_{BG}) in such manner as to cause the voltage level of said pulse train to be responsive to the output of said DC voltage source without the dividing effect of said third voltage divider during said appearances of said first pulse components.

5. A system in accordance with Claim 4, charac-



terized in that said first pulse components (V_{BQ}) of said pulse train normally recur at a line rate, but are absent during appearances of said third pulse components (V_{AK}), and each of said first pulse components is timed to coincide with a backporch segment of the horizontal blanking portion of a line interval.

6. A system in accordance with Claim 5, characterized in that said second pulse components (V_{RB}) of said pulse train occur during segments of said horizontal and vertical blanking portions not overlapping with said second (V_{RB}) and third (V_{AK}) pulse components.

7. A system in accordance with Claim 6, characterized in that said third voltage divider (75, 73, 74) is subject to modification during periods of absence of all said pulse components in such manner as to then exhibit, at said second divider output terminal, a voltage division ratio smaller than the voltage division ratio exhibited at said second intermediate point (22—23) on said first voltage divider, the base (V_B) level of said pulse train being determined in accordance with the voltage at said second divider output terminal during said periods of absence of all said pulse components.

Patentansprüche

1. Codier/Decodiersystem für Dreiniveau-Sandcastleimpulse, mit Signalverarbeitungsschaltungen, die sich auf einem integrierten Schaltungsplättchen befinden, bestehend aus:

einer außerhalb des integrierten Schaltungsplättchens befindlichen Einrichtung (60) zur Lieferung eines Zuges von Dreiniveau-Impulsen an eine Klemme (SC) des integrierten Schaltungsplättchens, wobei diese Dreiniveau-Impulse eine erste Impulskomponente enthalten, die einen ersten Spannungspegel (V_{BQ}) hat, eine zweite Impulskomponente, die einen zweiten Spannungspegel (V_{RB}) hat, der niedriger ist als der erste Spannungspegel, und eine dritte Impulskomponente, die einen dritten Spannungspegel (V_{AK}) hat, der zwischen dem ersten und dem zweiten Spannungspegel liegt;

einer Quelle (11) für eine Gleichspannung;

einem ersten Spannungsteiler (20), der sich auf dem integrierten Schaltungsplättchen befindet und über die Gleichspannungsquelle geschaltet ist;

einem auf dem integrierten Schaltungsplättchen befindlichen ersten Spannungsvergleicher (31) zum Vergleichen des Spannungspegels des Impulszuges mit dem Pegel einer ersten Referenzspannung, mit einem Referenzeingang, der an einen ersten Zwischenpunkt (21—22) am ersten Spannungsteiler angeschlossen ist, wo die erste Referenzspannung erscheint, und mit einem Signaleingang, der an die besagte Klemme (SC) des Schaltungsplättchens gekoppelt ist;

einem auf dem integrierten Schaltungsplättchen befindlichen zweiten Spannungsvergleicher (35) zum Vergleichen des Spannungspegels des Impulszuges mit dem Pegel einer zweiten Referenzspannung, die niedriger als die erste Referenzspannung ist, mit einem Referenzeingang, der mit einem zweiten Zwischenpunkt (23—24) am ersten Spannungsteiler verbunden ist, wo die zweite Referenzspannung erscheint, und mit einem Signaleingang, der an die besagte Klemme des Schaltungsplättchens gekoppelt ist;

einem auf dem integrierten Schaltungsplättchen befindlichen dritten Spannungsvergleicher (33) zum Vergleichen des Spannungspegels des Impulszuges mit dem Pegel einer dritten Referenzspannung, die zwischen der ersten und der zweiten Referenzspannung liegt, mit einem Referenzeingang, der an einen dritten Zwischenpunkt (22—23) am ersten Spannungsteiler angeschlossen ist, wo die dritte Referenzspannung erscheint, und mit einem Signaleingang, der an die besagte Klemme des Schaltungsplättchens gekoppelt ist; und

einer auf dem integrierten Schaltungsplättchen befindlichen Einrichtung (37), die auf die Ausgangsgrößen der Spannungsteiler anspricht, um den Betrieb der Signalverarbeitungsschaltungen zu steuern;

wobei die den Dreiniveau-Impulszug liefernde Einrichtung (60) gekennzeichnet ist durch:

einen zweiten Spannungsteiler (65), der sich außerhalb des integrierten Schaltungsplättchens befindet und über die Gleichspannungsquelle geschaltet ist und der eine Teiler-Ausgangsklemme für ein Spannungsteilungsverhältnis hat, das zwischen den Spannungsteilungsverhältnissen an dem ersten und an dem dritten Zwischenpunkt des ersten Spannungsteilers liegt; und

eine außerhalb des integrierten Schaltungsplättchens befindliche Einrichtung (53), die mit der Ausgangsklemme des zweiten Teilers gekoppelt ist und während der Erscheinungszeiten der dritten Impulskomponenten (V_{AK}) wirksam ist, um den Spannungspegel des Impulszuges während der Erscheinungszeiten der dritten Impulskomponente entsprechend der an der Ausgangsklemme des zweiten Teilers erscheinenden Spannung zu bestimmen.

2. System nach Anspruch 1, dadurch gekennzeichnet, daß es einen Farbfernsehempfänger aufweist, um Farbbilder als Antwort auf zusammengesetzte Videosignale wiederzugeben, die bildrepräsentative Leuchtdichte- und Farbartkomponenten enthalten, welche während Horizontal-austastabschnitten aufeinanderfolgender Zeilenintervalle innerhalb periodischer Teilbildintervalle fehlen und außerdem während des Vertikal-austastabschnitts eines jeden Teilbildintervalls fehlen, wobei die Signalverarbeitungsschaltung die bildrepräsentativen Leuchtdichte- und Farbartkomponenten verarbeitet und wobei jede der dritten Impulskomponenten (V_{AK}) des Impulszuges eine Mehrzahl aufeinanderfolgender Zeilenintervalle (7H) innerhalb eines der Vertikalaustastabschnitte umfaßt.

3. System nach Anspruch 2, dadurch gekennzeichnet, daß die Einrichtung (60) zur Lieferung des Dreiniveau-Impulszuges folgendes enthält:



einen dritten, selektiv eingeschalteten Spannungsteiler (75, 74), der sich außerhalb des integrierten Schaltungsplättchens befindet und über die Gleichspannungsquelle geschaltet ist und der eine zweite Teiler-Ausgangsklemme (P) hat, die normalerweise ein Spannungsteilungsverhältnis liefert, das zwischen den Spannungsteilungsverhältnissen am zweiten und am dritten Zwischenpunkt der ersten Spannungsteilers liegt; und

eine außerhalb des integrierten Schaltungsplättchens befindliche Einrichtung (43), um den Spannungspegel des Impulszuges entsprechend der Spannung an der zweiten Teiler-Ausgangsklemme während der Erscheinungszeiten der zweiten Impulskomponenten (V_{RB}) zu bestimmen.

4. System nach Anspruch 3, dadurch gekennzeichnet, daß die Einrichtung zur Lieferung des Dreiniveau-Impulszuges folgendes enthält:

eine außerhalb des integrierten Schaltungsplättchens befindliche Einrichtung (41) zur effektiven Abschaltung des dritten Spannungsteilers während der Erscheinungszeiten der ersten Impulskomponenten (V_{BG}) in solcher Weise, daß der Spannungspegel des Impulszuges während der Erscheinungszeiten der ersten Impulskomponenten auf den Ausgang der Gleichspannungsquelle ohne den teilenden Effekt des dritten Spannungsteilers anspricht.

5. System nach Anspruch 4, dadurch gekennzeichnet, daß die ersten Impulskomponente (V_{BG}) des Impulszuges normalerweise mit einer Zeilenfrequenz wiederkehren, jedoch während der Erscheinungszeiten der dritten Impulskomponenten (V_{AK}) fehlen, und daß jede der ersten Impulskomponenten zeitlich so liegt, daß sie mit einer hinteren Schwarzscher des Horizontalaustabschnittes eines Zeilenintervalls zusammenfällt.

6. System nach Anspruch 5, dadurch gekennzeichnet, daß die zweiten Impulskomponenten (V_{RB}) des Impulszuges während Teilbereichen der Horizontal- und Vertikalaustabschnitte auftreten, die sich nicht mit den zweiten (V_{RB}) und den dritten (V_{AK}) Impulskomponenten überlappen.

7. System nach Anspruch 6, dadurch gekennzeichnet, daß der dritte Spannungsteiler (75, 73, 74) während der Zeiten des Fehlens aller Impulskomponenten derart modifiziert wird, daß an der Ausgangsklemme des zweiten Teilers ein Spannungsteilungsverhältnis gilt, welches kleiner ist als das Spannungsteilungsverhältnis am zweiten Zwischenpunkt (22—23) des ersten Spannungsteilers, und daß der Grundpegel (V_B) des Impulszuges entsprechend der Spannung bestimmt wird, die an der Ausgangsklemme des zweiten Teilers während der Zeiten des Fehlens aller Impulskomponenten herrscht.

Revendications

1. Système de codage/décodage d'une impulsion en château de sable à trois niveaux, com-

prenant des circuits de traitement de signaux disposés sur une pastille de circuit intégré, comprenant:

un moyen (60) à l'extérieur de ladite pastille de circuit intégré, pour fournir un train d'impulsions à trois niveaux, comprenant des premières composantes impulsionnelles présentant un premier niveau de tension (V_{BG}), des secondes composantes impulsionnelles présentant un second niveau de tension (V_{RB}) plus bas que ledit premier niveau de tension et des troisièmes composantes impulsionnelles présentant un troisième niveau de tension (V_{AK}) entre lesdits premier et second niveau de tension, à une borne (SC) de ladite pastille de circuit intégré;

une source (11) de tension continue;

un premier diviseur de tension (20) disposé sur ladite pastille de circuit intégré et connecté aux bornes de ladite source de tension continue;

un premier comparateur de tension (31) disposé sur ladite pastille de circuit intégré, pour comparer le niveau de tension dudit train d'impulsions au niveau d'une première tension de référence, ledit premier comparateur de tension ayant une entrée de référence connectée à un premier point intermédiaire (21—22) sur ledit premier diviseur de tension, auquel apparaît ladite première tension de référence, et une entrée de signaux couplée à ladite borne (SC) de la pastille;

un second comparateur de tension (35) disposé sur ladite pastille de circuit intégré, pour comparer le niveau de tension dudit train d'impulsions au niveau d'une seconde tension de référence plus faible que ladite première tension de référence; ledit second comparateur de tension ayant une entrée de référence connectée à un second point intermédiaire (23—24) sur ledit premier diviseur de tension, où apparaît ladite seconde tension de référence, et une entrée de signaux couplée à ladite borne de la pastille;

un troisième comparateur de tension (33) disposé sur ladite pastille de circuit intégré, pour comparer le niveau de tension dudit train d'impulsions au niveau d'une troisième tension de référence, entre lesdites première et seconde tensions de référence; ledit troisième comparateur de tension ayant une entrée de référence connectée à un troisième point intermédiaire (22—23) dudit premier diviseur de tension, où apparaît ladite troisième tension de référence, et une entrée de signaux couplée à ladite borne de la pastille; et

un moyen (37) disposé sur ladite pastille de circuit intégré et répondant aux sorties desdits comparateurs de tension, pour contrôler le fonctionnement desdits circuits de traitement de signaux;

ledit moyen (60) fournissant le train d'impulsions à trois niveaux étant caractérisé par:

un second diviseur de tension (65) à l'extérieur de ladite pastille de circuit intégré et connecté aux bornes de ladite source de tension continue; ledit second diviseur de tension ayant une borne de sortie de diviseur présentant un rapport de



division de tension entre les rapports de division de tension présentés auxdits premier et troisième points intermédiaires sur ledit premier diviseur de tension; et

un moyen (53), disposé à l'extérieur de ladite pastille de circuit intégré, couplé à la borne de sortie dudit second diviseur, et servant, pendant des apparitions desdites troisièmes composantes impulsionnelles (V_{AK}), à déterminer le niveau de tension dudit train d'impulsions pendant lesdites apparitions desdites troisièmes composantes impulsionnelles selon la tension apparaissant à la borne de sortie dudit second diviseur.

2. Système selon la revendication 1, caractérisé en ce qu'il comprend un récepteur de télévision en couleur pour visualiser des images en couleur en réponse à des signaux vidéo composites comprenant des composantes respectives de luminance et de chrominance représentatives de l'image, lesdites composantes représentatives de l'image étant absentes pendant des parties d'effacement horizontal d'intervalles successifs de ligne pendant des intervalles périodiques de trame, et également absentes pendant la partie d'effacement vertical de chaque intervalle de trame, où ledit montage de traitement de signaux traite lesdites composantes de luminance et de chrominance représentatives de l'image, et où chacune desdites troisièmes composantes impulsionnelles (V_{AK}) dudit train d'impulsions contient un certain nombre d'intervalles successifs de ligne (7H) dans l'une desdites parties d'effacement vertical.

3. Système selon la revendication 2, caractérisé en ce que ledit moyen fournissant le train d'impulsions à trois niveaux (60) comprend:

un troisième diviseur de tension, sélectivement validé (75, 74), à l'extérieur de ladite pastille de circuit intégré, et connecté aux bornes de ladite source de tension continue; ledit troisième diviseur de tension ayant une seconde borne de sortie de diviseur (P) présentant normalement un rapport de division de tension entre les rapports de division de tension présentés auxdits second et troisième points intermédiaires dudit premier diviseur de tension; et

un moyen (43) à l'extérieur de ladite pastille de circuit intégré, pour déterminer le niveau de tension dudit train d'impulsions selon la tension à

ladite seconde borne de sortie de diviseur pendant les apparitions desdites secondes composantes impulsionnelles (V_{RB}).

4. Système selon la revendication 3, caractérisé en ce que ledit moyen fournissant le train d'impulsions à trois niveaux comprend:

un moyen (41), à l'extérieur de ladite pastille de circuit intégré, pour inhiber efficacement ledit troisième diviseur de tension pendant des apparitions desdites premières composantes impulsionnelles (V_{BG}) de manière à forcer le niveau de tension dudit train d'impulsions à être sensible à la sortie de ladite source de tension continue sans l'effet de division dudit troisième diviseur de tension pendant lesdites apparitions desdites premières composantes impulsionnelles.

5. Système selon la revendication 4, caractérisé en ce que lesdites premières composantes impulsionnelles (V_{BG}) dudit train d'impulsions sont normalement récurrentes à une fréquence horizontale, mais sont absentes pendant des apparitions desdites troisièmes composantes impulsionnelles (V_{AK}) et chacune desdites premières composantes impulsionnelles est temporisée pour coïncider avec un segment de palier arrière de la partie d'effacement horizontal d'un intervalle de ligne.

6. Système selon la revendication 5, caractérisé en ce que lesdites secondes composantes impulsionnelles (V_{RB}) dudit train d'impulsions se produisent pendant des segments des parties d'effacement horizontal et vertical ne se chevauchant pas avec lesdites secondes (V_{RB}) et troisièmes (V_{AK}) composantes impulsionnelles.

7. Système selon la revendication 6, caractérisé en ce que ledit troisième diviseur de tension (75, 73, 74) est sujet à une modification pendant des périodes d'absence de toutes lesdites composantes impulsionnelles de manière à présenter alors, à ladite seconde borne de sortie de diviseur, un rapport de division de tension plus petit que le rapport de division de tension présenté audit second point intermédiaire (22—23) sur ledit premier diviseur de tension, le niveau de base (V_B) dudit train d'impulsions étant déterminé selon la tension à ladite seconde borne de sortie de diviseur pendant des périodes d'absence de toutes lesdites composantes impulsionnelles.

