

ABSTRACT OF THE DISCLOSURE

A synchronous semiconductor storage device includes: an internal clock activation signal generation circuit for generating an internal clock activation signal `cke_c` and a latch signal `cke1` based on a system clock signal `CLK` and a clock activation signal `CKE` each having a series of pulses; a CKE latch clock control signal generation circuit for generating, based on the internal clock activation signal `cke_c`, the latch signal `cke1`, the system clock signal `CLK`, and the clock activation signal `CKE`, a CKE latch clock control signal `cke_x` which controls activation/inactivation of a CKE latch clock signal, and an internal clock signal generation circuit for generating an internal clock signal `clk_in` based on the internal clock activation signal `cke_c` and the system clock signal `CLK`, wherein stored data corresponding to a plurality of external signals including a control signal and an address signal are transmitted in synchronization with the internal clock signal `clk_in`.

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