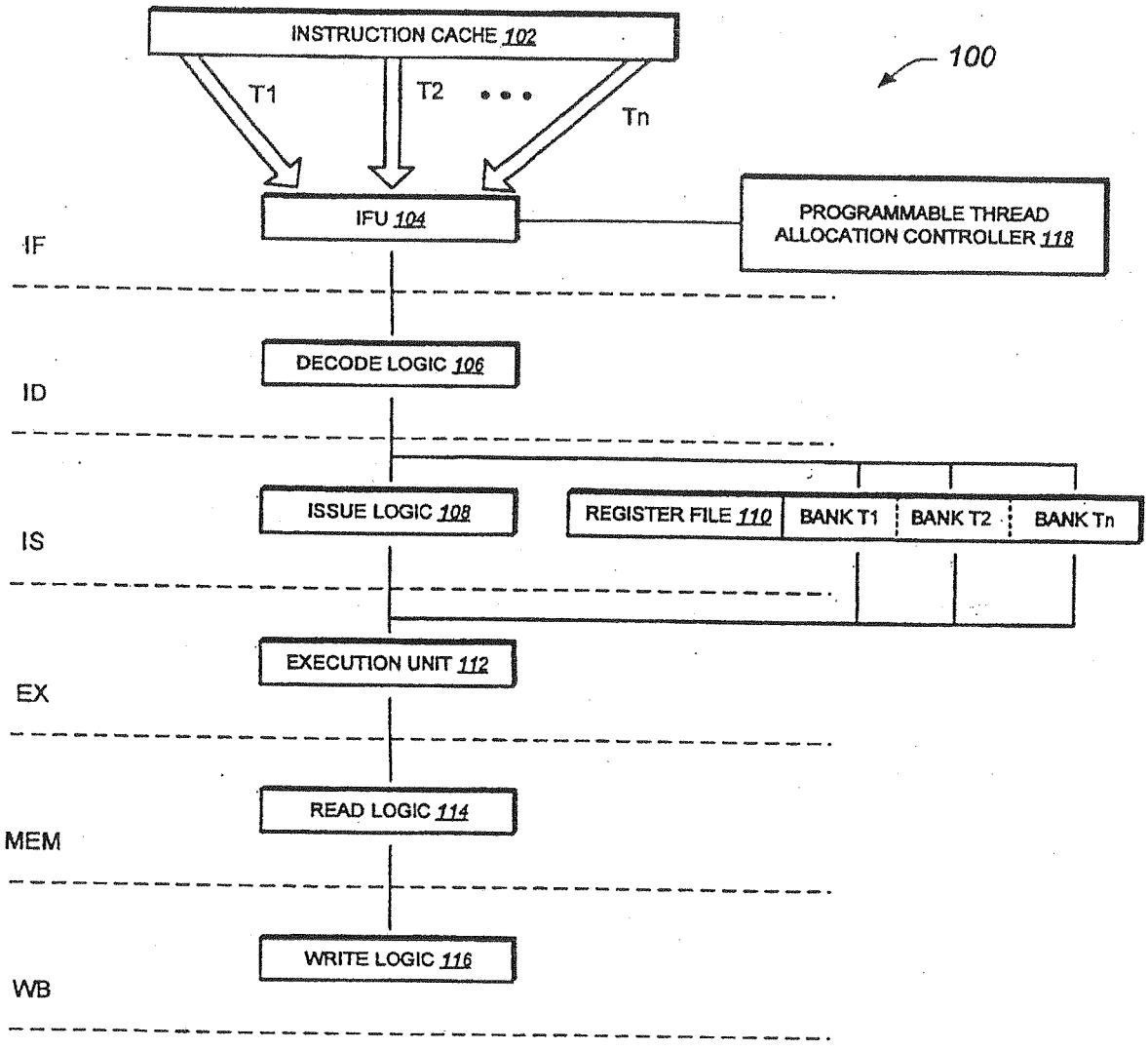

INSTRUCTION CACHE 102
100
T1
T2
Tn
IFU 104
PROGRAMMABLE THREAD ALLOCATION CONTROLLER 118
IF
DECODE LOGIC 106
ID
ISSUE LOGIC 108
REGISTER FILE 110
BANK T1
BANK T2
BANK Tn
IS
EXECUTION UNIT 112
EX
READ LOGIC 114
MEM
WRITE LOGIC 116
WB

FIG._1

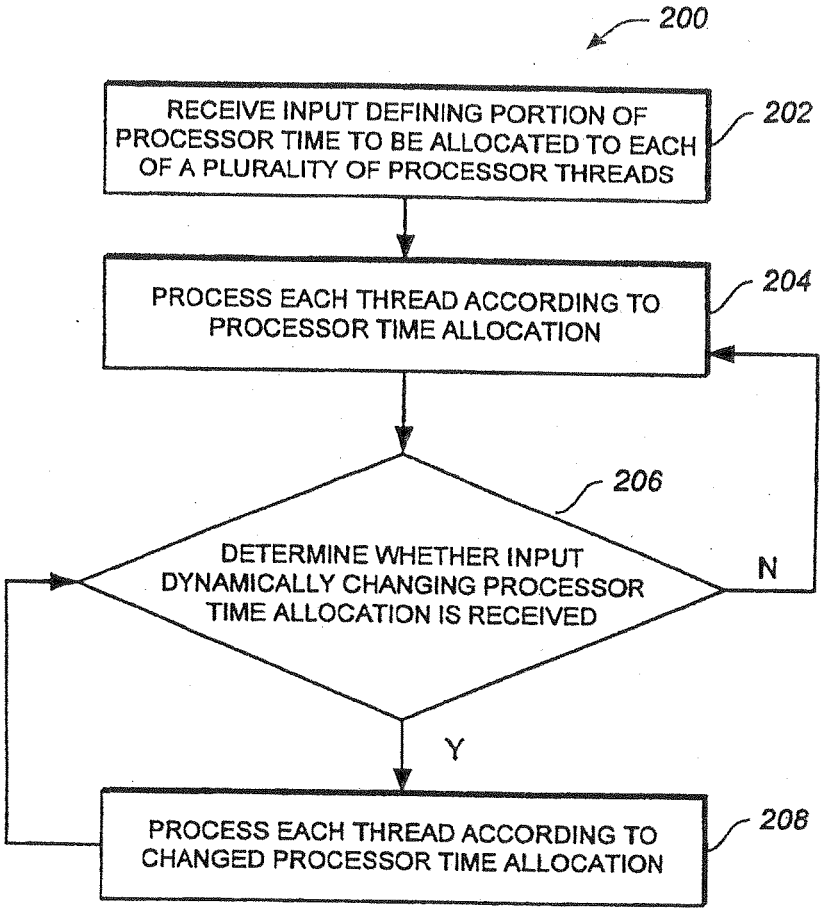

200
RECEIVE INPUT DEFINING PORTION OF PROCESSOR TIME TO BE ALLOCATED TO EACH OF A PLURALITY OF PROCESSOR THREADS
202
PROCESS EACH THREAD ACCORDING TO PROCESSOR TIME ALLOCATION
204
206
DETERMINE WHETHER INPUT DYNAMICALLY CHANGING PROCESSOR TIME ALLOCATION IS RECEIVED
N
Y
PROCESS EACH THREAD ACCORDING TO CHANGED PROCESSOR TIME ALLOCATION
208

FIG._2

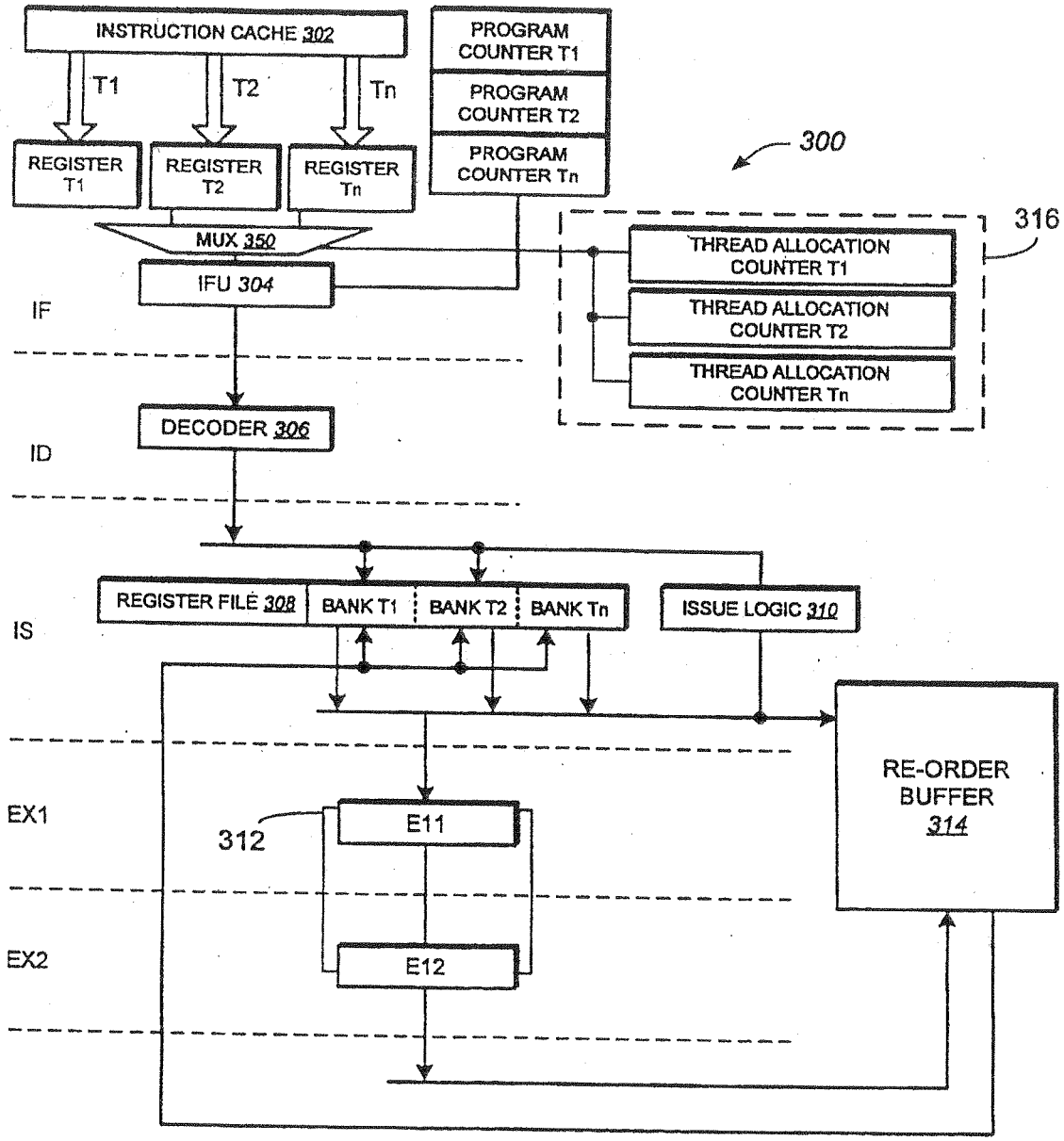

INSTRUCTION CACHE 302
T1
T2
Tn
REGISTER T1
REGISTER T2
REGISTER Tn
PROGRAM COUNTER T1
PROGRAM COUNTER T2
PROGRAM COUNTER Tn
300
316
MUX 350
IFU 304
THREAD ALLOCATION COUNTER T1
THREAD ALLOCATION COUNTER T2
THREAD ALLOCATION COUNTER Tn
IF
DECODER 306
ID
REGISTER FILE 308
BANK T1
BANK T2
BANK Tn
ISSUE LOGIC 310
IS
RE-ORDER BUFFER 314
EX1
312
E11
EX2
E12

FIG._3

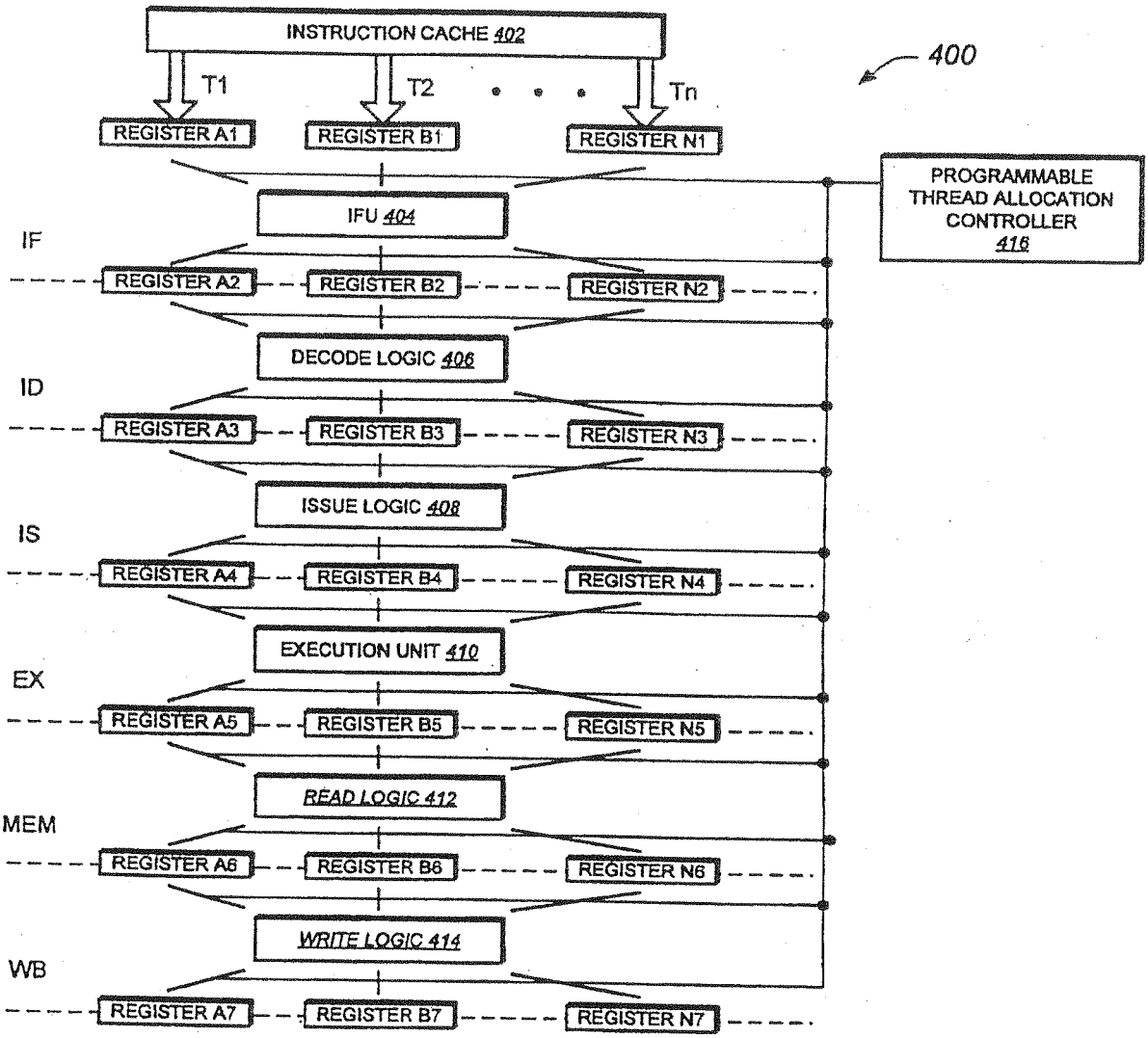

INSTRUCTION CACHE 402
400
T1
T2
Tn
REGISTER A1
REGISTER B1
REGISTER N1
PROGRAMMABLE THREAD ALLOCATION CONTROLLER 416
IFU 404
IF
REGISTER A2
REGISTER B2
REGISTER N2
DECODE LOGIC 406
ID
REGISTER A3
REGISTER B3
REGISTER N3
ISSUE LOGIC 408
IS
REGISTER A4
REGISTER B4
REGISTER N4
EXECUTION UNIT 410
EX
REGISTER A5
REGISTER B5
REGISTER N5
READ LOGIC 412
MEM
REGISTER A6
REGISTER B6
REGISTER N6
WRITE LOGIC 414
WB
REGISTER A7
REGISTER B7
REGISTER N7

FIG._4

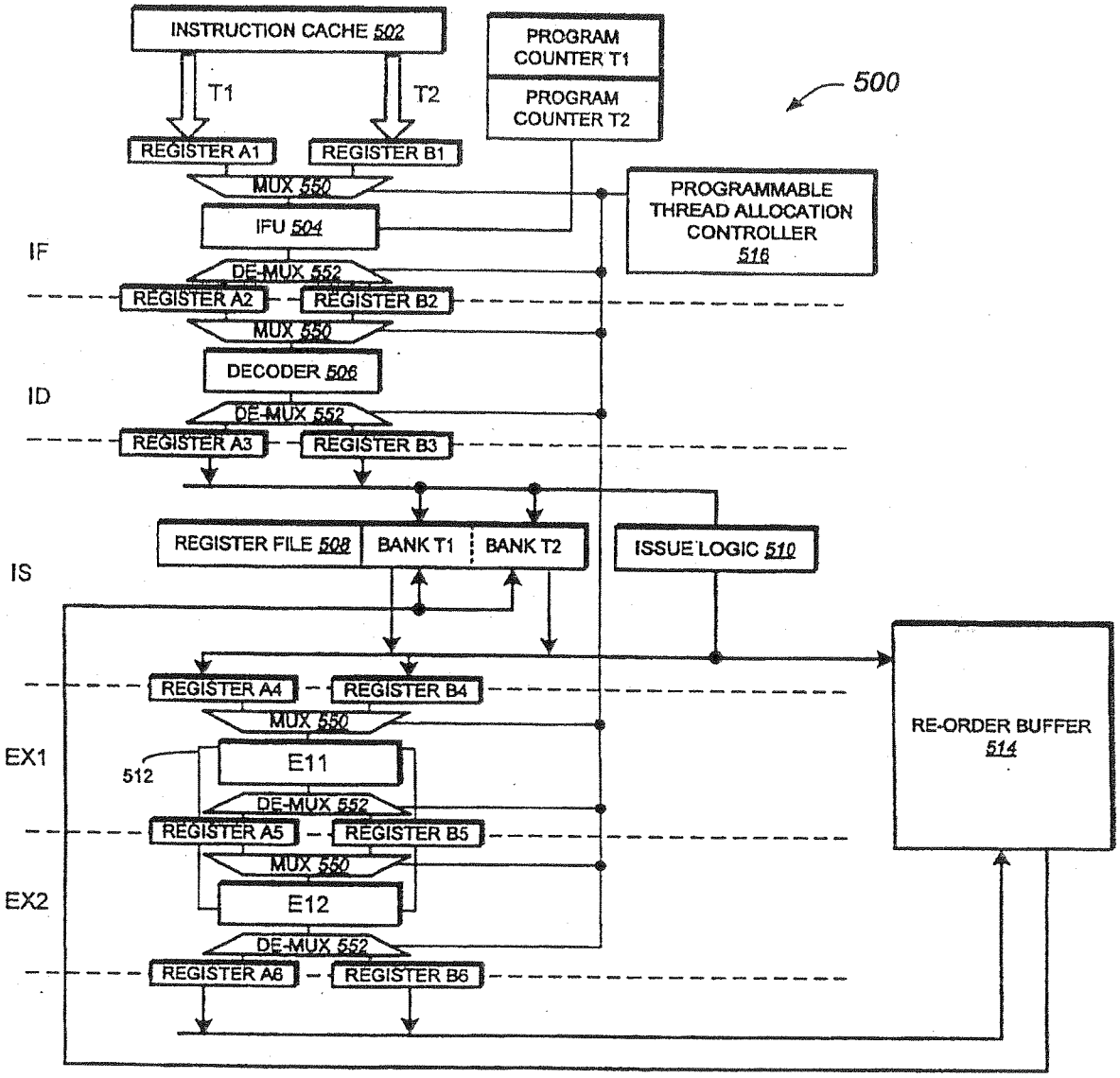

INSTRUCTION CACHE 502
T1
T2
PROGRAM COUNTER T1
PROGRAM COUNTER T2
500
REGISTER A1
REGISTER B1
MUX 550
IFU 504
PROGRAMMABLE THREAD ALLOCATION CONTROLLER 516
IF
DE-MUX 552
REGISTER A2
REGISTER B2
MUX 550
DECODER 506
ID
DE-MUX 552
REGISTER A3
REGISTER B3
REGISTER FILE 508
BANK T1
BANK T2
ISSUE LOGIC 510
IS
RE-ORDER BUFFER 514
REGISTER A4
REGISTER B4
MUX 550
EX1
512
E11
DE-MUX 552
REGISTER A5
REGISTER B5
MUX 550
EX2
E12
DE-MUX 552
REGISTER A6
REGISTER B6

FIG._5

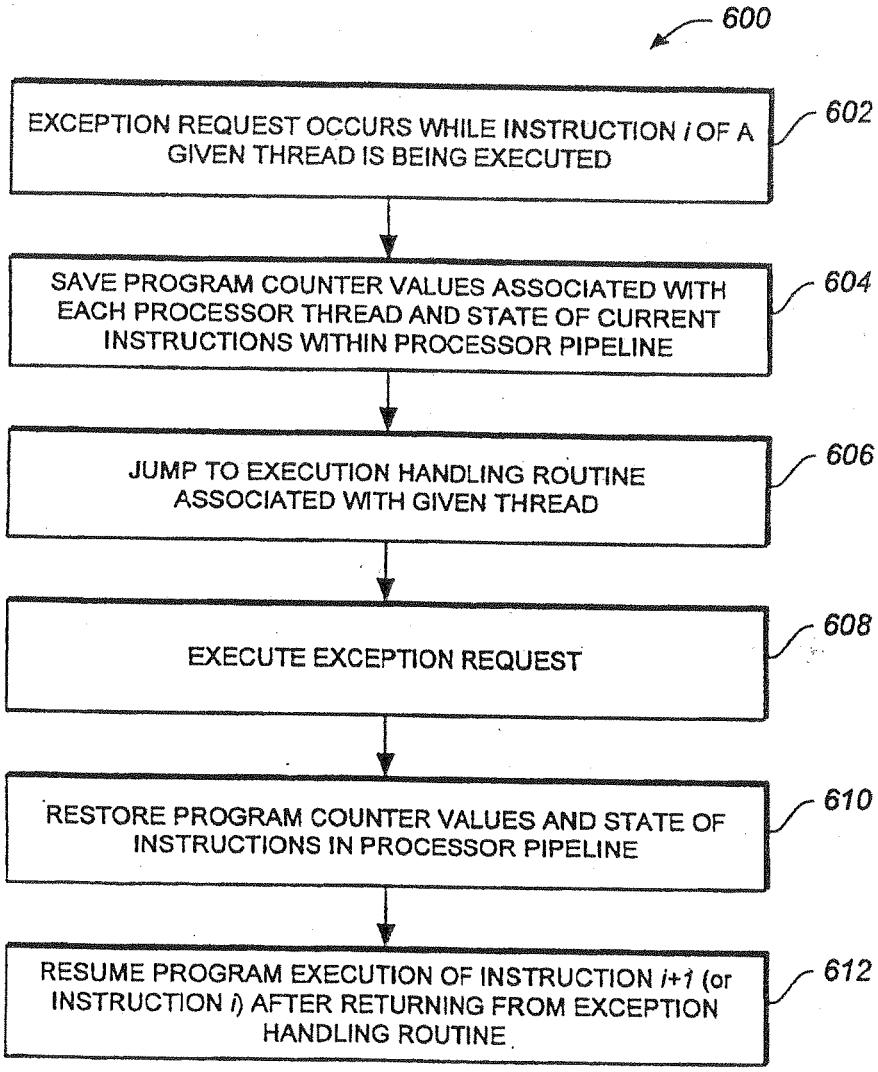

600
EXCEPTION REQUEST OCCURS WHILE INSTRUCTION *i* OF A GIVEN THREAD IS BEING EXECUTED
602
SAVE PROGRAM COUNTER VALUES ASSOCIATED WITH EACH PROCESSOR THREAD AND STATE OF CURRENT INSTRUCTIONS WITHIN PROCESSOR PIPELINE
604
JUMP TO EXECUTION HANDLING ROUTINE ASSOCIATED WITH GIVEN THREAD
606
EXECUTE EXCEPTION REQUEST
608
RESTORE PROGRAM COUNTER VALUES AND STATE OF INSTRUCTIONS IN PROCESSOR PIPELINE
610
RESUME PROGRAM EXECUTION OF INSTRUCTION *i+1* (or INSTRUCTION *i*) AFTER RETURNING FROM EXCEPTION HANDLING ROUTINE
612

FIG._ 6

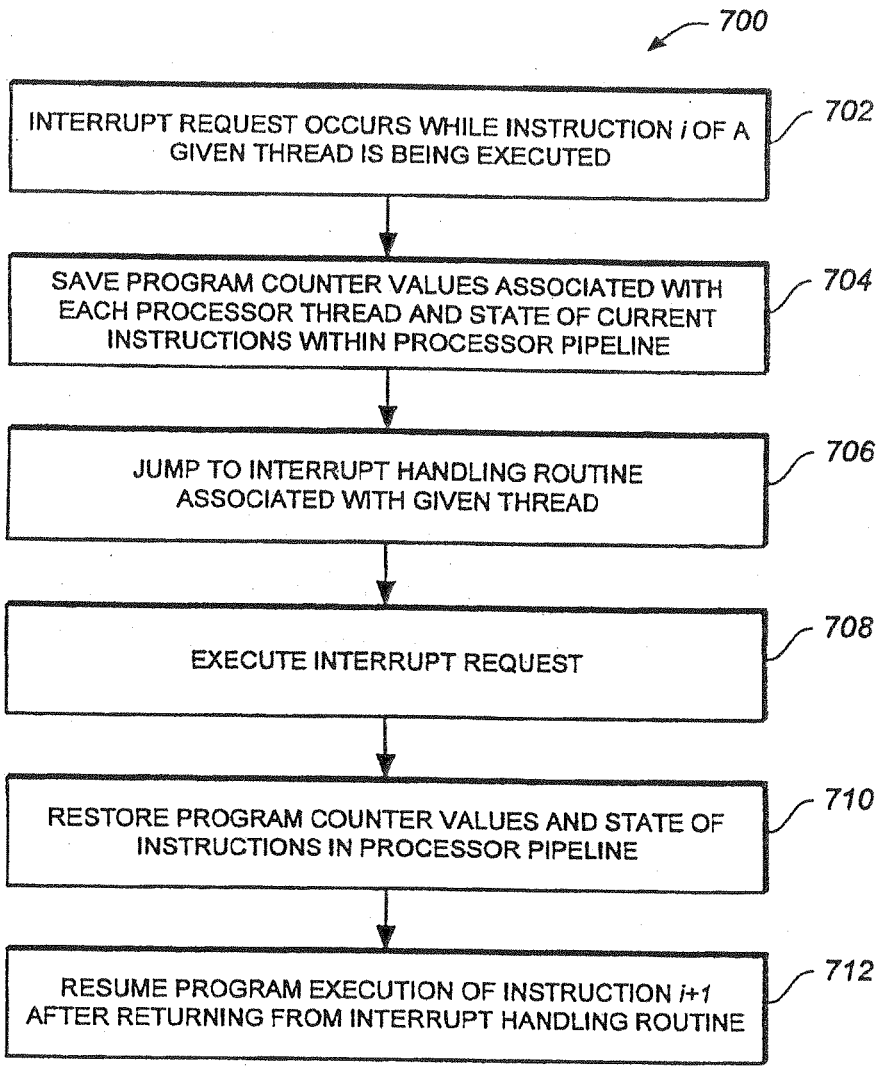

700
INTERRUPT REQUEST OCCURS WHILE INSTRUCTION i OF A GIVEN THREAD IS BEING EXECUTED
702
SAVE PROGRAM COUNTER VALUES ASSOCIATED WITH EACH PROCESSOR THREAD AND STATE OF CURRENT INSTRUCTIONS WITHIN PROCESSOR PIPELINE
704
JUMP TO INTERRUPT HANDLING ROUTINE ASSOCIATED WITH GIVEN THREAD
706
EXECUTE INTERRUPT REQUEST
708
RESTORE PROGRAM COUNTER VALUES AND STATE OF INSTRUCTIONS IN PROCESSOR PIPELINE
710
RESUME PROGRAM EXECUTION OF INSTRUCTION i+1 AFTER RETURNING FROM INTERRUPT HANDLING ROUTINE
712

FIG._7